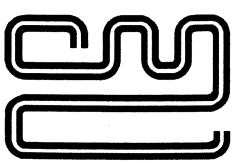
# Integrated Circuits Data Book

Edition 2





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# Integrated Circuits Data Book

Sectional Contents

# Integrated Circuits Data Book

Section 1

# Product Selection

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# Consumer Microcircuits Limited

**Consumer Microcircuits Limited (CML)** is a member of the highly successful CML Microsystems Plc group of companies, and is based at Witham in England.

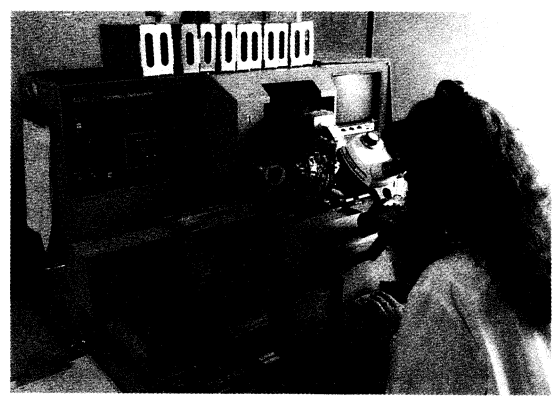
For over 20 years CML has been involved in the design and manufacture of specialized integrated circuits for Communications Markets Worldwide.

Specializing in audio processing and signalling devices, the company products utilize a mixed analogue and digital CMOS process. The combination of detailed system knowledge and engineering capability have resulted in products for Two-Way Mobile and Cellular radio, Telecommunications, Data-Communications, Voice Security and Military Communications.

As part of a 'total-capability' offering, CML has its own extensive modern production and packaging facilities producing both plastic and ceramic devices.
All microcircuit products are offered in surface mount or dual-in-line packages; 100 percent are tested and fully guaranteed.

This combination of 'on-site' Engineering and Production allows CML to offer the highest level of customer service, quality and prompt delivery.

CML's own team of sales engineers and over 30 Distributors Worldwide ensure customers receive excellent on-going local technical and commercial support.



# CML Product Selector

| Device | Description | Page | Two-Way Mobile Radio | Cellular Radio | Military Comms | Cordless Telephones | Telecoms | Modems for Radio and Data Comms | Paging | Voice Security/ Voice Coding | General Purpose |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FX004 | Voice Band Inverter | 2.3 | P | | . | . | . | . | . | P | S |
| FX009A | Digitally Controlled Amp Array | 10.3 | . | P | . | . | . | . | . | . | P |
| FX013 | HSC Tone Decoder | 7.3 | . | . | . | . | . | . | P | . | . |
| FX019 | Digitally Controlled 'Quad' Amp Array | 10.9 | . | . | . | . | . | . | . | . | P |
| FX105 | Tone Detector | 10.15 | . | . | . | . | . | . | . | . | P |
| FX118 | Duplex Frequency Inverter | 5.3 | . | . | . | P | . | . | . | P | . |
| FX203 | Selcall Tone Codec | 2.11 | P | . | . | . | . | . | . | . | . |
| FX214/224/234 | VSB Scrambler | 9.3 | P | P | . | . | . | . | . | P | S |
| FX304 | C-Net Audio Processor | 3.3 | . | P | . | . | . | . | . | S | . |
| FX306 | Audio Filter Array | 3.9 | P | P | . | . | . | . | . | . | S |
| FX315 | CTCSS Encoder | 2.19 | P | . | . | . | . | . | . | . | . |
| FX316 | NMT Filter Array | 3.15 | . | P | . | . | . | . | . | . | . |
| FX326 | Audio Bandpass Filter | 10.23 | . | . | . | . | . | . | . | . | P |
| FX336 | R2000 Filter Array | 3.21 | P | P | . | . | . | . | . | . | . |
| FX346 | AMPS/TACS, NMT Processor | 3.27 | . | P | . | . | . | . | . | . | . |
| FX365/FX365A | CTCSS Encoder/Decoder | 2.25 | P | . | . | . | . | . | . | . | . |
| FX366 | AMPS/TACS Quad Filter Array | 3.35 | . | P | . | . | . | . | . | . | S |
| FX375 | Private Squelch Circuit | 2.35 | P | . | . | . | . | . | . | P | . |
| FX406 | Unifil® Analogue Processor | 10.29 | . | . | . | . | S | . | . | . | P |
| FX429/529 | FFSK MPT1327/PAA Modem | 6.3 | P | . | . | . | . | P | . | . | . |
| FX439 | FFSK Modem | 8.23 | P | P | . | . | . | P | . | . | . |
| FX469 | 1200/2400 Baud FFSK Modem | 8-29 | . | . | . | . | . | P | . | . | . |
| FX489 | GMSK Modem | 8.37 | . | . | . | . | . | P | . | . | . |
| FX506 | Mobile Radio Audio Processor | 2.45 | P | . | S | . | . | . | . | . | . |

# CML Product Selector .....

| Device | Description | Page | Two-Way Mobile Radio | Cellular Radio | Military Comms | Cordless Telephones | Telecoms | Modems for Radio and Data Comms | Paging | Voice Security/ Voice Coding | General Purpose |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FX609 | CVSD Codec | 9.17 | . | . | . | . | . | . | . | P | P |
| FX611 | 12/16kHz SPM Detector | 6.3 | . | . | . | . | P | . | . | . | . |
| FX613 | Universal Call Progress Decoder | 6.9 | . | . | . | . | P | . | . | . | . |
| FX619 | 'Eurocom' Delta Codec | 4.3 | . | . | P | . | . | . | . | P | . |
| FX621 | Low-Power SPM Detector | 6.17 | . | . | . | . | P | . | . | . | . |
| FX623 | Call Progress Tone Decoder | 6.23 | . | . | . | . | P | . | . | . | . |
| FX629 | 'Military' Delta Modulation Codec | 4.13 | . | . | P | . | . | . | . | P | . |
| FX631 | Low-Voltage SPM Detector | 6.29 | . | . | . | . | P | . | . | . | . |
| FX701P | Frequency Sensitive Switch | 6.37 | . | . | . | . | P | . | . | . | S |
| FX709 | VSR Codec | 9.23 | . | . | . | . | P | . | . | P | P |
| **DBS 800 System** | . . . . . | 2.61 | | | | | | | | | |
| FX802 | DVSR Codec | 2.87 | P | S | . | . | . | . | . | P | . |
| FX803 | Audio Signalling Processor | 2.101 | P | . | . | . | S | . | . | . | . |
| FX805 | Sub-Audio Signalling Processor | 2.117 | P | . | . | . | . | . | . | . | . |
| FX806A | PLMR Audio Processor | 2.133 | P | . | S | . | . | . | . | . | . |
| FX809 | FFSK Modem | 2.145 | P | . | . | . | . | P | . | . | . |
| FX812 | VSR Codec | 3.41 | . | P | . | . | . | . | . | P | . |
| FX816 | NMT Audio Processor | 3.53 | . | P | . | . | . | . | . | . | . |
| FX826 | TACS Audio Processor | 3.65 | . | P | . | . | . | . | . | . | . |
| FX836 | R2000 Audio Processor | 3.77 | . | P | . | . | . | . | . | . | . |
| **Modular Products** | | | | | | | | | | | |
| CM1481 | Non-Predictive Selcall Module | 2.159 | P | . | . | . | . | . | . | . | . |
| **CML Modem Guide** ..... | | 8.2 | | | | | | ● | | | |
| **Application Notes** | Rolling Code Scrambling | 9.13 | | | | | | | | | |
| | RS232 Modem | 8.49 | | | | | | | | | |
| | Trunking (Digital Signalling) | 8.19 | | | | | | | | | |
| | Xtal Configurations | 11.8 | | | | | | | | | |

**KEY to Symbols:**

**P** = Primary Applications **S** = Secondary Applications

## Other CML Products

Products that are in production but not detailed in this publication.
Please Contact Consumer Microcircuits Limited or your local distributor for further information.

| Device | Description | Two-Way Mobile Radio | Cellular Radio | Military Comms | Telecoms | Modems for Radio and Data Comms | Paging | Voice Security Voice Coding | General Purpose | Recommended Replacement FX |
|---|---|---|---|---|---|---|---|---|---|---|
| FX003 | Selcall Decoder | P | . | . | . | . | . | . | . | 203/803 |
| FX101 | Frequency Sensitive Switch | . | . | . | . | . | . | . | P | . |
| FX103 | Q.T.C. Decoder | P | . | . | . | . | P | . | . | . |
| FX107/207/307 | Selective Signalling | . | . | . | . | . | . | . | P | . |
| FX205 | Tone Encoder | . | . | . | . | . | . | . | P | . |
| FX301/401 | Frequency Sensitive Switch | . | . | . | . | . | . | . | P | . |
| FX309 | CVSD Codec | . | . | P | . | . | . | P | P | 609 |
| FX313/323 | Q.T.C. Data Store | P | . | . | . | . | P | . | . | . |
| FX335 | CTCSS Encoder/Decoder | P | . | . | . | . | . | . | . | 365/805 |
| FX403 | Q.T.C. Encoder/Decoder | P | . | . | . | . | . | . | . | |
| FX407/507/607 | Sequential Code Transceiver | P | . | . | . | . | . | . | . | 803 |
| FX409 | FFSK Modem | P | P | . | . | P | . | . | . | 439 |
| FX417/517 | 5-Tone Selcall Transceiver | P | . | . | . | . | . | . | . | 803 |
| FX419 | FFSK Modem | P | P | . | . | P | . | . | . | 439 |
| FX501/601 | Tone Operated Switches | . | . | . | . | . | . | . | P | . |
| FX503 | Programmable Selcall Encoder | P | . | . | . | . | . | . | . | . |
| FX707 | Code Selector | P | . | . | . | . | . | . | . | . |
| FX806 | PLMR Audio Processor | P | . | S | . | . | . | . | . | 806A |

**KEY to Symbols:**

**P** = Primary Applications **S** = Secondary Applications

# Integrated Circuits Data Book

Section 2

# Two-Way Mobile Radio

# CML Semiconductor Products

PRODUCT INFORMATION

# FX004

## Voice Band Inverter

Publication D/004/3 September 1987
Provisional Issue

### Features/Applications

- Fixed Frequency Inversion
- CTCSS Compatible
- Choice of Three Audio Bandwidths and Inversion Frequencies
- $\mu$P Compatible Interface
- Automatic Private/Clear Switching
- Private Mobile Radio
- Community Repeaters
- Interconnect Systems
- Cordless Telephones
- Telephony

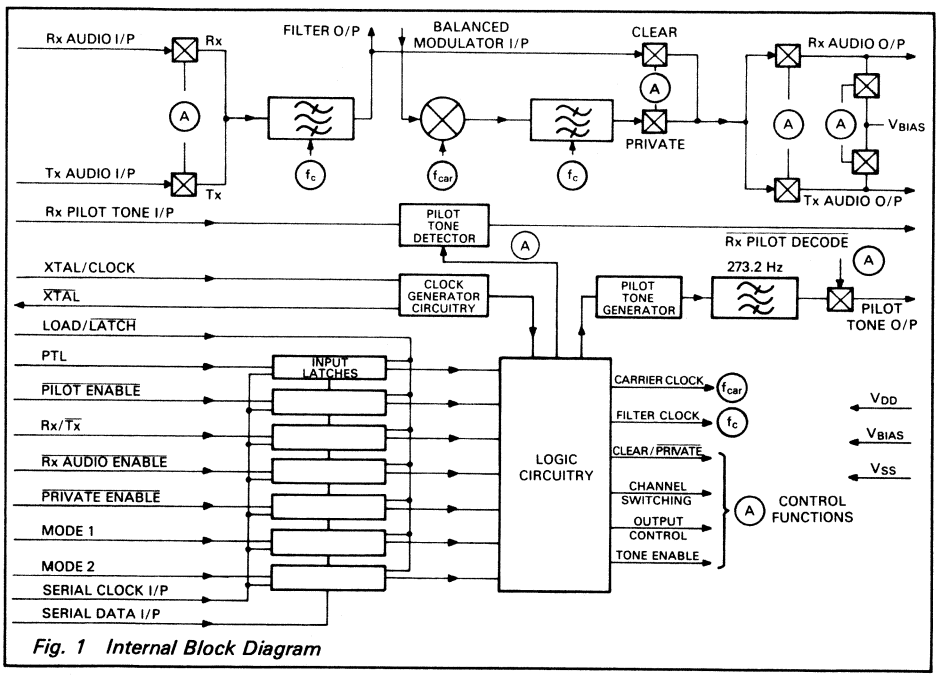



*Fig. 1 Internal Block Diagram*

FX004

### Brief Description

The FX004 is designed to protect speech privacy in Private Mobile Radio and other common channel radio systems. It uses "FIXED FREQUENCY INVERSION" techniques which exchange the low and high frequencies of the transmitted voiceband signal to render the message unintelligible to eavesdropping.

Sharp cut-off in the internal voiceband filters permits operation with CTCSS and similar sub-audio signalling schemes and ensures the high quality of the recovered audio. The device incorporates a programmable clock divider which controls the carrier frequency and filter cut-off frequencies, thus permitting the selection of one of three scrambling codes and transmission bandwidths. A pilot tone generator and detector are used to operate the automatic clear/private facility in mixed equipment systems. Control of the Rx/$\overline{\text{Tx}}$, PTL and privacy functions is by pin selection or use of serial/parallel microprocessor interfaces.

The FX004 operates from a single 5V supply and uses a 1MHz crystal oscillator to ensure correct pitch of the recovered speech. Signal coupling and supply decoupling are the only external components needed and a choice of DIL or SMD packages is available.

| Pin Number | | | Function |
|---|---|---|---|
| DIL FX004J | Quad Plastic FX004LG | PLCC FX004LH | |
| 1 | 1 | 2 | **Filter Output:** This is the audio bandpass filtered signal and is coupled externally to the Balanced Modulator Input pin via capacitor $C_6$. See Fig. 2. |
| 2 | 2 | 3 | **Load/$\overline{\text{Latch}}$:** This pin is used for controlling input latches in both Parallel and Serial loading modes. In Parallel, a logic "1" makes the latches transparent and the following inputs operate directly, PTL, Pilot Enable, Rx/$\overline{\text{Tx}}$, $\overline{\text{Rx Audio Enable}}$, $\overline{\text{Private Enable}}$, Mode 1 and Mode 2. When at logic "0", the data present is latched in. During Serial loading, Load/$\overline{\text{Latch}}$ should be kept low until data is completely loaded then the pin strobed 0 – 1 – 0, latching the new data in. Internal 1MΩ pullup. See Fig. 4. |
| 3 | 3 | 4 | **PTL:** A logic '1' level at this input enables the Audio Output in Rx mode when $\overline{\text{Rx Audio Enable}}$ is at logic '1'. This feature enables channel checking without intercepting a private conversation. Internal 1MΩ pullup. |
| 4 | 4 | 5 | **$\overline{\text{Pilot Enable}}$:** A logic '0' at this input enables the 273.2 Hz pilot tone at the Tx Pilot Tone Output when in Tx mode. Internal 1MΩ pullup. |
| 5 | 5 | 6 | **Rx/$\overline{\text{Tx}}$:** This input selects the receive or transmit operating mode. Logic '1' is Rx, logic '0' is Tx. Internal 1MΩ pullup. |
| 6 | 6 | 7 | **$\overline{\text{Rx Audio Enable}}$:** A logic '0' at this input enables the Rx Audio path in Rx mode. May be connected to a CTCSS decoder. Internal 1MΩ pullup. |
| 7 | 7 | 8 | **$\overline{\text{Private Enable}}$:** This input controls the input action of the balanced modulator by switching the carrier clock (refer to Table 1). When audio signals are inverted the signal path gain is adjusted automatically to compensate for upper sideband loss. Internal 1MΩ pullup. For an 'Auto-Clear' function this input should be connected to the $\overline{\text{Rx Pilot Decode}}$ pin via external integrating components $R_2$ and $C_9$, see Fig. 2. |
| 8 | 8 | 9 | **Mode 1** } These two inputs control Audio band frequency, Carrier frequency and Loading control mode. See Table 2. Internal 1MΩ pullups. |
| 9 | 9 | 10 | **Mode 2** } |
| 10 | 10 | 13 | **Rx Pilot Tone Input:** This pin is the input to the Rx pilot tone decoder. Signals should be A.C. coupled. See Fig. 2. The tone decoder is disabled in Tx mode. |
| 11 | 11 | 14 | **Rx Audio Input:** This is the audio input pin in Rx mode. Signals should be A.C. coupled. See Fig. 2. |

| Pin Number | | | Function |
|---|---|---|---|
| DIL FX004J | Quad Plastic FX004LG | PLCC FX004LH | |
| 12 | 12 | 15 | $V_{SS}$: Negative supply (GND). |
| 13 | 13 | 16 | **Tx Audio Input:** This is the audio input pin in Tx mode (mic). Signals should be A.C. coupled. See Fig. 2. |
| 14 | 14 | 17 | **Rx Audio Output:** This is the audio output in Rx mode, internally biased at $V_{DD}/2$ in Tx mode. |
| 15 | 15 | 18 | **Tx Audio Output:** This is the audio output in Tx mode, internally biased at $V_{DD}/2$ when Rx mode is selected. |
| 16 | 16 | 20 | **Tx Pilot Tone Output:** This pin outputs the 273.2Hz pilot tone and would normally be summed with the Tx Audio Output to modulate the transmitter. When not enabled or in Rx this output is open circuit (high-impedance). |
| 17 | 17 | 21 | **$\overline{\text{Rx Pilot Decode}}$:** This pin is the output of the pilot tone detector, it outputs a logic '0' when a valid 273.2Hz tone is input. Has high impedance load to $V_{DD}$ for wired 'OR' connection to other pins. For an 'Auto-Clear' function this input should be connected to the Private Enable pin via external integrating components $R_2$ and $C_9$, see Fig. 2. |
| 18 | 18 | 22 | $V_{BIAS}$: This is the bias pin and is set internally to $V_{DD}/2$. It should be externally decoupled using a capacitor of 1.0$\mu$F (minimum) to $V_{SS}$. See Fig. 2. |
| 19 | 19 | 23 | **Serial Data Input:** Data present at this input is clocked into the input register by the "0 – 1" clock transition of the Serial Clock Input. See Fig. 4. Internal 1MΩ pullup. |
| 20 | 20 | 24 | **Serial Clock Input:** The timing clock pulses for serial loading are input here. Internal 1MΩ pullup. |
| 21 | 21 | 25 | **$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter. |
| 22 | 22 | 26 | **Xtal/Clock:** This is the input to the clock oscillator inverter. 1MHz Xtal input or externally derived clock can be injected into this input. |
| 23 | 23 | 28 | $V_{DD}$: Positive supply. A single +5V power supply is required. |
| 24 | 24 | 1 | **Balanced Modulator Input:** This pin should be connected to the Filter Output pin via capacitor $C_6$, see Fig. 2. It is internally biased at $V_{DD}/2$. |
| | | 11, 12 19, 27 | No Internal Connection. |

## External Conditions

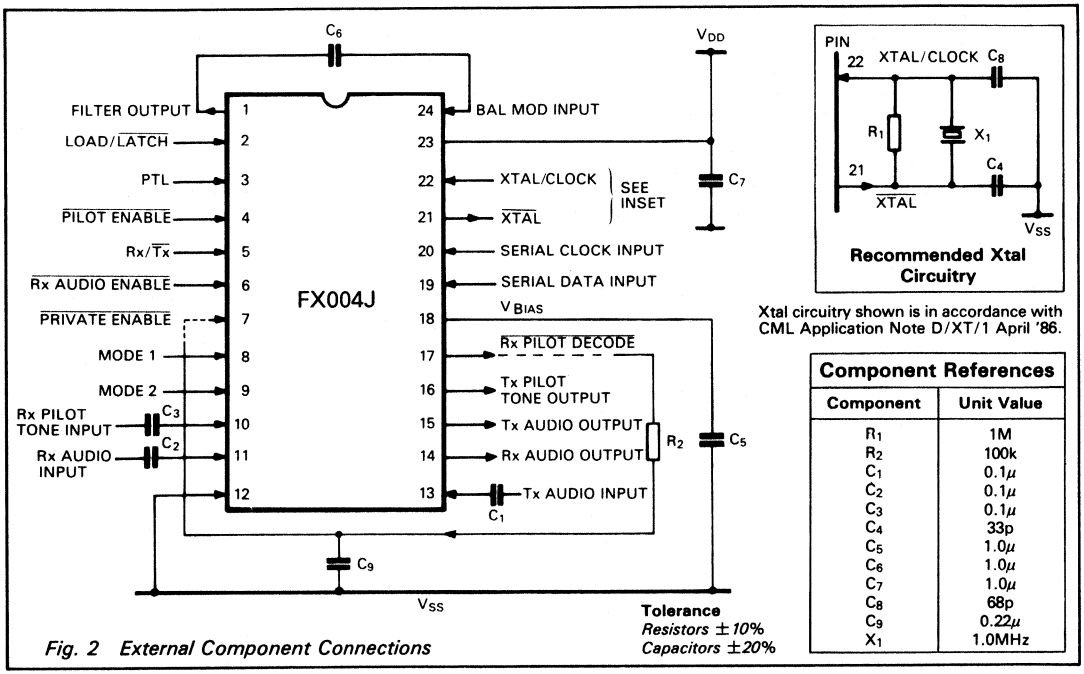



*Fig. 2 External Component Connections*

Xtal circuitry shown is in accordance with CML Application Note D/XT/1 April '86.

**Component References**

| Component | Unit Value |
|---|---|
| $R_1$ | 1M |
| $R_2$ | 100k |
| $C_1$ | 0.1μ |
| $C_2$ | 0.1μ |
| $C_3$ | 0.1μ |
| $C_4$ | 33p |
| $C_5$ | 1.0μ |
| $C_6$ | 1.0μ |
| $C_7$ | 1.0μ |
| $C_8$ | 68p |
| $C_9$ | 0.22μ |
| $X_1$ | 1.0MHz |

### Private Enable (Auto-Clear)

To minimise the effect of noise and signal strength fluctuations on the 'Auto-Clear' function, the use of external integrating components between the Rx Pilot Decode output and the Private Enable input is required. Components $R_2$ and $C_9$, having a time constant of 20ms are recommended, as shown in figure 2.

### Audio Quality

If it is necessary to install the FX004 Voice Band Inverter before the transmitter's existing pre-emphasis stage, an additional pre-emphasis stage before the FX004 followed by a de-emphasis stage after the FX004 will enhance the audio quality. At the receiver the FX004 should be installed between the demodulator and existing de-emphasis stage.

**Input and Output Pin Conditions**

| Rx/$\overline{Tx}$ | PTL | $\overline{\text{Private Enable}}$ | $\overline{\text{Pilot Enable}}$ | $\overline{\text{Rx Audio Enable}}$ | Assumed Rx I/P | Tx I/P | Rx O/P | Tx O/P | Tx Pilot O/P |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | X | X | 1 | X | X | $V_{DD}/2$ | $V_{DD}/2$ | O/C |
| 1 | 1 | X | X | 1 | Signal | X | Non Inverted | $V_{DD}/2$ | O/C |
| 1 | X | 0 | X | 0 | Frequency Inverted | X | Clear (Passband Invert) | $V_{DD}/2$ | O/C |
| 1 | X | 1 | X | 0 | Clear | X | Clear | $V_{DD}/2$ | O/C |
| 0 | X | 1 | 1 | X | X | Signal | $V_{DD}/2$ | Clear (Passband Non-Invert) | O/C |
| 0 | X | 1 | 0 | X | X | Signal | $V_{DD}/2$ | Clear (Passband Non-Invert) | Tone |
| 0 | X | 0 | 0 | X | X | Signal | $V_{DD}/2$ | Inverted (Passband Invert) | Tone |
| 0 | X | 0 | 1 | X | X | Signal | $V_{DD}/2$ | Inverted (Passband Invert) | O/C |

*Table 1 Control Truth Table* (X = don't care)

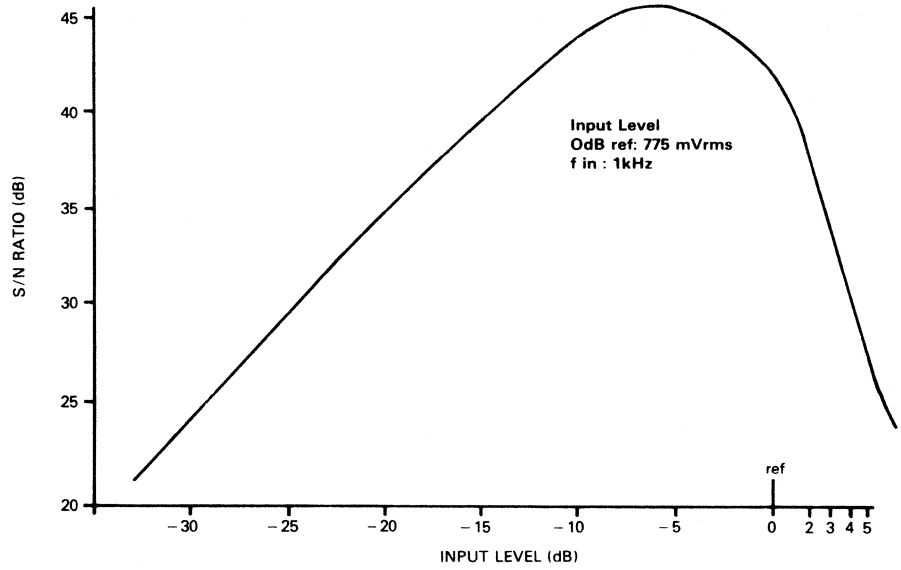
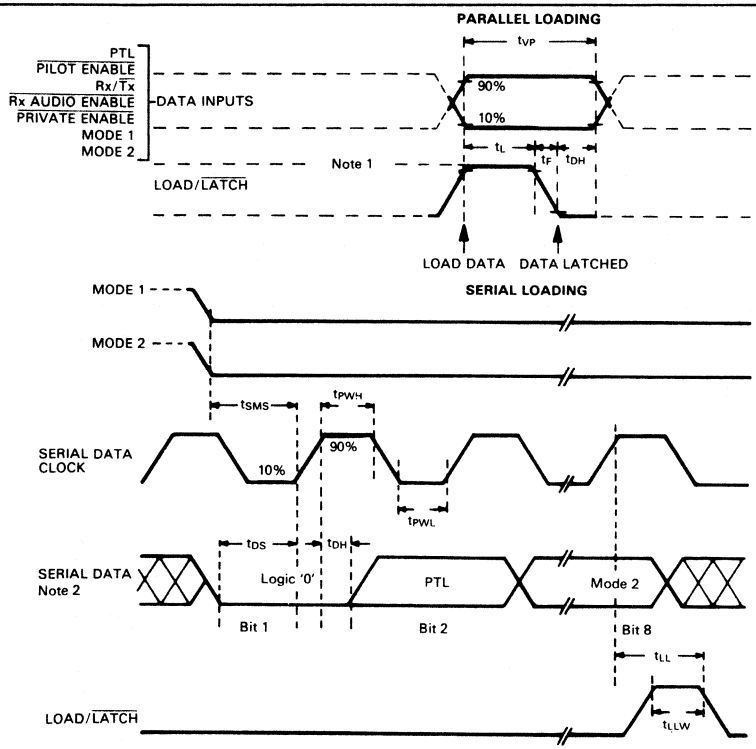



*Fig. 3 Typical S/N Ratio Vs Input Level*




**Timing**

| | |
|---|---|
| $t_{VP}$ | 200ns Min. |
| $t_L$ | 150ns Min. |
| $t_F$ | 50ns Max. |
| $t_{DH}$ | 50ns Min. |
| $t_{SMS}$ | 250ns Min. |
| $t_{DS}$ | 150ns Min. |
| $t_{PWH}$ | 250ns Min. |
| $t_{PWL}$ | 250ns Min. |
| $t_{LL}$ | 250ns Min. |
| $t_{LLW}$ | 150ns Min. |

**NOTES:** 1. With LOAD/$\overline{\text{LATCH}}$ at Logic '1' latches are transparent and data acts directly.

2. Serial Data Loading Sequence: – Logic '0' – PTL – $\overline{\text{PILOT ENABLE}}$ – Rx/$\overline{\text{Tx}}$ – $\overline{\text{Rx AUDIO ENABLE}}$ – $\overline{\text{PRIVATE ENABLE}}$ – MODE 1 – MODE 2.

*Fig. 4 Loading Timing Diagrams*

# Audio Frequency Bands

### Band Usage

Any Audio Band may be selected for clear or private functions, but "intended" use would be:

1. **Band A** Rx/$\overline{Tx}$ Private (333 – 3370Hz)
   **Band B** Rx/$\overline{Tx}$ Clear (300 – 3033Hz)
   Compatible with 'Auto Clear' pilot tone, CTCSS and PMR bandwidths.

2. **Band A** Rx/$\overline{Tx}$ Private/Clear (333 – 3370Hz)
   This is similar to (1) except that clear audio does not comply with mandatory PMR bandwidths.

3. **Band B** Rx/$\overline{Tx}$ Private/Clear (300 – 3033Hz)
   This complies with mandatory PMR bandwidths at all times but its use in "Auto -Clear" Mode (with Pilot Tone) is not recommended because the Pilot Tone is not filtered out at the receiver. This is suitable for fixed mode Private or manual Private/Clear operation.

4. **Band C** Rx/$\overline{Tx}$ Private/Clear (273 – 2757Hz) Required for time-compressed applications where loss of recovered "Private" voice bandwidth is avoided. The Pilot Tone could be used in the time-compressed mode if injected after compression.

*Table 2 Loading Mode/Audio Band Control*

| Parallel Loading Mode | | | | | | Serial Loading Mode | | |
|---|---|---|---|---|---|---|---|---|
| Mode 1 I/P | Mode 2 I/P | Audio Band-Freq. (Hz) | Carrier Freq. (Hz) | Divisor ($f_{clk}/_X$) | Control Mode | Serial Data In Bit 7 | Serial Data In Bit 8 | Audio Band |
| 0 | 1 | C 273 – 2757 | 3030 | X = 330 | Parallel | 0 | 1 | C |
| 1 | 0 | A 333 – 3370 | 3703 | X = 270 | Parallel | 1 | 0 | A |
| 1 | 1 | B 300 – 3033 | 3333 | X = 300 | Parallel | 1 | 1 | B |
| 0 | 0 | – | – | – | Serial | 0 | 0 | B |

**Audio Bands**

The audio band/modulation frequency relationships with their division ratios are shown in Table 2 and are produced with a Xtal/clock frequency ($f_{clk}$) of 1MHz. The modulation frequency and band limits will alter proportionally with Xtal frequency.

*Table 3 Bandwidths*

| Audio Band | Stopband @≥–42dB. F max | Passband | | Attenuation at Carrier Frequency | | Stopband @≥–42dB. F min. |
|---|---|---|---|---|---|---|
| A | 278Hz | 333Hz | 3370Hz | 3703Hz | 20dB | 4036Hz |
| B | 250Hz | 300Hz | 3033Hz | 3333Hz | 20dB | 3633Hz |
| C | 227Hz | 273Hz | 2757Hz | 3030Hz | 20dB | 3302Hz |

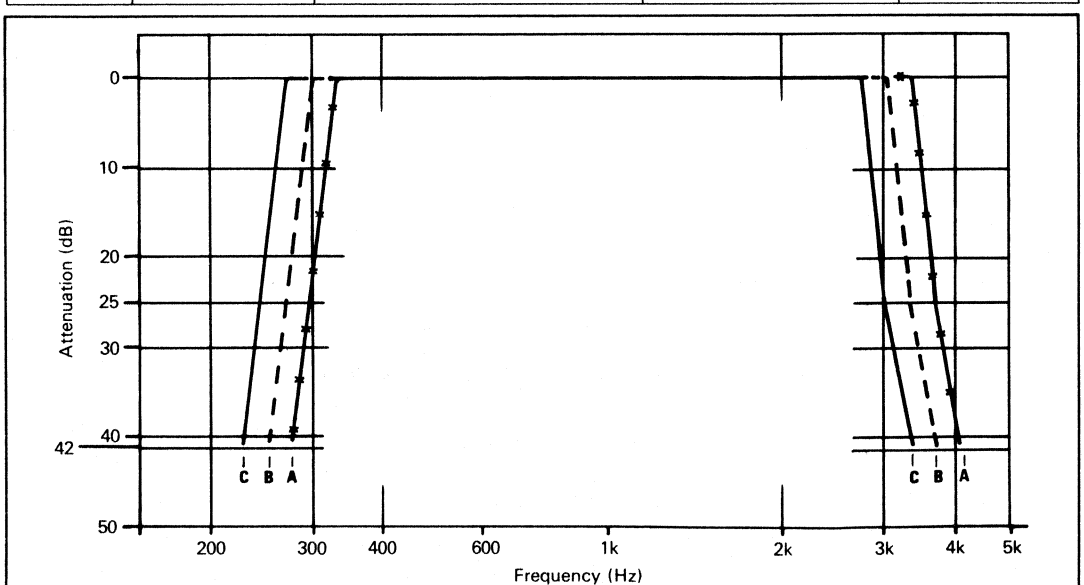



*Fig. 5 Typical Audio Bandpass Filter Responses (1 Filter)*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (supply pins) | | ±30mA |
| (other pins) | | ±20mA |
| Total device dissipation @ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX004J** | −30°C to +85°C (Cerdip) |
| | **FX004LG/LH** | −30°C to +70°C (Plastic) |
| Storage temperature range: | **FX004J** | −55°C to +125°C (Cerdip) |
| | **FX004LG/LH** | −40°C to +85°C (Plastic) |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

$V_{DD}$ = +5V, $T_{amb}$ = 25°C, Xtal/Clock ($f_{clk}$) = 1MHz, 0dB ref: 775mVrms.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | 1 | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | – | 8.0 | – | mA |
| Audio Input Impedance | | – | 500 | – | kΩ |
| Audio Output Impedance | | – | 500 | – | Ω |
| Logic Input Impedance | | – | 1 | – | MΩ |
| Logic Output Impedance | | | | | |
| (Rx Pilot Decode) To $V_{DD}$ | | – | 100 | – | kΩ |
| To $V_{SS}$ | | – | 500 | – | Ω |
| Input Logic '1' | 1 | 3.5 | – | – | V |
| Input Logic '0' | 1 | – | – | 1.5 | V |
| Output Logic '1' | 1 | 4 | – | – | V |
| Output Logic '0' | 1 | – | – | 1 | V |
| **Dynamic Values:** | 1 | | | | |
| Audio Input Levels Rx/Tx | 8 | – | −8 | – | dB |
| Audio Output Levels Rx/Tx | | – | −8 | – | dB |
| **Audio Bandpass Filter (in clear)** | | | | | |
| Passband Frequencies Band A | 2 | 333 | – | 3370 | Hz |
| Passband Frequencies Band B | 2 | 300 | – | 3033 | Hz |
| Passband Frequencies Band C | 2 | 273 | – | 2757 | Hz |
| Passband Gain | 5 | – | 0 | – | dB |
| Passband Ripple | 5 | – | ±1 | – | dB |
| Output Noise Level | 3 | – | −50 | – | dB |
| Insertion Loss | | – | 0 | – | dB |
| Total Harmonic Distortion | 9 | – | 2 | 5 | % |
| **Pilot Tone Detector** | | | | | |
| Sensitivity | | – | 13 | – | mVrms |
| Response Time | 6 | – | 50 | – | ms |
| Talk off and Falsing | 4 | | | | |
| **Pilot Tone Output** | | | | | |
| Tone Output Level | | −2 | 0 | +2 | dB |
| Distortion | | – | – | 5 | % |
| Tone Frequency | 7 | – | 273.2 | – | Hz |
| **Parallel/Serial Inputs (Fig. 4)** | | | | | |
| Parallel Data Valid Time ($t_{VP}$) | | 200 | – | – | ns |
| Parallel Load Time ($t_L$) | | 150 | – | – | ns |
| Pulse Fall Time ($t_F$) | | – | – | 50 | ns |
| Data Hold Time ($t_{DH}$) | | 50 | – | – | ns |
| Serial Mode Set Up Time ($t_{SMS}$) | – | 250 | – | – | ns |
| Data Set Up Time ($t_{DS}$) | | 150 | – | – | ns |
| Clock 'High' Pulse Width ($t_{PWH}$) | | 250 | – | – | ns |
| Clock 'Low' Pulse Width ($t_{PWL}$) | | 250 | – | – | ns |
| Load/Latch Set Up Time ($t_{LL}$) | | 250 | – | – | ns |
| Load/Latch Pulse Width ($t_{LLW}$) | | 150 | – | – | ns |

**Notes:**

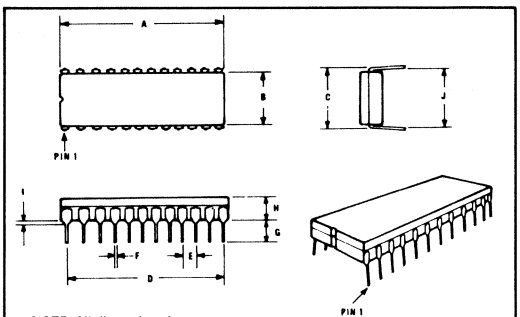
1. *Characteristics specified at 5V $V_{DD}$.*
2. *Bandpass limits at −1dB of mean passband level.*
3. *Measured at the Rx audio output in Private with Rx audio input A.C short circuit.*
4. *Talk off: — for 30mV pilot tone (273Hz), 5kHz white noise at −3dB on tone, 1 drop out per minute is expected. Typically 5ms/drop out.*
   *Falsing: — for 380mVrms (not clipping) 5kHz white noise 25 falses per minute are expected. 10ms/false. Measured without integration components.*
5. *All bandpass filters display similar performances. See figure 5.*
6. *Tested with composite signal of 300 mVrms 1kHz tone, Pilot tone 30mVrms in white noise of 5kHz at 75mVrms.*
7. *In Tx only.*
8. *See figure 3 with respect to signal to noise ratio.*
9. *For −3dB, 1kHz input.*

## Package Outlines

The FX004J, the cerdip package, is illustrated in *Figure 6*. The 'LG' version is shown in *Figure 7*, and the 'LH' version in *Figure 8*. Both 'LG' and 'LH' packages are supplied in conductive trays for handling convenience.

To allow complete identification, the FX004LG and LH packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4 for LG packages, between pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 6* **FX004J** *DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 32.03 | 31.50 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 } | TYPICAL |
| F | 0.46 } | |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 | TYPICAL |
| J | 18.20 | 16.54 |

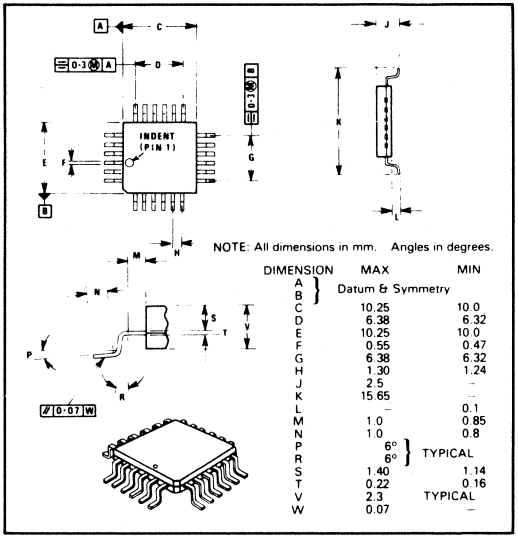
## Ordering Information

| | |
|---|---|
| **FX004J** | **24-pin cerdip DIL** |
| **FX004LG** | **24-pin quad plastic encapsulated, bent and cropped.** |
| **FX004LH** | **28-lead Plastic leaded chip carrier.** |

## Handling Precautions

The FX004J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

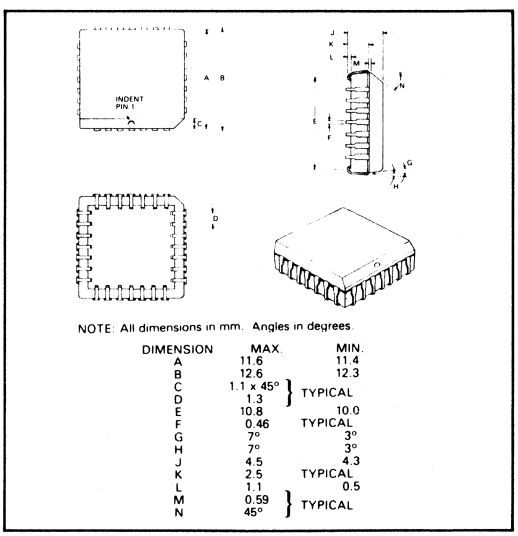
*Fig. 7* **FX004LG** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A } | Datum & Symmetry | |
| B } | | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° } | TYPICAL |
| R | 6° } | |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig. 8* **FX004LH** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 11.6 | 11.4 |
| B | 12.6 | 12.3 |
| C | 1.1 x 45° } | TYPICAL |
| D | 1.3 } | |
| E | 10.8 | 10.0 |
| F | 0.46 | TYPICAL |
| G | 7° | 3° |
| H | 7° | 3° |
| J | 4.5 | 4.3 |
| K | 2.5 | TYPICAL |
| L | 1.1 | 0.5 |
| M | 0.59 } | TYPICAL |
| N | 45° } | |

# CML Semiconductor Products

PRODUCT INFORMATION

# FX203 Selcall Tone Codec with Microprocessor Interface

Publication D/203/2 October 1991
Provisional Issue

## Features/Applications

- Single-Chip Selcall Codec
- CCIR, EEA or ZVEI/SZVEI Versions
- On-Chip General Purpose Timer
- Separate General Purpose 4-bit Input/2-bit Output Port
- Mobile or Handheld Selcall
- 4-bit Microprocessor I/O Data Port
- Powersave Facility
- Uses Low-Cost 4MHz Xtal
- Low-Power 5V CMOS Process

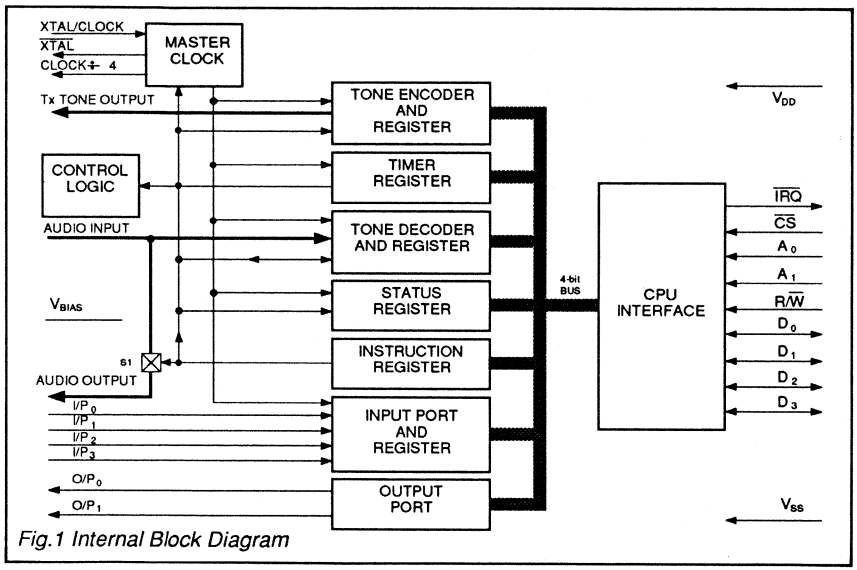



*Fig.1 Internal Block Diagram*

**FX203**

## Brief Description

The FX203 is a single-chip 'N' tone Selective Call encoder-decoder peripheral intended for use with a host microprocessor. The device is available in 3 toneset formats, CCIR, EEA or ZVEI/SZVEI.

A 4-bit data I/O bus, 2-bit address, $\overline{CS}$, R/$\overline{W}$ and $\overline{IRQ}$ lines are provided for connection to the microprocessor.

Separate general purpose 4-bit input and 2-bit output ports are available to allow external circuitry access to the microprocessor via this device. Functions such as 'PTT,' 'Rx Squelch,' 'Alert Bleeps' and 'Lamp Drivers' could operate through this facility.

An on-chip general purpose timer is provided for such functions as Rx and Tx tone period timing. Time periods of between 10ms and 140ms in 10ms steps may be programmed via the microprocessor interface.

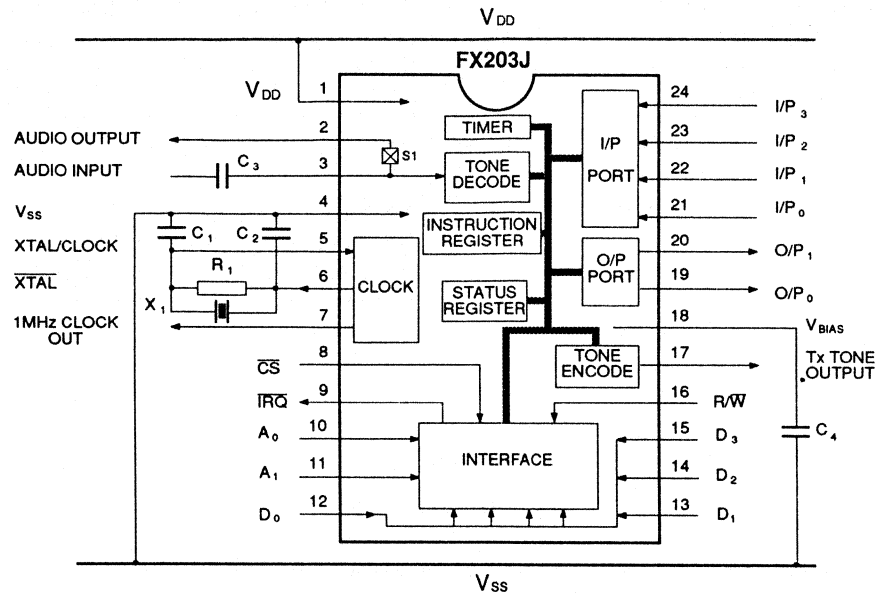
The FX203 reference oscillator utilizes a low-cost 4.0 MHz Xtal or externally derived clock. The divide by 4 (1.0 MHz) output may be used to drive the clock circuitry of other devices such as the FX365 CTCSS Encoder/Decoder, FX004 Voice Band Inverter, or the FX214 VSB Audio Scrambler.

The FX203 requires a single 5-volt supply and utilizes 'chip enable'/'powersave' facilities for reduced current consumption in the Standby mode.

| Pin Number | | Function |
|---|---|---|
| DIL FX203*J | Quad FX203*LG FX203*LS | * C, E, Z tonesets |
| 1 | 1 | **$V_{DD}$ :** Positive supply rail. A single +5-volt power supply is required. |
| 2 | 2 | **Audio Output :** The received audio output, selected by the Audio Output Enable bit, $D_1$, in the Instruction Register. This output could be the result of a squelch function. |
| 3 | 3 | **Audio Input :** The audio input to the Tone Decoder and audio output switching. The composite (voice and tone) received audio requires to be coupled to this pin via capacitor $C_3$. See Figures 1 and 2. |
| 4 | 4 | **$V_{SS}$ :** Negative supply rail (GND). |
| 5 | 5 | **Xtal/Clock :** The input to the clock oscillator inverter. A 4.0 MHz Xtal or externally derived clock should be connected here. See Figure 2. |
| 6 | 6 | **$\overline{\text{Xtal}}$ :** The output of the 4.0 MHz clock oscillator. See Figure 2. |
| 7 | 7 | **Clock ÷ 4 :** A 1.0 MHz ( $X_1 \div 4$ ) clock is available at this output for external use. Note the output impedance and source current limits. |
| 8 | 8 | **$\overline{\text{CS}}$ :** The chip select input. A logic '0' on this pin will select the FX203. See Figure 3, Timing diagram. |
| 9 | 9 | **$\overline{\text{IRQ}}$ :** The Interrupt logic output. An active interrupt is set as a logic '0'. This pin can be wire OR'd to external circuitry. An external pullup resistor may be required on this output.<br>Conditions that cause Interrupt Requests are:<br>(1) Rx Ready (tone decoded) – $\overline{\text{IRQ}}$ and Status bit $D_0$<br>(2) Timer Cycle expired – $\overline{\text{IRQ}}$ and Status bit $D_1$<br>(3) Input Port data change – $\overline{\text{IRQ}}$ and Status bit $D_2$ |
| 10<br>11 | 10<br>11 | **$A_0$ :** Register address pins. These inputs, with the R/$\overline{\text{W}}$ input, select the internal<br>**$A_1$ :** register to be addressed via the CPU Interface ($D_0 - D_3$) using the logic states as detailed below. Register information is detailed on pages 4 and 5. |
| 12<br>13<br>14<br>15 | 12<br>13<br>14<br>15 | **$D_0$ :**<br>**$D_1$ :** The 4-bit microprocessor interface for communication with the internal<br>**$D_2$ :** registers as directed by the $A_0$, $A_1$ and R/$\overline{\text{W}}$ inputs.<br>**$D_3$ :** |
| 16 | 16 | **R/$\overline{\text{W}}$ :** The Read/Write logic input, which with the $A_0$ and $A_1$ address inputs determine the Microprocessor/ Register communication. Read = logic'1', Write = logic '0'. |
| 17 | 17 | **Tx Tone Output :** The transmitted tone output of the Tone Encoder. Tone 'F' (Notone) will cause this output to go to $V_{BIAS}$. When not enabled this output is high impedance. |
| 18 | 18 | **$V_{BIAS}$ :** The output of the on-chip bias circuitry, held at $V_{DD}/2$. When the Encoder is not enabled this pin will be at $V_{SS}$. This pin requires to be decoupled to $V_{SS}$ with a capacitor, $C_4$. |
| 19<br>20 | 19<br>20 | **$O/P_0$ :** The 2-bit logic output port whose state is controlled by the Instruction<br>**$O/P_1$ :** Register ($D_2$, $D_3$). |
| 21<br>22<br>23<br>24 | 21<br>22<br>23<br>24 | **$I/P_0$ :**<br>**$I/P_1$ :** The 4-bit logic input port. See page 5.<br>**$I/P_2$ :** These pins each have an internal 1MΩ pullup resistor.<br>**$I/P_3$ :** |

| | R/$\overline{\text{W}}$ | $A_1$ | $A_0$ | Register |
|---|---|---|---|---|
| | 0 | 0 | 0 | Tone Encode |
| **Write** | 0 | 0 | 1 | Instruction |
| | 0 | 1 | 0 | Timer |
| | 1 | 0 | 0 | Tone Decode |
| **Read** | 1 | 0 | 1 | Status |
| | 1 | 1 | 0 | Input Port |

## External Components




| Component | Value | Component | Value |
|---|---|---|---|
| $R_1$ | 1MΩ | $C_3$ | 0.1µF |
| $C_1$ | 33pF | $C_4$ | 1.0µF |
| $C_2$ | 33pF | $X_1$ | 4.0MHz |

Tolerances: R = ± 10%. C = ± 20%.

*Fig.2 External Component Connections*

## General and Operational Notes

### Power-up Arrangements

It is recommended that the following sequence be employed to set all internal registers to a start-up state upon power-up.

**Write** – Hex. '0' to Timer Register for a period greater than Power-Up Reset Time (TS).

*The following actions clear the Status Register and reset all interrupts.*

**Read** – Status Register.

**Read** – Tone Decode Register.

**Read** – Input Port Register.

**Write** – To Output Port as required.

*The data in the Decoder Register is not valid until after the first active Decoder interrupt has been received.*

### Operation

Operation of the FX203 is Full Duplex.

The receive mode is achieved by writing any Timer setting except Hex. '0.'

The Tone Decode Register must be read before the expected arrival of the next tone, as register contents are overwritten.

Data written to the device via the CPU Interface is acted upon at the end of the Data Set-up Time ($t_{DSW}$), when the $\overline{CS}$ input goes high (logic '1').

The Timer may be written to at any time. The Timer is reset when data is written to it. The new Timer period starts when the $\overline{CS}$ input goes high (logic '1').

### Layout

All external components (as recommended in Figure 2) should be kept close to the package.

Tracks should be kept short, particularly the Audio and $V_{BIAS}$ inputs.

Xtal/clock and digital tracks should be kept well away from analogue circuitry. Analogue inputs and outputs should be screened wherever possible and the high level Tx Tone Output kept separate from other analogue inputs and outputs.

A "ground plane" connected to $V_{SS}$ will assist in eliminating external pick-up.

## Internal Register States

The following descriptions show the condition of each of the 6 registers used by the FX203 to communicate with both microprocessor and radio systems. Table 1 details the hexadecimal 4-bit data words used in these registers. Timing information for the CPU Interface is given in Figure 3.

### Instruction Register — Write Only — $R/\overline{W} = 0$ $A_1 = 0$ $A_0 = 1$

The Instruction Register addresses the functions of the FX203

| Bit No | Logic | Function | | |
|---|---|---|---|---|
| $D_0$ | 1 | **Tx Enable :** | – | Enables the Transmitter circuitry. |
| | 0 | | – | Disables the Transmitter circuitry. |
| $D_1$ | 1 | **Audio Output Enable :** | – | Switches the Audio Input to the Audio Output. |
| | 0 | | – | Disables the Audio Output switch (S1). |
| $D_2$ | 1 or 0 | **Output Port O/$P_0$ :** | – | The logic state of this line. |
| $D_3$ | 1 or 0 | **Output Port O/$P_1$ :** | – | The logic state of this line. |

### Tone Encode Register — Write Only — $R/\overline{W} = 0$ $A_1 = 0$ $A_0 = 0$

$D_0$ $D_1$ $D_2$ $D_3$

**LSB** **MSB**

The 4-bit Hex. word written to this register will produce the required tone (Table 1) at the TX Tone Output

### Tone Decode Register — Read Only — $R/\overline{W} = 1$ $A_1 = 0$ $A_0 = 0$

$D_0$ $D_1$ $D_2$ $D_3$

**LSB** **MSB**

The 4-bit Hex. word in this register will indicate the frequency (Table 1) of the received tone

### Timer Register — Write Only — $R/\overline{W} = 0$ $A_1 = 1$ $A_0 = 0$

$D_0$ $D_1$ $D_2$ $D_3$

**LSB** **MSB**

The 4-bit Hex. word written to this register will automatically reset the timer and start a timing cycle as shown

| Hex Code | | Function/Tone Period |
|---|---|---|
| 0 | – | Disable Receiver, Transmitter and Timer |
| | Reset and start tone period of: | |
| 1 | – | 10ms |
| 2 | – | 20ms |
| 3 | – | 30ms |
| 4 | – | 40ms |
| 5 | – | 50ms |
| 6 | – | 60ms |
| 7 | – | 70ms |
| 8 | – | 80ms |
| 9 | – | 90ms |
| A | – | 100ms |
| B | – | 110ms |
| C | – | 120ms |
| D | – | 130ms |
| E | – | 140ms |
| F | – | Disable Timer operation only |

## Internal Register States

| Status Register | Read Only | $R/\overline{W} = 1$ $A_1 = 0$ $A_0 = 1$ |
|---|---|---|

The Status Register indicates the source of any interrupt

**Bit No** — **Condition** — A logic '1' in the Status Register indicates that the bit is **Set**. The Interrupt line (IRQ) is a logic '0' when active

**$D_0$** — **Rx Ready :**
$D_0$ and an interrupt are **Set** when the Tone Decoder has decoded a received tone and latched the 4-bit Hex. word into the Tone Decode Register. This register requires to be read before the next tone is decoded or that information will be overwritten.
$D_0$ and the interrupt are **Cleared** by reading the Status Register followed by reading the Tone Decode Register.

**$D_1$** — **Timer :**
$D_1$ and an interrupt are **Set** when the intervals programmed by the Timer Register have expired. $D_1$ and the interrupt are **Cleared** after reading the Status Register.

**$D_2$** — **Input Port ($I/P_0 - I/P_3$) :**
$D_2$ and an interrupt are **Set** when the data state at the Input Port changes.
$D_2$ and the interrupt are **Cleared** by reading the Status Register followed by reading the Input Port register.

**$D_3$** — This bit is unallocated. Set at a logic '0.'

| Input Port | Read Only | $R/\overline{W} = 1$ $A_1 = 1$ $A_0 = 0$ |
|---|---|---|

**$D_0$ $D_1$ $D_2$ $D_3$**
**LSB** **MSB**

By reading this register the microprocessor can monitor the state of the 4 logic input pins ($I/P_0 - I/P_3$).This facility allows external systems to communicate with the microprocessor via this device

The FX203 caters for CCIR, EEA and ZVEI/Suppressed ZVEI sequential tone system frequencies in three tone sets, "C," "E" and "Z" respectively, as shown in Table 1.
See the 'Specifications' pages for overall FX203 Tone performance characteristics.

| Hex. Input/Output | $D_3$ | $D_2$ | $D_1$ | $D_0$ | 'C' Tone Set $f_0$ (Hz) | 'E' Tone Set $f_0$ (Hz) | 'Z' Tone Set $f_0$ (Hz) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1981 | 1981 | 2400 |
| 1 | 0 | 0 | 0 | 1 | 1124 | 1124 | 1060 |
| 2 | 0 | 0 | 1 | 0 | 1197 | 1197 | 1160 |
| 3 | 0 | 0 | 1 | 1 | 1275 | 1275 | 1270 |
| 4 | 0 | 1 | 0 | 0 | 1358 | 1358 | 1400 |
| 5 | 0 | 1 | 0 | 1 | 1446 | 1446 | 1530 |
| 6 | 0 | 1 | 1 | 0 | 1540 | 1540 | 1670 |
| 7 | 0 | 1 | 1 | 1 | 1640 | 1640 | 1830 |
| 8 | 1 | 0 | 0 | 0 | 1747 | 1747 | 2000 |
| 9 | 1 | 0 | 0 | 1 | 1860 | 1860 | 2200 |
| A | 1 | 0 | 1 | 0 | 2400 | 1055 | 2800 |
| B | 1 | 0 | 1 | 1 | 930 | 930 | 810 |
| C | 1 | 1 | 0 | 0 | 2247 | 2247 | 970 |
| D | 1 | 1 | 0 | 1 | 991 | 991 | 885 |
| E | 1 | 1 | 1 | 0 | 2110 | 2110 | 2600 |
| F | 1 | 1 | 1 | 1 | Notone | Notone | Notone |

*Table 1 Tone Frequency Programming Codes*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX203J** | -30°C to +85°C (ceramic) |
| | **FX203LG/LS** | -30°C to +70°C (plastic) |
| Storage temperature range: | **FX203J** | -55°C to +125°C (ceramic) |
| | **FX203LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.0 MHz. Audio level 0dB ref: = 775mV rms.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current – | | | | | |
| Rx on, Tx and Timer Disabled | | – | 1.25 | – | mA |
| Rx on, Tx Enabled, Timer Running | 1 | – | 3.0 | – | mA |
| **Interface Levels** | | | | | |
| **CPU Data Port ($D_0$ – $D_3$) In/Out** | 8 | | | | |
| Logic '1' | | 3.5 | – | – | V |
| Logic '0' | | – | – | 1.5 | V |
| Output Logic '1' Source Current | 9 | – | – | 120 | µA |
| Output Logic '0' Sink Current | 10 | – | – | 360 | µA |
| Three State Output Leakage Current | | – | – | 4.0 | µA |
| **Input Port ($I/P_0$ – $I/P_3$) & (R/W, $A_0$, $A_1$, CS )** | | | | | |
| Logic '1' | | 3.5 | – | – | V |
| Logic '0' | | – | – | 1.5 | V |
| **Output Port ($O/P_0$ – $O/P_1$), (IRQ)** | 2 | | | | |
| Logic '1' | | 4.0 | – | – | V |
| Logic '0' | | – | – | 1.0 | V |
| **Impedances** | | | | | |
| Input Port | | 0.1 | 1.0 | – | MΩ |
| Output Port | | – | 15.0 | 50.0 | kΩ |
| Audio Input | 11 | 0.1 | 1.0 | – | MΩ |
| Audio Switch S1 'ON' | 11 | – | 2.0 | 5.0 | kΩ |
| Audio Switch S1 'OFF' | 11 | 1.0 | 10.0 | – | MΩ |
| Tx Tone Output (Enabled) | 14 | – | 1.0 | – | kΩ |
| Tx Tone Output (Disabled) | | 1.0 | 10.0 | – | MΩ |
| Clock + 4 Output | | – | 3.0 | 10.0 | kΩ |
| IRQ Output (Logic '1') | | – | 25.0 | 100.0 | kΩ |
| IRQ Output (Logic '0') | | – | 150.0 | 500.0 | Ω |
| **Encoder** | | | | | |
| Tone Output Level | 1 | -1.0 | 0 | +1.0 | dB |
| Tone Frequency Accuracy 'C' | | -4.0 | *fo* | +4.0 | Hz |
| Tone Frequency Accuracy 'E' | | -0.3 | *fo* | +0.3 | % |
| Tone Frequency Accuracy 'Z' | | -0.3 | *fo* | +0.3 | % |
| Tone Output Risetime | 3 | – | 1.0 | – | ms |
| Total Harmonic Distortion | | – | – | 5.0 | % |

## Specification

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Decoder** | | | | | | |
| Signal Input Range | | 4 | -28.0 | – | +7.0 | dB |
| Decode Bandwidth – | | | | | | |
| Probability > 0.995 | 'C' | 5 | ±1.0 | – | – | % |
| Probability > 0.995 | 'E' | 5 | ±1.0 | – | – | % |
| Probability > 0.995 | 'Z' | 5 | ±2.0 | – | – | % |
| Not Decode Bandwidth – | | | | | | |
| Probability < 0.03 | 'C' | 6 | – | – | ±3.0 | % |
| Probability < 0.03 | 'E' | 6 | – | – | ±3.0 | % |
| Probability < 0.03 | 'Z' | 6 | – | – | ±4.5 | % |
| Noise Response Rate | 'C' | 7,12 | – | 1.0 | – | Digits |
| Noise Response Rate | 'E' | 7,12 | – | 1.0 | – | Digits |
| Noise Response Rate | 'Z' | 7,13 | – | 1.0 | – | Digits |
| Decode Response Time | | | | | | |
| Notone to Tone | | 5 | 20 | 25 | Tp | ms |
| Tone to Notone | | | 33 | – | 53 | ms |
| **Timing** – (Figure 3) | | | | | | |
| Address Set Up Time | $t_{AS}$ | | 50 | – | – | ns |
| Read/Write Set Up Time | $t_{RWS}$ | | 50 | – | – | ns |
| Address Hold Time | $t_{AH}$ | | 0 | – | – | ns |
| Read/Write Recovery Time | $t_{RWR}$ | | 0 | – | – | ns |
| Chip Select Access Time | $t_{ACS}$ | 8 | – | – | 250 | ns |
| Output Hold Time (Read) | $t_{OHR}$ | | 0 | – | 100 | ns |
| Data Set Up Time (Write) | $t_{DSW}$ | | 150 | – | – | ns |
| Data Hold Time (Write) | $t_{DHW}$ | | 20 | – | – | ns |
| Power Up Reset Time | TS | | 3.0 | – | – | ms |

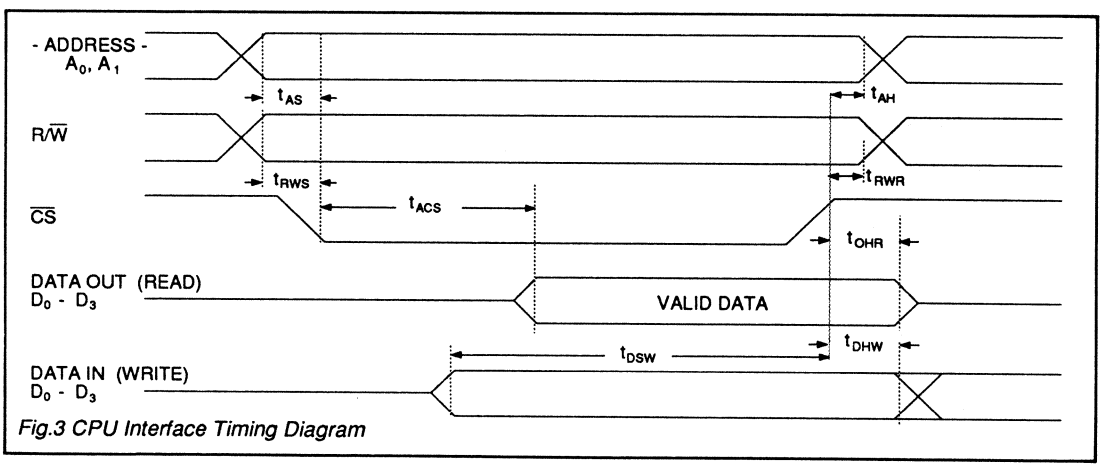



*Fig.3 CPU Interface Timing Diagram*

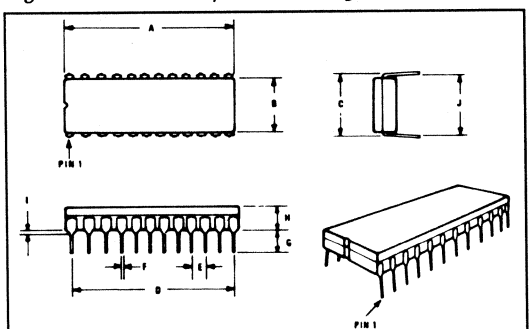
**Notes**

1. No Tx Tone load.
2. Sink/Source currents ≤ 0.1mA.
3. To 90% of nominal output, (from 'F tone' to 'not-F tone').
4. Sine or Square, a.c. coupled input.
5. With minimum tone period (Tp) for the tone set, S/N ratio 0dB.
6. Under all conditions of input amplitude and S/N ratio, with maximum Tp specified for the tone set.
7. Gaussian Noise Input 6kHz band limited with a maximum input level corresponding to 1-digit code falsing rate. (random to random single characters).
8. With each data line loaded as: C = 50pf and R =10kΩ.
9. $V_{OUT}$ = 4.6V
10. $V_{OUT}$ = 0.4V
11. External connections on the Audio Output may alter these values.
12. Single digit response in a 40.0-hour period.
13. Single digit response in a 1.0-hour period.
14. An emiter follower output with an internal 10kΩ pulldown resistor.

## Package Outline

The FX203J, the cerdip package is shown in Figure 4. The 'LG' version is shown in Figure 5 and the 'LS' version in Figure 6.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 4* **FX203*J** *24-pin DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 32.03 | 31.50 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 | TYPICAL |
| F | 0.46 | |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 | TYPICAL |
| J | 18.20 | 16.54 |

## Ordering Information

* Insert the required system toneset

| *CCIR* | *EEA* | *ZVEI/SZVEI* |
|---|---|---|
| * (C) | (E) | (Z) |

**FX203(*)J** – Figure 4
24-pin cerdip DIL

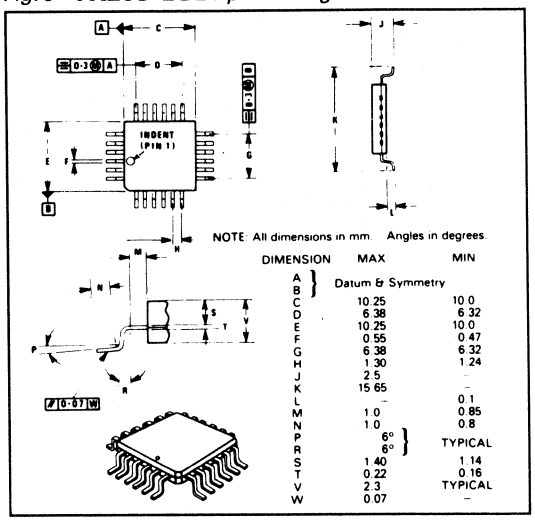
**FX203(*)LG** – Figure 5
24-pin quad plastic encapsulated bent and cropped

**FX203(*)LS** – Figure 6
24-lead plastic leaded chip carrier

## Handling Precautions

The FX203 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

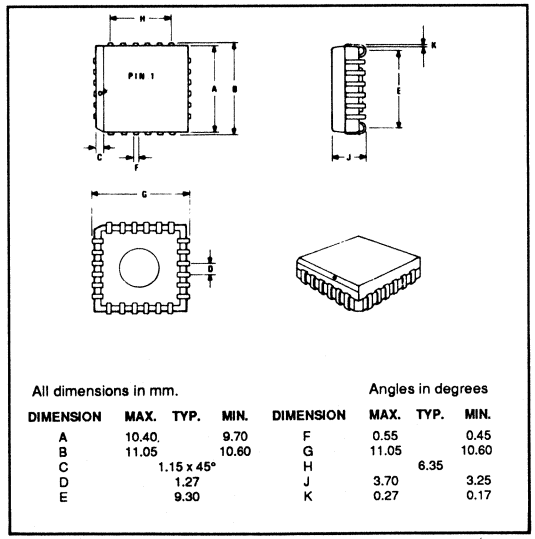
*Fig. 5* **FX203*LG** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig. 6* **FX203*LS** *24-pin Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.40 | | 9.70 | F | 0.55 | | 0.45 |
| B | 11.05 | | 10.60 | G | 11.05 | | 10.60 |
| C | | 1.15 x 45° | | H | | 6.35 | |
| D | | 1.27 | | J | 3.70 | | 3.25 |
| E | | 9.30 | | K | 0.27 | | 0.17 |

# CML Semiconductor Products

PRODUCT INFORMATION

# FX315

## CTCSS Encoder

Publication D/315/4 October 1991

### Features/Applications

- 40 CTCSS Frequencies
- Field Programmable Tone Encoder
- Xtal Frequency Stability
- Low Distortion Sinewave Output
- Low Power 5 volt CMOS
- Surface Mount or DIL Package Style

### Applications

- CTCSS Encode Applications
- Repeater Access Control
- Mobile or Hand Held Radio Squelch Control
- Low Frequency Tone Generation

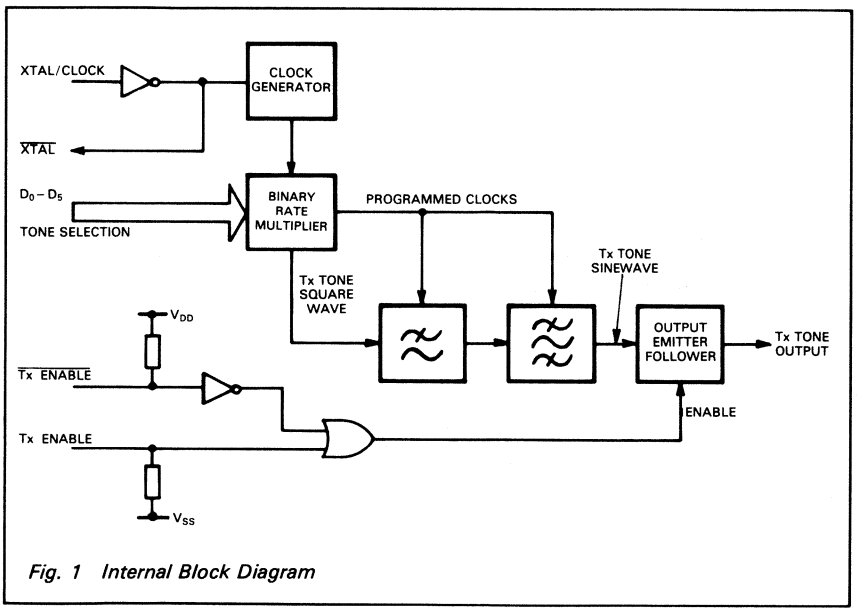



*Fig. 1 Internal Block Diagram*

FX315

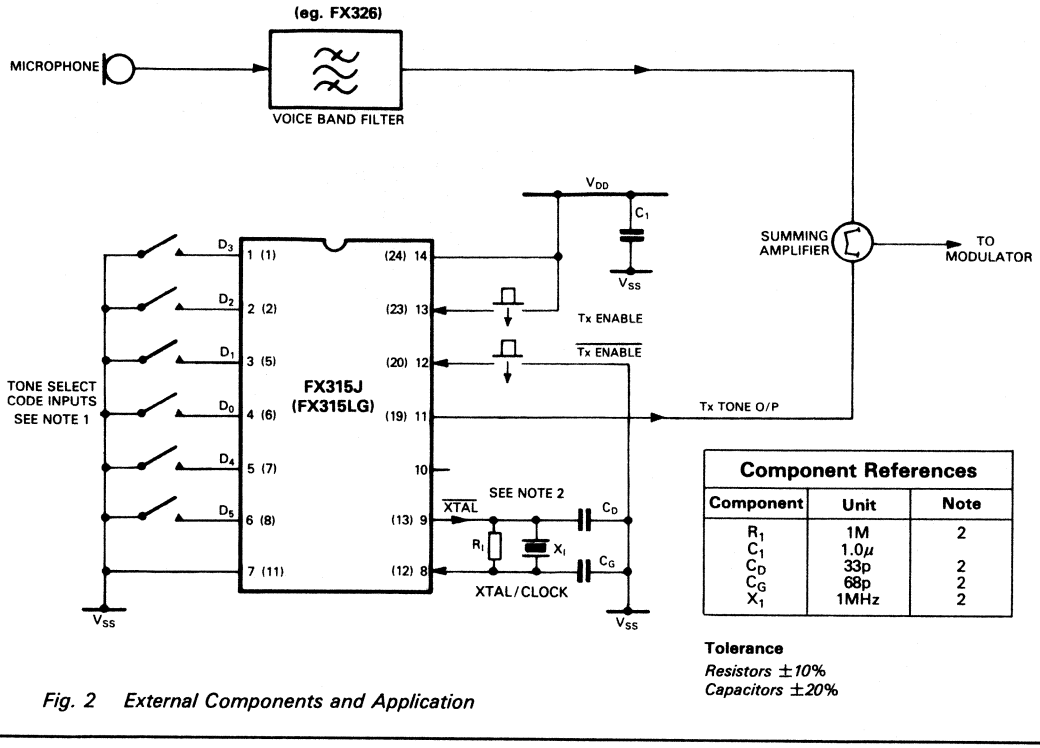
### Brief Description

The FX315 is a monolithic CMOS integrated circuit tone encoder for sub-audio tone squelch systems. The tone frequencies are derived from an input reference frequency and an on-chip inverter is provided to drive an external crystal circuit.

Tone selection is by a logic code at the $D_0 - D_5$ programming inputs and two control inputs allow either a logic '1' or logic '0' to enable the device. A low distortion sinewave is generated at the Tx Tone Output when the FX315 is activated. The emitter follower output stage can source 1mW directly into a 600 Ohm load.

| Pin Number | | Function |
|---|---|---|
| DIL FX315J | Quad FX315LG | |
| 1 | 1 | $D_3$ |
| 2 | 2 | $D_2$ |
| 3 | 5 | $D_1$ — **Data Inputs:** The logic combination at these inputs defines the CTCSS tone that the FX315 will encode (see Table 1). The input is not latched and can be changed at any time. A logic '1' will be programmed if the input is open circuit, allowing the use of SPST switches. Internal 1MΩ pull-up to $V_{DD}$ per pin. |
| 4 | 6 | $D_0$ |
| 5 | 7 | $D_4$ |
| 6 | 8 | $D_5$ |
| 7 | 11 | $V_{SS}$: Negative Supply. |
| 8 | 12 | **Xtal/Clock:** 1MHz Xtal input or externally derived clock can be injected here. Input to the on-chip inverting oscillator, at no time should supply voltage be applied without the input clock signal. |
| 9 | 13 | **$\overline{\text{XTAL}}$:** 1MHz Xtal output. Inverting output of the on-chip inverting oscillator. When used as a Xtal oscillator, track lengths and loading on the two oscillator pins should be minimised. |
| 10 | | **Internally wired.** Leave open circuit. |
| 11 | 19 | **Tx TONE OUTPUT:** The output of a low impedance emitter follower tone output stage. The tone is generated about a d.c. level of $V_{DD}/2$. The pin is high impedance when not enabled. |
| 12 | 20 | **$\overline{\text{Tx ENABLE}}$:** A logic '0' input at this pin will force the device into tone encoding. Internal 1MΩ pull-up to $V_{DD}$. |
| 13 | 23 | **Tx ENABLE:** A logic '1' input at this pin will force the device into tone encoding. Internal 1MΩ pull-down to $V_{SS}$. |
| 14 | 24 | $V_{DD}$: Positive 5 volt supply. |
| | 3.4.9.10 14.15.16. 17.18.21 22 | Not connected. |

## Application Notes




| Component References | | |
|---|---|---|
| **Component** | **Unit** | **Note** |
| $R_1$ | 1M | 2 |
| $C_1$ | 1.0$\mu$ | |
| $C_D$ | 33p | 2 |
| $C_G$ | 68p | 2 |
| $X_1$ | 1MHz | 2 |

**Tolerance**
*Resistors* ±*10%*
*Capacitors* ±*20%*

*Fig. 2 External Components and Application*

**Notes:**

1. The FX315 'Tone Select' code inputs, left open circuit will be programmed with Logic '1's by the internal 1MΩ pull-up resistors.
This enables the use of simple devices when coding. Wire links can be fitted for permanent code, SPST switches will allow code changes in the field. Using preformed coded 7-pin inserts will enable the user to communicate in predetermined groups.

2. $X_1$ is a parallel resonant crystal. A reference frequency of 1 MHz± 0.19% is required to maintain a tone accuracy within ±0.5%.
Crystal circuitry shown in Figure 2 is in accordance with CML Application Note D/XT/1 April 1986. Where two or more circuits are required to use a single oscillator (eg. repeater applications), the signal at $\overline{\text{XTAL}}$ can be used to drive one additional Xtal/Clock input. Any further circuits can be driven from the buffered $\overline{\text{XTAL}}$ output of the second device.

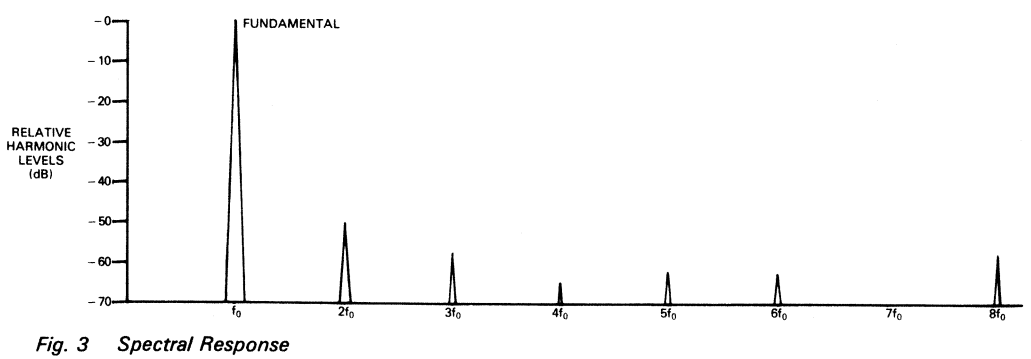



*Fig. 3 Spectral Response*

## Application Notes

| Nominal Freq. (Hz) | FX315 Freq. $f_0$ (Hz) | $\Delta f_0$ (%) | Programmable Inputs $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | Nominal Freq. (Hz) | FX315 Freq. $f_0$ (Hz) | $\Delta f_0$ (%) | Programmable Inputs $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 67.0 | 67.06 | +0.10 | 1 | 1 | 1 | 1 | 1 | 1 | 131.8 | 131.67 | -0.10 | 1 | 0 | 0 | 1 | 0 | 0 |
| 69.3 | 69.37 | +0.10 | 1 | 0 | 0 | 1 | 1 | 1 | 136.5 | 136.69 | +0.14 | 0 | 0 | 0 | 1 | 1 | 0 |
| 71.9 | 71.84 | -0.08 | 1 | 1 | 1 | 1 | 1 | 0 | 141.3 | 141.48 | +0.13 | 0 | 0 | 0 | 1 | 0 | 0 |
| 74.4 | 74.33 | -0.10 | 0 | 1 | 1 | 1 | 1 | 1 | 146.2 | 145.96 | -0.16 | 1 | 1 | 1 | 0 | 1 | 0 |
| 77.0 | 76.99 | -0.02 | 1 | 1 | 1 | 1 | 0 | 0 | 151.4 | 151.45 | +0.03 | 1 | 1 | 1 | 0 | 0 | 0 |
| 79.7 | 79.65 | -0.06 | 1 | 0 | 1 | 1 | 1 | 1 | 156.7 | 156.59 | -0.07 | 0 | 1 | 1 | 0 | 1 | 0 |
| 82.5 | 82.50 | 0.0 | 0 | 1 | 1 | 1 | 1 | 0 | 162.2 | 162.10 | -0.06 | 0 | 1 | 1 | 0 | 0 | 0 |
| 85.4 | 85.34 | -0.07 | 0 | 0 | 1 | 1 | 1 | 1 | 167.9 | 168.01 | +0.07 | 1 | 0 | 1 | 0 | 1 | 0 |
| 88.5 | 88.62 | +0.14 | 0 | 1 | 1 | 1 | 0 | 0 | 173.8 | 173.43 | -0.21 | 1 | 0 | 1 | 0 | 0 | 0 |
| 91.5 | 91.38 | -0.13 | 1 | 1 | 0 | 1 | 1 | 1 | 179.9 | 180.21 | +0.17 | 0 | 0 | 1 | 0 | 1 | 0 |
| 94.8 | 94.88 | +0.08 | 1 | 0 | 1 | 1 | 1 | 0 | 186.2 | 186.46 | +0.14 | 0 | 0 | 1 | 0 | 0 | 0 |
| 97.4 | 97.46 | +0.06 | 0 | 1 | 0 | 1 | 1 | 1 | 192.8 | 193.16 | +0.19 | 1 | 1 | 0 | 0 | 1 | 0 |
| 100.0 | 99.87 | -0.13 | 1 | 0 | 1 | 1 | 0 | 0 | 203.5 | 202.88 | -0.31 | 1 | 1 | 0 | 0 | 0 | 0 |
| 103.5 | 103.39 | -0.11 | 0 | 0 | 1 | 1 | 1 | 0 | 206.5 | 206.78 | +0.14 | 0 | 0 | 0 | 1 | 1 | 1 |
| 107.2 | 107.17 | -0.03 | 0 | 0 | 1 | 1 | 0 | 0 | 210.7 | 210.84 | +0.07 | 0 | 1 | 0 | 0 | 1 | 0 |
| 110.9 | 110.85 | -0.04 | 1 | 1 | 0 | 1 | 1 | 0 | 218.1 | 217.96 | -0.07 | 0 | 1 | 0 | 0 | 0 | 0 |
| 114.8 | 114.80 | 0.0 | 1 | 1 | 0 | 1 | 0 | 0 | 225.7 | 225.58 | -0.05 | 1 | 0 | 0 | 0 | 1 | 0 |
| 118.8 | 118.60 | -0.17 | 0 | 1 | 0 | 1 | 1 | 0 | 233.6 | 233.75 | +0.07 | 1 | 0 | 0 | 0 | 0 | 0 |
| 123.0 | 123.12 | +0.10 | 0 | 1 | 0 | 1 | 0 | 0 | 241.8 | 242.54 | +0.31 | 0 | 0 | 0 | 0 | 1 | 0 |
| 127.3 | 127.50 | +0.16 | 1 | 0 | 0 | 1 | 1 | 0 | 250.3 | 250.06 | +0.10 | 0 | 0 | 0 | 0 | 0 | 0 |
| Test | 4032 | 0.0 | 1 | 1 | 0 | 0 | 1 | 1 | | | | | | | | | |

*Table 1 Code Programming* *Logic "1" = $V_{DD}$* *Logic "0" = $V_{SS}$* *Xtal Frequency ($X_1$) = 1.0MHz*

## General Notes

The FX315 is dedicated to continuous tone controlled squelch systems (CTCSS) in radio applications. It can however, be used wherever encoding of low frequency tones is required such as intercoms, door entry systems or industrial applications.

The performance of a CTCSS system can be degraded if speech frequencies in the signalling spectrum are not removed prior to transmission. This can be achieved by filtering the microphone signals to attenuate frequencies below 250Hz. Figure 2 illustrates adding the Tx Tone Output to the filtered microphone signals prior to modulation.

The FX315 requires a clock of 1MHz which is internally converted to logic level square waves. Consideration should therefore be given to possible interference problems with RF or IF circuitry caused by 1MHz or its harmonics (Fig. 3). A decoupling capacitor ($C_1$) should be used to smooth the supply rails. This will reduce the level of superimposed noise on the supply caused by internal switching transients (particularly at 1MHz and $f_0$).

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3 to ($V_{DD}$ + 0.3V) |
| Output sink/source current (supply pins) | | ±30mA |
| (other pins) | | ±20mA |
| Total device dissipation @ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX315J** | −30°C to +85°C (Ceramic) |
| | **FX315LG** | −30°C to +70°C (Plastic) |
| Storage temperature range: | **FX315J** | −55°C to +125°C (Ceramic) |
| | **FX315LG** | −40°C to +85°C (Plastic) |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

$V_{DD}$ = 5V, $T_{amb}$ = 25°C, $\phi$ = 1MHz . $R_L$ = 600Ω, $C_L$ = 15pF.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current (Enabled) | | — | 1.5 | — | mA |
| Logic Input Impedance | | — | 500 | — | kΩ |
| Xtal Input Impedance | | — | 10 | — | MΩ |
| Inputs Logic '1' | 1 | 3.5 | — | — | V |
| Inputs Logic '0' | 1 | — | — | 1.5 | V |
| **Dynamic Values:** | | | | | |
| Tone Output Level | | −3 | 0 | — | dBm |
| Tone Accuracy ($f_0$ error) | | — | — | ±0.31 | %$f_0$ |
| Total Harmonic Distortion | 2 | — | 2 | 5 | % |
| Tone Output Load Current | | — | — | 5 | mA |
| Tone Output Rise Time ($t_R$) | | — | 1 | — | ms |
| Tone Level Variations | | — | 0.1 | — | dB |
| Output Harmonic Attenuation | | −49 | — | — | dB |

**Notes:** *1. Relate to all inputs.*

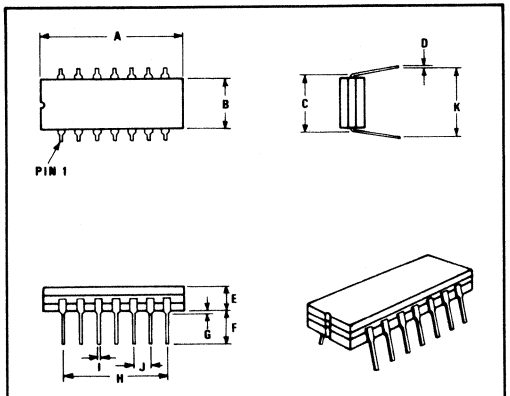
*2. T.H.D. measurements taken in the 0 − 6kHz bandwidth.*

*3. Output Loading: Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200 pF are unavoidable a resistor of typically <100Ω put in series with the load should minimise this effect.*

## Package Outlines

The FX315J, the cerdip package, is illustrated in figure 4. The 'LG' version is shown in figure 5. The 'LG' package is supplied in a conductive tray for handling convenience. To allow complete identification the FX315LG package has an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 4* **FX315J** *DIL Package*



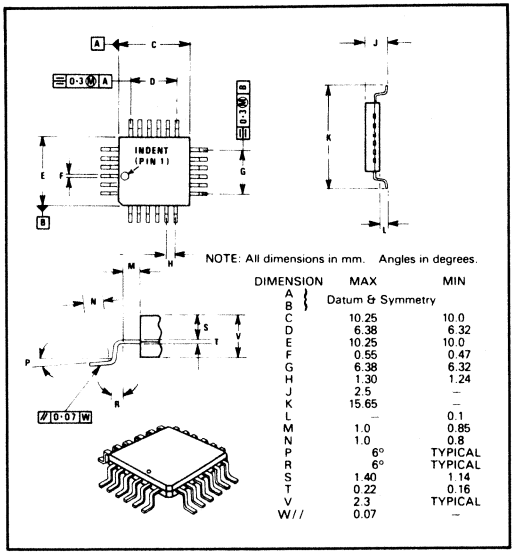

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.45 | 19.15 |
| B | 6.38 | 6.22 |
| C | 8.00 | 7.75 |
| D | 0.25 } TYPICAL | |
| E | 4.10 } | |
| F | 4.30 | 4.10 |
| G | 1.40 | |
| H | 15.24 } TYPICAL | |
| I | 0.46 } | |
| J | 2.54 | |
| K | 10.67 | 9.65 |

## Handling Precautions

The FX315J/LG is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

*Fig. 5* **FX315LG** *Quad Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A } | Datum & Symmetry | |
| B } | | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W// | 0.07 | – |

## Ordering Information

**FX315J** **14-pin cerdip DIL.**

**FX315LG** **24-pin quad plastic encapsulated, bent and cropped.**

# CML Semiconductor Products

PRODUCT INFORMATION

# FX365

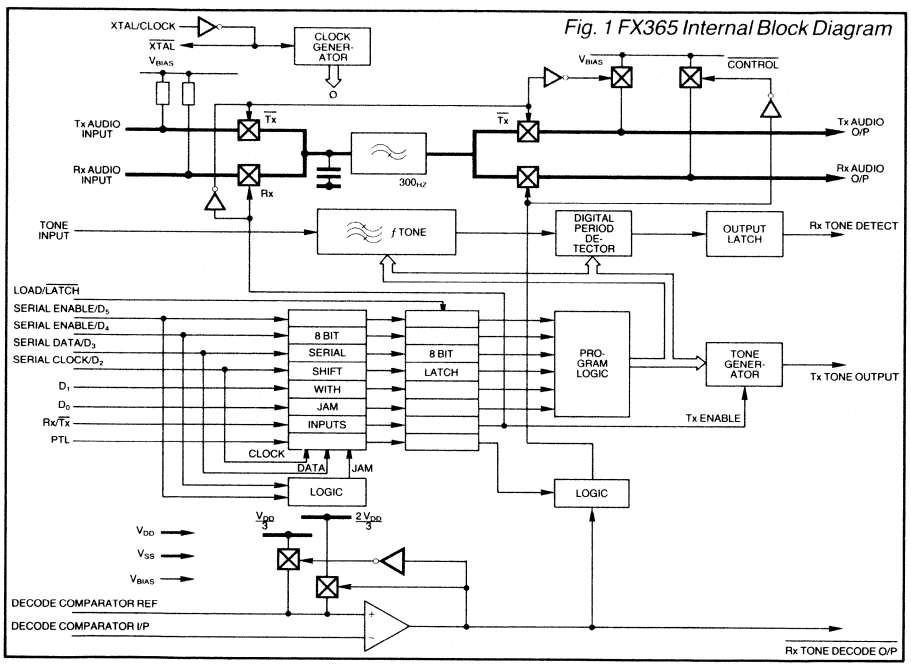
## μP Compatible CTCSS Encoder/Decoder

Publication D/365/5 October 1991
Provisional Issue

### Features/Applications

- CTCSS Encoder/Decoder
- Serial/Parallel μP Interface
- 38 Programmable Tones
- Separate Rx/Tx Audio Paths
- HP Filter for Rejection of CTCSS Tone and Prefiltering of Tx Audio
- Low Falsing with Noise Inputs
- Tx Phase Reversal Facility
- 'No Tone' Facility
- HF Filters on Inputs
- On-Chip Analogue Switching
- Low Power 5V CMOS
- Xtal Controlled Tones
- Meets EIA RS220(B)/MPT1306
- Choice of DIL or Surface Mount Package Styles

*Fig. 1 FX365 Internal Block Diagram*




**FX365**

### Brief Description

The FX365 is a CMOS LSI device intended for use as a CTCSS Encoder/Decoder in radio communications systems. Designed specifically for microprocessor controlled multichannel equipment, the FX365 incorporates a number of advanced features which improve performance and facilitate system design. The tone frequency to be encoded or decoded, the transmit enable command and the monitor receiver audio command may all be entered via an 8-bit port and a load/latch pulse. Alternatively, the programming information may be entered via a serial data port and a data clock. The device has a new tone decoder design which reduces false decode outputs due to noise to insignificant levels.

The tone encoder has a phase reversal facility, the tone decoder and speech path high pass filter have separate inputs and both are protected against the effects of incident RF voltages. The speech path filter has low passband ripple, low output noise and a cut-off frequency of 300Hz regardless of the programmed CTCSS tone.

Separate Rx and Tx audio paths are provided for prefiltering of Tx audio and rejection of the CTCSS tone in Rx mode.

The FX365 uses a 1MHz crystal reference oscillator, a single 5-volt supply; and the choice of DIL or SMT packages makes it suitable for fixed or portable equipment.

| Pin Number | | | Function |
|---|---|---|---|
| DIL FX365J | Quad Plastic FX365LG | PLCC FX365LS | |
| 1 | 1 | 1 | **$V_{DD}$:** Positive Supply. |
| 2 | 2 | 2 | **Xtal/Clock I/P:** Input to on-chip inverter used with a 1MHz Xtal or external clock source. |
| 3 | 3 | 3 | **$\overline{\text{Xtal}}$:** Output of on-chip inverter (clock output). |
| 4 | 4 | 4 | **Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch Rx/$\overline{\text{T}}$x, PTL, $D_0$–$D_5$. This pin is internally pulled to $V_{DD}$. A logic '1' applied to this input puts the 8 latches in 'transparent' mode. A logic '0' applied to this input puts the 8 latches in the 'latched' mode. In parallel mode data is loaded and latched by a logic 1→ 0 transition (see Fig. 4). In serial mode data is loaded and latched by a 0→1→0 strobe pulse on this pin (see Fig. 5). |
| 5 | 5 | 5 | **$D_5$/Serial Enable 1:** Data input $D_5$ (in parallel mode). A logic '1' applied to this input together with a logic '0' applied to $D_4$/SERIAL ENABLE 2 will put the device in 'Serial mode' (see Fig. 5). This pin internally pulled to $V_{DD}$. |
| 6 | 6 | 6 | **$D_4$/Serial Enable 2:** Data input $D_4$ (in parallel mode). A logic '0' applied to this input together with a logic '1' on pin 5 will place the device in 'serial mode' (see Fig. 5). This pin internally pulled to $V_{DD}$. |
| 7 | 7 | 7 | **$D_3$/Serial Data:** Data input $D_3$ (in parallel mode). In serial mode this pin becomes the serial data input for $D_5$–$D_0$, Rx/$\overline{\text{T}}$x, PTL (see Fig. 5). $D_5$ is clocked first and PTL last. This pin internally pulled to $V_{DD}$. |
| 8 | 8 | 8 | **$D_2$/Serial Clock:** Data $D_2$ (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 5). This pin is internally pulled to $V_{DD}$. |
| 9 | 9 | 9 | **$D_1$:** Data $D_1$ (in parallel mode). This pin internally pulled to $V_{DD}$. |
| 10 | 10 | 10 | **$D_0$:** Data $D_0$ (in parallel mode). This pin internally pulled to $V_{DD}$. |
| 11 | 11 | 11 | **$V_{SS}$:** Negative supply. |
| 12 | 12 | 12 | **Decode Comparator Ref (I/P):** This pin is internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1MΩ resistors depending on the logical state of the TONE DECODE O/P pin. TONE DEC O/P = 1 will bias this input to $2V_{DD}/3$, a logic '0' will bias this input to $V_{DD}/3$. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions. |
| 13 | 13 | 13 | **$\overline{\text{Rx Tone Decoder (O/P)}}$:** Gated output of the decode comparator. This output is used to gate the Rx Audio path. A logic '0' on this pin indicates a successful decode and indicates that the 'decode comparator input' pin is more positive than the 'decode comparator ref' input (see Table 2). |

| Pin Number | | | Function |
|---|---|---|---|
| DIL FX365J | Quad Plastic FX365LG | PLCC FX365LS | |
| 14 | 14 | 14 | **Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is to be connected to the Rx TONE DETECT pin via an external integrator (see Figs. 2 & 3). |
| 15 | 15 | 15 | **Rx Tone Detect (O/P):** In Rx mode this pin will go to logic '1' during a successful decode (see Table 2). This pin is normally connected to the Decode Comparator input via the external integrator circuitry, as shown in Figs. 2 & 3. |
| 16 | 16 | 16 | **Tx Tone O/P:** A low impedance emitter follower stage for sourcing the CTCSS sinewave under the control of the Rx/$\overline{\text{Tx}}$ pin. This O/P when not transmitting a tone may be biased to $\frac{V_{DD}}{2} - 0.7V$ or O/C (see Table 2). |
| 17 | 17 | 17 | **Rx/$\overline{\text{Tx}}$:** This input (in parallel mode) selects Rx or Tx modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to $V_{DD}$ via a 1MΩ resistor. |
| 18 | 18 | 18 | **PTL:** In parallel Rx mode this pin operates as a 'press to listen' function by enabling the Rx audio path thus overriding the tone squelch function. In parallel Tx mode this pin reverses the phase of the transmitted CTCSS tone (squelch tail elimination). In serial mode this function is serially loaded (see Fig. 3). The phase reversal function should be applied by timing circuit to ensure correct system operation. |
| 19 | 19 | 19 | **Rx Audio Out:** This is the high pass filtered "Receive" audio output pin. This pin outputs audio when $\overline{\text{Rx TONE DECODE}}=0$, or PTL=1 or NOTONE is programmed (see Table 2). In Tx mode this pin is biased to $\frac{V_{DD}}{2}$. |
| 20 | 20 | 20 | **Tx Audio Out:** This is the high pass filtered "Transmit" audio output pin. In Tx mode this pin outputs audio present at the 'Tx AUDIO INPUT' pin. In Rx mode this pin is biased to $\frac{V_{DD}}{2}$. |
| 21 | 21 | 21 | **Bias:** This pin is the output of an internally generated $\frac{V_{DD}}{2}$ bias level and would normally be externally decoupled to $V_{SS}$ via $C_6$. |
| 22 | 22 | 22 | **Tx Audio I/P:** This is the Tx Audio input pin. In Tx mode audio may be prefiltered, using the Tx audio path, thus helping to avoid talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. The Tx audio path may also be used to prefilter speech when using scramblers which introduce noise in the low frequency band. This pin is internally biased to $\frac{V_{DD}}{2}$. |
| 23 | 23 | 23 | **Rx Audio Input:** This is the input to the audio high pass filter in Rx mode. This pin is internally biased to $\frac{V_{DD}}{2}$. |
| 24 | 24 | 24 | **Tone Input:** This is the input to the CTCSS tone detector and is internally biased to $\frac{V_{DD}}{2}$. |

## External Component Connections

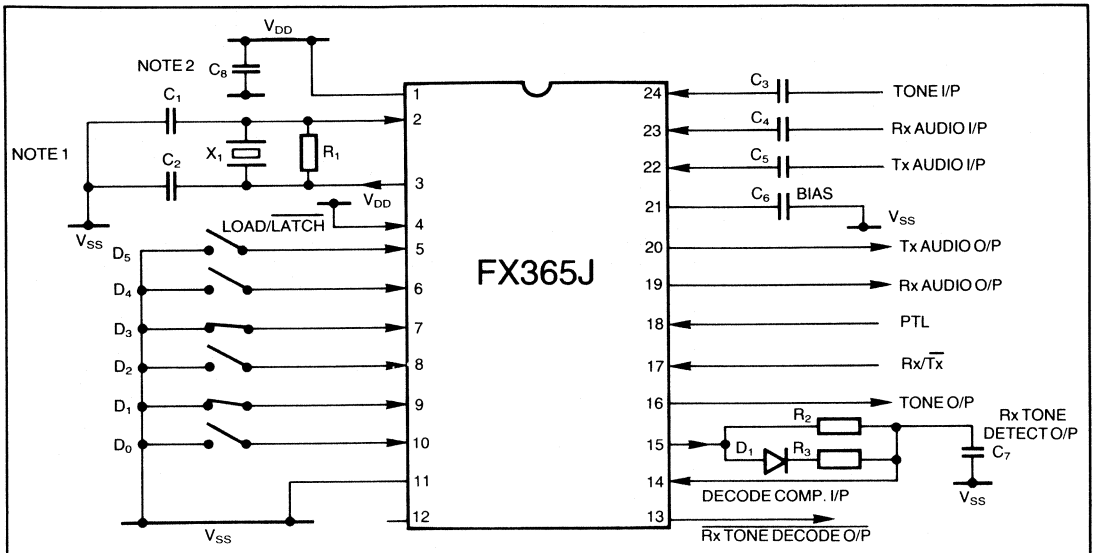



*Fig. 2 Parallel Wired Application*

| Component | Unit Value | Note |
|---|---|---|
| $R_1$ | 1M | 1 |
| $R_2$ | 820k | |
| $R_3$ | 330k | |
| $C_1$ | 68p | 1 |
| $C_2$ | 33p | 1 |
| $C_3$ | 0.1$\mu$ | |
| $C_4$ | 0.1$\mu$ | |

| Component | Unit Value | Note |
|---|---|---|
| $C_5$ | 0.1$\mu$ | |
| $C_6$ | 1.0$\mu$ | |
| $C_7$ | 0.1$\mu$ | |
| $C_8$ | 1.0$\mu$ | 2 |
| $D_1$ | small signal | |
| $X_1$ | 1MHz | 1 |

**NOTES:**

*Tolerances: Resistors ±10%. Capacitors ±20%*

*1. Xtal circuitry shown is in accordance with CML. Application Note D/XT/1 April 1986.*

*2. $C_8$ is used for power supply decoupling. Depending on application further filtering may be required.*

**Table 1 Component References and Values**

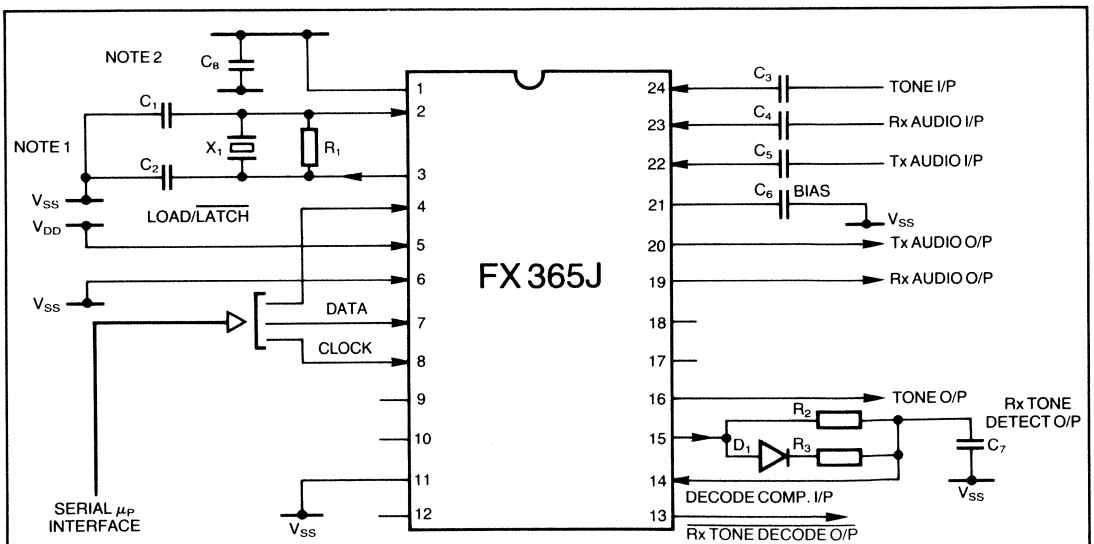



*Fig. 3 Serial Microprocessor Application*

## Truth Tables

| Input Pin – Condition | | | | Output Pin – Condition | | Result/Function | | | | | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_0$–$D_5$ | Rx/$\overline{Tx}$ | PTL | Decode Comp Input | Rx Tone Detect | $\overline{Tone}$ $\overline{Decode}$ | Tone Transmitter Enabled | Tx Tone Phase Reversed | Tx Audio Path Enabled | Tone Decoder Enabled | Rx Audio Path Enabled | |
| Tone | 0 | 0 | x | 0 | 1 | Yes | No | Yes | No | No (bias) | 1a |
| Tone | 0 | 1 | x | 0 | 1 | Yes | Yes | Yes | No | No (bias) | 1b |
| No tone | 0 | x | x | 0 | 1 | No (bias) | x | Yes | No | No (bias) | 2 |
| Tone | 1 | 0 | 0 | 0 | 1 | No (o/c) | x | No | Yes | No (bias) | 3a |
| Tone | 1 | 1 | 0 | 0 | 1 | No (o/c) | x | No | Yes | Yes | 3b |
| Tone | 1 | x | 1 | 1 | 0 | No (o/c) | x | No | Yes | Yes | 4 |
| No tone | 1 | x | x | x | 0 | No (o/c) | x | No | Yes | Yes | 5 |

**Notes:**

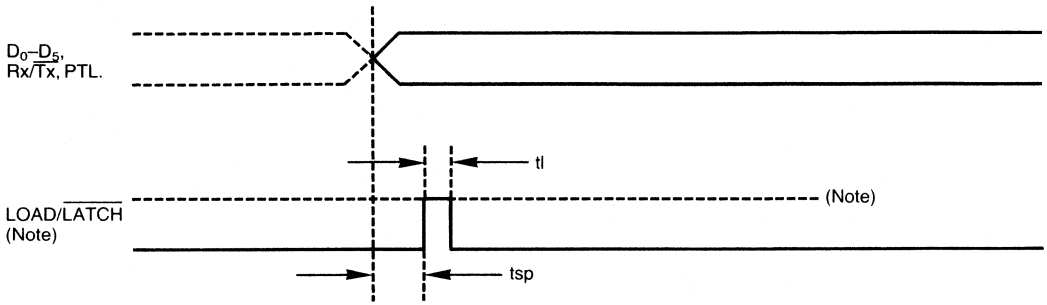
*1a. Normal tone transmit condition.*
*1b. Tone transmit with phase reversed.*
*2. 'NOTONE' programmed in Tx mode, tone transmit O/P set to $V_{DD}/2 - 0.7V$. Tx audio path enabled.*
*3a. Normal decode standby.*
*3b. Normal decode standby with PTL used to enable audio.*
*4. Normal 'decode of correct CTCSS tone' condition, PTL has no effect.*
*5. 'NOTONE' programmed in Rx mode, tone transmit O/P (o/c), Rx audio path enabled.*

**Table 2 Truth table defining combinations of input/output conditions.**

| Nominal Freq. Hz | FX365 Frequency | $\triangle f_o$% | Programme Inputs $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ |
|---|---|---|---|---|---|---|---|---|
| 67.0 | 67.05 | +.07 | 1 | 1 | 1 | 1 | 1 | 1 |
| 71.9 | 71.90 | 0.0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 74.4 | 74.35 | −.07 | 0 | 1 | 1 | 1 | 1 | 1 |
| 77.0 | 76.96 | −.05 | 1 | 1 | 1 | 1 | 0 | 0 |
| 79.7 | 79.77 | +.09 | 1 | 0 | 1 | 1 | 1 | 1 |
| 82.5 | 82.59 | +.10 | 0 | 1 | 1 | 1 | 1 | 0 |
| 85.4 | 85.38 | −.02 | 0 | 0 | 1 | 1 | 1 | 1 |
| 88.5 | 88.61 | +.13 | 0 | 1 | 1 | 1 | 0 | 0 |
| 91.5 | 91.58 | +.09 | 1 | 1 | 0 | 1 | 1 | 1 |
| 94.8 | 94.76 | −.04 | 1 | 0 | 1 | 1 | 1 | 0 |
| 97.4 | 97.29 | −0.11 | 0 | 1 | 0 | 1 | 1 | 1 |
| 100.0 | 99.96 | −.04 | 1 | 0 | 1 | 1 | 0 | 0 |
| 103.5 | 103.43 | −.07 | 0 | 0 | 1 | 1 | 1 | 0 |
| 107.2 | 107.15 | −.05 | 0 | 0 | 1 | 1 | 0 | 0 |
| 110.9 | 110.77 | −.12 | 1 | 1 | 0 | 1 | 1 | 0 |
| 114.8 | 114.64 | −.14 | 1 | 1 | 0 | 1 | 0 | 0 |
| 118.8 | 118.80 | 0.0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 123.0 | 122.80 | −.17 | 0 | 1 | 0 | 1 | 0 | 0 |
| 127.3 | 127.08 | −.17 | 1 | 0 | 0 | 1 | 1 | 0 |
| 131.8 | 131.67 | −.10 | 1 | 0 | 0 | 1 | 0 | 0 |
| 136.5 | 136.61 | +.08 | 0 | 0 | 0 | 1 | 1 | 0 |
| 141.3 | 141.32 | +.02 | 0 | 0 | 0 | 1 | 0 | 0 |
| 146.2 | 146.37 | +.12 | 1 | 1 | 1 | 0 | 1 | 0 |
| 151.4 | 151.09 | −.20 | 1 | 1 | 1 | 0 | 0 | 0 |
| 156.7 | 156.88 | +.11 | 0 | 1 | 1 | 0 | 1 | 0 |
| 162.2 | 162.31 | +.07 | 0 | 1 | 1 | 0 | 0 | 0 |
| 167.9 | 168.14 | +.14 | 1 | 0 | 1 | 0 | 1 | 0 |
| 173.8 | 173.48 | −.19 | 1 | 0 | 1 | 0 | 0 | 0 |
| 179.9 | 180.15 | +.14 | 0 | 0 | 1 | 0 | 1 | 0 |
| 186.2 | 186.29 | +.05 | 0 | 0 | 1 | 0 | 0 | 0 |
| 192.8 | 192.86 | +.03 | 1 | 1 | 0 | 0 | 1 | 0 |
| 203.5 | 203.65 | +.07 | 1 | 1 | 0 | 0 | 0 | 0 |
| 210.7 | 210.17 | −.25 | 0 | 1 | 0 | 0 | 1 | 0 |
| 218.1 | 218.58 | +.22 | 0 | 1 | 0 | 0 | 0 | 0 |
| 225.7 | 226.12 | +.18 | 1 | 0 | 0 | 0 | 1 | 0 |
| 233.6 | 234.19 | +.25 | 1 | 0 | 0 | 0 | 0 | 0 |
| 241.8 | 241.08 | −.30 | 0 | 0 | 0 | 0 | 1 | 0 |
| 250.3 | 250.28 | −.01 | 0 | 0 | 0 | 0 | 0 | 0 |
| Notone | Notone | — | 0 | 0 | 0 | 0 | 1 | 1 |
| Serial Input Mode | | | x | x | Clock | Data | 0 | 1 |

**Table 3 Tone programming Truth table**

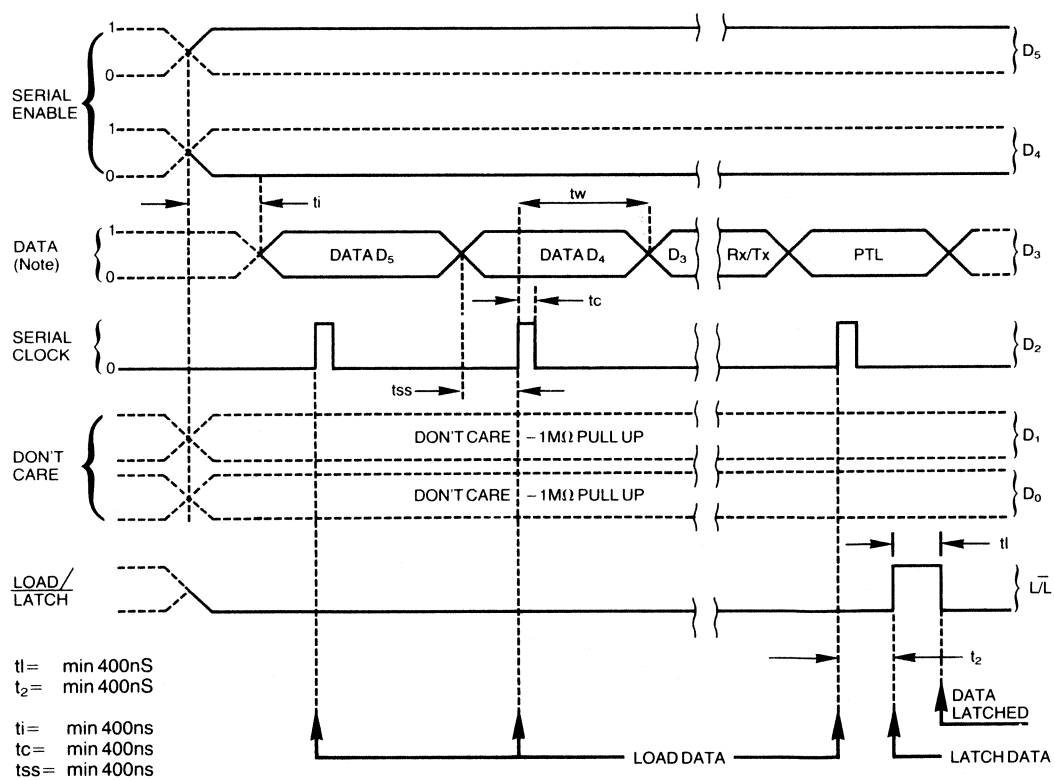
## Parallel and Serial Mode Timing Diagrams




Note: For wired, non microprocessor, applications load/latch should be connected to $V_{DD}$

tl min = 400ns
tsp min = 400ns

*Fig. 4 Parallel mode timing diagram*




tl = min 400nS
$t_2$ = min 400nS

ti = min 400ns
tc = min 400ns
tss = min 400ns
tw = min 400ns

tl = min 400ns
$t_2$ = min 400ns

Note 1: Serial bit 1 through bit 8 = $D_5$, $D_4$, $D_3$, $D_2$, $D_1$, $D_0$, Rx/Tx and PTL respectively.
Load bit 1 first, bit 8 last.

*Fig. 5 Serial mode timing diagram*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$=0V) | | −0.3V to ($V_{DD}$+0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX365J | −30°C to +85°C |
| | FX365LG/LS | −30°C to +70°C |
| Storage temperature range: | FX365J | −55°C to +125°C |
| | FX365LG/LS | −40°C to +85°C |
| Maximum device dissipation | | 800mW |
| Derating | | 10mW/°C |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. 0dB ref: = 300mVrms. Composite Signal = 0dB 1kHz Tone, −12dB Noise (band-limited 6kHz gaussian white noise), −20dB $f_0$ CTCSS Tone.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Characteristics** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | | | | |
| (Tx) | | – | 3.5 | – | mA |
| (Rx) | | – | 3.5 | – | mA |
| Tone Input Impedance | | – | 1.0 | – | MΩ |
| Audio Input Impedance | | – | 1.0 | – | MΩ |
| Audio Output Impedance | | – | 1.0 | – | kΩ |
| Digital Input Impedance | 1 | – | 1.0 | – | MΩ |
| Input Logic "1" | 1 | 3.5 | – | – | V |
| Input Logic "0" | 1 | – | – | 1.5 | V |
| Logic "1" Output 1' source = 0.1mA | 2 | 4.0 | – | – | V |
| Logic "0" Output 1' sink = 0.1 mA | 2 | – | – | 1.0 | V |
| **Dynamic Characteristics** | | | | | |
| **Decoder** | | | | | |
| Decode Input Signal Level | 3 | −20 | – | – | dB |
| Decode Response Time | 3, 6 | – | – | 250 | ms |
| De-Response Time | 3, 6 | – | – | 250 | ms |
| Decode Selectivity | 3 | ±0.5 | – | ±3.0 | %$f_0$ |
| **Encoder** | | | | | |
| Tone Output Level (relative 775mVrms) | | −3.0 | 0 | – | dB |
| Tone Frequency Accuracy ($f_0$ error) | | −0.3 | – | +0.3 | %$f_0$ |
| ***Risetime to 90% (nominal output)*** | | | | | |
| ***$f_0$ > 100Hz*** | ***4*** | ***–*** | ***55.0*** | ***–*** | ***ms*** |
| ***$f_0$ < 100Hz*** | ***4*** | ***–*** | ***70.0*** | ***–*** | ***ms*** |
| Tone Output Load Current | | – | – | 5.0 | mA |
| Total Harmonic Distortion | | – | 2.0 | 5.0 | % |
| Output Level Variation Between Tones | | – | 0.1 | – | dB |
| **Audio Filter** | | | | | |
| Total Harmonic Distortion | 5 | – | 2.0 | 5.0 | % |
| ***Output Noise Level*** | | | | | |
| ***Input a.c. Short Cct, Audio Switch Enabled*** | | ***–*** | ***–49.0*** | ***–45.0*** | ***dB*** |
| Cut-Off frequency | | – | 300 | – | Hz |
| Bandpass Ripple (300Hz –3000Hz) | 5 | −1.0 | – | +1.0 | dB |
| Stopband Attenuation <250Hz | 5 | 36.0 | 40.0 | – | dB |
| Passband Gain (ref. 1kHz) | | – | 0 | – | dB |
| **Audio Switch** | | | | | |
| Isolation | 5 | – | 60.0 | – | dB |
| **Serial/Parallel Inputs** | | | | | |
| Parallel Set-Up Time ($t_{SP}$) | 7 | 400 | – | – | ns |
| Load/Latch Pulse Width ($t_L$) | 7 | 400 | – | – | ns |
| Serial Clock Pulse Width ($t_C$) | 7 | 400 | – | – | ns |
| Serial Set-Up Time ($t_{SS}$) | 7 | 400 | – | – | ns |
| Serial Clock Frequency | 7 | – | 1.0 | – | MHz |

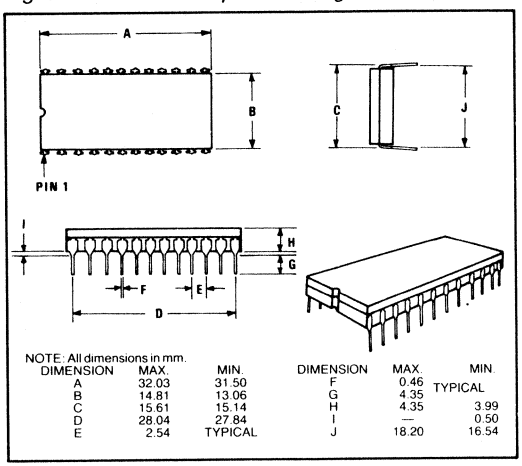
**Notes**

1. Refers to Rx/$\overline{\text{Tx}}$, PTL, Decode Comparator Input, $D_0$, $D_1$, $D_2$, $D_3$, $D_4$, $D_5$.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programme tone and RL = 600Ω. CL = 15pF. Includes response to a phase reversal instruction.
5. 1kHz reference = 0dB.
6. $f_0$ > 100Hz, (for 100Hz >$f_0$>67Hz: t = (100/$f_0$ Hz) x 250ms).
7. See Figures 4 and 5.

## Packaging Outlines

The FX365J, the cerdip package, is illustrated in figure 6. The 'LG' version is shown in figure 7, and the 'LS' version in figure 8. To allow complete identification, the FX365 LG and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 6* **FX365J** *Cerdip DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. | DIMENSION | MAX. | MIN. |
|---|---|---|---|---|---|
| A | 32.03 | 31.50 | F | 0.46 | TYPICAL |
| B | 14.81 | 13.06 | G | 4.35 | |
| C | 15.61 | 15.14 | H | 4.35 | 3.99 |
| D | 28.04 | 27.84 | I | — | 0.50 |
| E | 2.54 | TYPICAL | J | 18.20 | 16.54 |

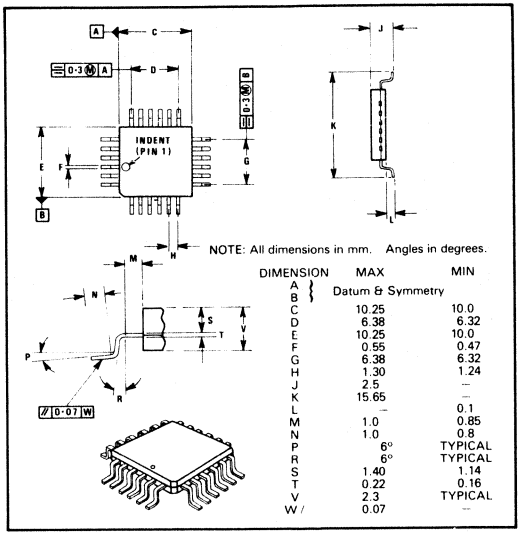
## Ordering Information

| | |
|---|---|
| **FX365J** | **24-pin cerdip DIL** |
| **FX365LG** | **24-pin quad plastic encapsulated, bent and cropped** |
| **FX365LS** | **24-lead plastic leaded chip carrier** |

## Handling Precautions

The FX365J/LG/LS is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

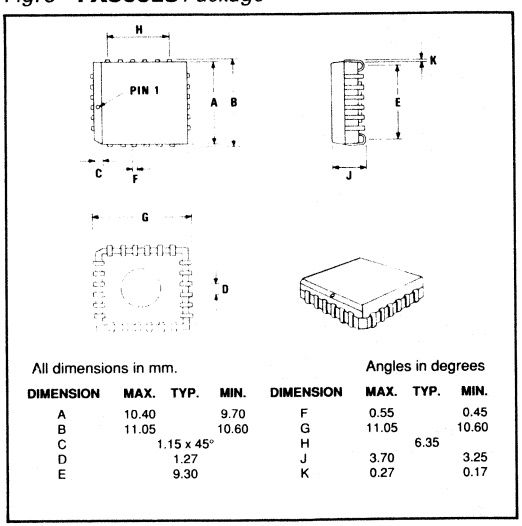
*Fig. 7* **FX365LG** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | — |
| K | 15.65 | — |
| L | — | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | — |

*Fig. 8* **FX365LS** *Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.40 | | 9.70 | F | 0.55 | | 0.45 |
| B | 11.05 | | 10.60 | G | 11.05 | | 10.60 |
| C | | 1.15 x 45° | | H | | 6.35 | |
| D | | 1.27 | | J | 3.70 | | 3.25 |
| E | | 9.30 | | K | 0.27 | | 0.17 |

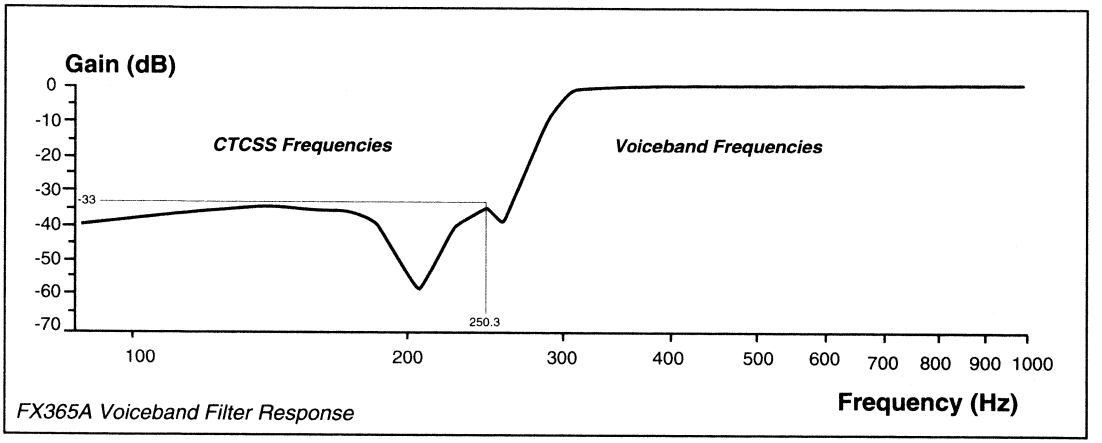
# CML Semiconductor Products
PRODUCT INFORMATION

# FX365A CTCSS Encoder/Decoder

Publication No. D/365A/2 February 1993
Advance Information

## Features

- **Improved Audio and Noise Performance**
- **39 Programmable Sub-Audio Tones + NOTONE**
- **Sub-Audio Frequency Range 67.0Hz to 250.3Hz**
- **Pin Compatible with FX365 Microcircuits**
- **High Voiceband/CTCSS Isolation**




*FX365A Voiceband Filter Response*

## Brief Description

The FX365A is a half-duplex µProcessor controlled CTCSS Encoder and Decoder with integral voice-band filtering.

This device which is pin compatible with standard FX365 microcircuits is also available in a 24-pin plastic Small Outline Integrated Circuit (S.O.I.C); the FX365A DW. The FX365A demonstrates improved voice-band noise performance.

The FX365A has the capability of encoding and decoding 39 separate sub-audio tones, 38 of which are detailed in the current FX365 Data Sheet, plus an additional tone of 69.3Hz.

This Data Sheet, which details the differences between the **FX365A** and the FX365 microcircuits, should be used with the current **FX365** Data Sheet.

### Programmable Sub-Audio Rx and Tx Frequencies (Hz)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 67.0 | **69.3** | 71.9 | 74.4 | 77.0 | 79.7 | 82.5 | 85.4 |
| 88.5 | 91.5 | 94.8 | 97.4 | 100.0 | 103.5 | 107.2 | 110.9 |
| 114.8 | 118.8 | 123.0 | 127.3 | 131.8 | 136.5 | 141.3 | 146.2 |
| 151.4 | 156.7 | 162.2 | 167.9 | 173.8 | 179.9 | 186.2 | 192.8 |
| 203.5 | 210.7 | 218.1 | 225.7 | 233.6 | 241.8 | 250.3 | NOTONE |

*FX365A Tx and Rx Sub-Audio Frequencies*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX365A J** | -40°C to +85°C (cerdip) |
| | **FX365A DW/LG/LS** | -40°C to +85°C (plastic) |
| Storage temperature range: | **FX365A J** | -55°C to +125°C (cerdip) |
| | **FX365A DW/LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 1.0MHz. Audio level 0dB ref: = 300mV rms
Composite Signal Content = *1.0kHz tone at 0dB, Noise at -12dB (gaussian white noise band-limited to 6.0kHz), Programmed CTCSS tone at -20dB.*

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current (Tx) | | – | 3.5 | – | mA |
| (Rx) | | – | 3.5 | – | mA |
| **Audio Filter** | | | | | |
| Passband Frequencies | | 300 | | 3000 | Hz |
| Passband Gain | | | | | |
| at 1.0kHz | | – | 0 | – | dB |
| w.r.t. 1.0kHz | | -2.0 | – | 0.5 | dB |
| Stopband | | | | | |
| Frequencies | | – | – | 250 | Hz |
| Attenuation | | 33.0 | 36.0 | - | dB |
| Output Noise (a.c. short circuit) | 1 | – | -54.0 | -48.0 | dB |
| SINAD | 2 | 36.0 | 40.0 | – | dB |
| Tx Output Impedance | | – | 2.0 | – | kΩ |
| Tx Output Amplitude | | – | 950 | – | mVrms |
| Spurious Emissions | | – | – | -48.0 | dB |

**Notes**

1. Measured in a 30kHz bandwidth.
2. With an input level of 308mVrms at 1.0kHz, in a 30kHz bandwidth.

## 69.3Hz Tone Generation

The additional sub-audio tone provided by the FX365A is 69.3Hz.

With reference to the FX365 Data Sheet – Table 3, the programming information is as follows:

| Nominal Freq. (Hz) | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ |
|---|---|---|---|---|---|---|
| 69.3 | 1 | 0 | 0 | 1 | 1 | 1 |

## Ordering Information

| | |
|---|---|
| **FX365A DW** | 24-pin S.O.I.C. |
| **FX365A J** | 24-pin cerdip DIL |
| **FX365A LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX365A LS** | 24-lead plastic leaded chip carrier |

# CML Semiconductor Products

PRODUCT INFORMATION

# FX375

## Private Squelch Circuit

Publication D/375/3 October 1991
Provisional Issue

### Features/Applications

- Tone Operated Private/Clear Switching
- CTCSS Tone Encode/Decode
- Separate Rx/Tx Speech Paths
- Fixed Frequency Speech Inversion
- µP Compatible Interface with Serial or Parallel Control Loading
- On-Chip Pre- and De-Emphasis Filtering in the Tx Path
- 38 Programmable Tones + 'NoTone' Facility
- Audio Path Filtering (300Hz – 3033Hz)
- Low Power 5V CMOS

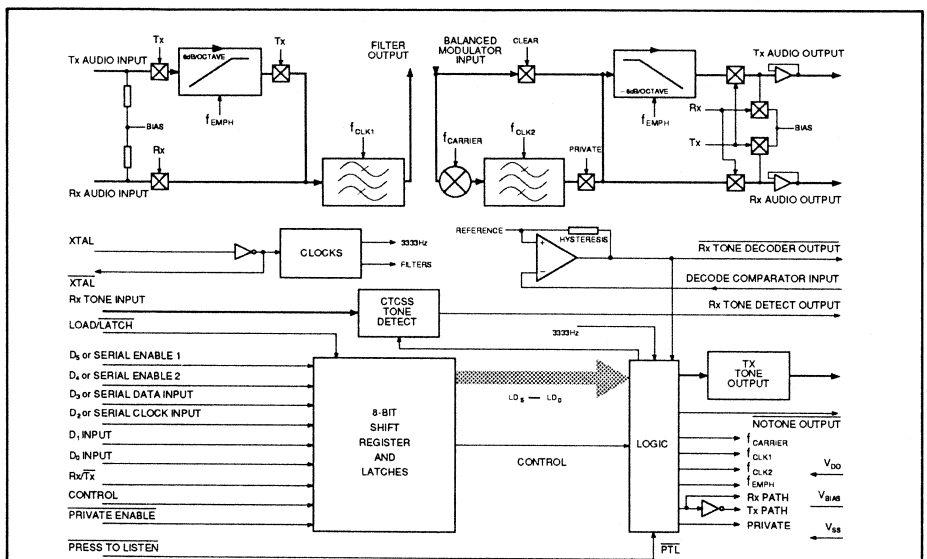



*Fig.1 Internal Block Diagram*

FX375

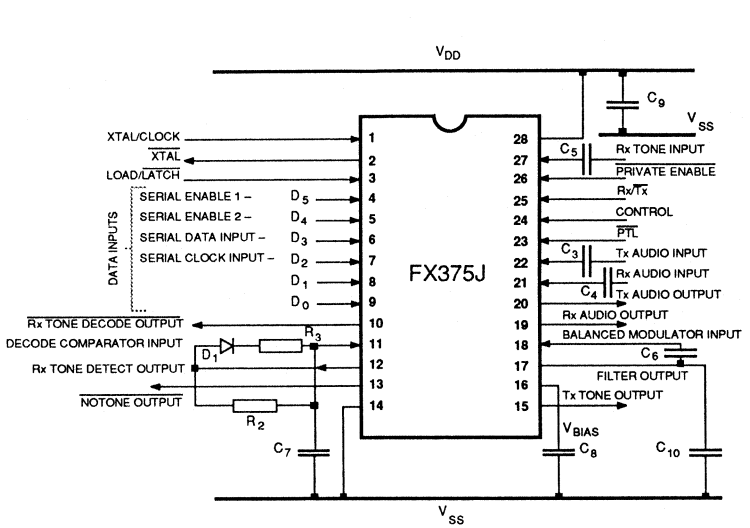
### Brief Description

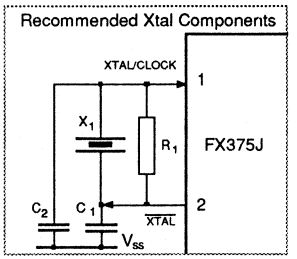
The FX375 is a Low-Power CMOS LSI microcircuit designed for Tone Operated Voice Privacy in communication systems.
This half-duplex device consists of a Fixed Frequency Voice Band Inverter interfaced with a Continuous Tone Controlled Squelch System (CTCSS) Encoder/ Decoder, whose allocated tone is used for voice privacy and audio squelch operation.
Frequency Inversion is achieved by modulating the input audio with a fixed carrier frequency to exchange the high and low frequencies of the voice band, making the resulting audio output unintelligible to receivers not equipped with a compatible system.
The on-chip CTCSS Dencoder is capable of encoding and decoding any one of 38 sub-audio tones in the range 67.0Hz to 250.3Hz, these Xtal derived tones are selected by a 6-bit binary word that can be loaded to the device in either a serial or parallel format.
The Privacy function is exclusive only to units using the same tone set, other intercepted signals remain "as transmitted."
A 'Press to Listen' facility allows monitoring of the channel prior to transmitting.
This device has separate, switched Rx and Tx voice, and tone audio paths. Voice paths use switched capacitor bandpass filters for the attenuation of sub-audio tones and unwanted modulation products.
6dB/octave pre- and de-emphasis filtering in the Tx path maintains natural sounding audio from this device when embodied in communication transceivers.
The FX375, which is available in DIL and SMT packages, can be simply controlled by switches, or interfaced to a µProcessor.
External requirements are a single 5-volt supply, an external 4.0MHz Xtal or clock input and signal coupling components.

| Pin Number | | Function |
|---|---|---|
| FX375J FX375LH | FX375LG FX375LS | |
| 1 | 2 | **Xtal/Clock:** The input to the clock oscillator inverter. An external 4MHz Xtal or clock input is to be applied at this pin. See Figure 2. |
| 2 | 3 | **$\overline{\text{Xtal}}$:** The 4MHz output of the clock oscillator inverter. See Figure 2. |
| 3 | 4 | **Load/$\overline{\text{Latch}}$:** This input regulates the operation of the eight input latches : $D_0$, $D_1$, $D_2$, $D_3$, $D_4$, $D_5$, Rx/Tx and Private Enable for both parallel and serial input load modes. Rx/Tx and Private Enable inputs can be used independently in either mode by the use of Load/Latch and Control inputs configured as shown in Table 3, the data format ($D_0 - D_5$), remains as set. This input has an internal 1MΩ pullup resistor. |
| 4 | – | **$D_5$ – (Serial Enable 1) :** The Rx/$\overline{\text{Tx}}$ tone programming and function inputs. Programmed as shown in Table 2 these inputs will select the CTCSS tone frequency and parallel or serial loading function. Notone, when set in receive, enables the Rx Audio Output and forces the Rx Tone Decode Output to a logic '0,' in transmit the Tx Tone Output is held at $V_{BIAS}$ (Notone). These inputs each have an internal 1MΩ pullup resistor. If FX375LG or LS package styles are used Pin 5 (Serial Enable 2) should be externally connected to $V_{SS}$. |
| 5 | 5 | **$D_4$ – (Serial Enable 2) :** |
| 6 | 6 | **$D_3$ – (Serial Data Input) :** |
| 7 | 7 | **$D_2$ – (Serial Clock Input) :** |
| 8 | – | **$D_1$** |
| 9 | – | **$D_0$** |
| 10 | 8 | **$\overline{\text{Rx Tone Decode Output}}$ :** The output of the decode comparator. In Rx a logic '0' indicates 'CTCSS tone decoded' above the internal reference level, or Notone programmed. This action internally enables the Rx audio path and Frequency Inversion function (when applicable) as shown in Table 1. In Tx this output is a logic '1'. |
| 11 | 9 | **Decode Comparator Input :** A logic '1' at this pin, in Rx, is compared internally with a fixed reference level, a more positive input value will produce a logic '0' at the Rx Tone Decode Output. This input should be externally connected to the Rx Tone Detect Output via external integrator components $C_7$, $R_2$, $R_3$, $D_1$ (see Figure 2). |
| 12 | 10 | **Rx Tone Detect Output :** This output, in Rx, goes to a logic '1' when a valid, programmed CTCSS tone is received at the Rx Tone Input. This input should be externally connected to the Decode Comparator Input via external integrator components $C_7$, $R_2$, $R_3$, $D_1$ (see Figure 2). |
| 13 | – | **$\overline{\text{Notone Output}}$ :** Outputs a logic '0' when a " Notone" CTCSS code has been programmed . It can be used to operate squelch circuitry under receive "Notone" conditions. |
| 14 | 11 | **$V_{SS}$ :** Negative supply rail (GND).<br>The FX375LG and LS package styles are configured as a serial-data loading device, Parallel Programing Inputs $D_0$, $D_1$ and $D_5$, and the NOTONE Output pin functions are not available. |

| Pin Number | | Function |
|---|---|---|
| FX375J FX375LH | FX375LG FX375LS | |
| 15 | 12 | **Tx Tone Output :** This is the buffered, programmed CTCSS tone sinewave output in Tx. During Rx and Notone operation this output is held at $V_{BIAS}$. See note "g," page 7 with reference to capacitive load limits of this output. |
| 16 | 13 | **$V_{BIAS}$ :** This bias pin is set internally to $V_{DD}/2$. It must be externally decoupled using a capacitor, $C_8$, of 1.0µF (minimum) to $V_{SS}$, see Figure 2. |
| 17 | 14 | **Filter Output :** The Input Audio Bandpass Filter output, this pin must be connected to the Balanced Modulator Input via a capacitor, $C_6$, and decoupled to $V_{SS}$ by $C_{10}$, see Figure 2. |
| 18 | 15 | **Balanced Modulator Input :** The input to the Balanced Modulator, this pin must be connected to the Filter Output via a capacitor, $C_6$, see Figure 2. |
| 19 | 16 | **Rx Audio Output :** Outputs the received audio from a buffered output stage and is held at $V_{BIAS}$ when in Tx. |
| 20 | 17 | **Tx Audio Output :** The output of the audio path in the Tx mode and is held at $V_{BIAS}$ when in Rx. |
| 21 | 18 | **Rx Audio Input :** The Audio input pin for the Rx mode. Input signals should be a.c. coupled via an external capacitor, $C_4$, see Figure 2. |
| 22 | 19 | **Tx Audio Input :** This is the voice input pin for the Tx mode. Signals should be a.c. coupled via an external capacitor, $C_3$, see Figure 2. |
| 23 | 20 | **$\overline{\text{PTL}}$ :** The "Press To Listen" function input, in the receive mode a logic '0' enables the Rx Audio Output directly, overriding tone squelch but not intercepting a private conversation. In the transmit mode a logic '0' reverses the phase of the Tx Tone Output for "squelch tail" reduction (see Table 1), this function, in Tx, should be accurately applied by a timing circuit to ensure correct system operation. |
| 24 | 21 | **Control :** This input, with Load/$\overline{\text{Latch}}$, selects the operational mode of Rx/$\overline{\text{Tx}}$ and Private Enable functions, see Table 3. |
| 25 | 22 | **Rx/$\overline{\text{Tx}}$ :** Selects the receive or transmit mode (Rx = '1', Tx = '0') and can be loaded by serial or parallel means, as described in Table 3. |
| 26 | 23 | **$\overline{\text{Private Enable}}$ :** This input selects either Private or Clear modes (Clear = '1', Private ='0'), and can be loaded by serial or parallel means, as described in Table 3. In Rx this input could be taken from the Rx Tone Decode Output. This input has an internal 1MΩ pullup resistor. |
| 27 | 24 | **Rx Tone Input :** The received tone input to the on-chip CTCSS decoder and should be a.c. coupled via capacitor $C_5$, see Figure 2. |
| 28 | 1 | **$V_{DD}$ :** Positive supply rail. A single +5V power supply is required. |

## Operational Information




| Component | Unit Value |
|---|---|
| $R_1$ | 1M |
| $R_2$ | 820k |
| $R_3$ | 330k |
| $C_1$ | 33p |
| $C_2$ | 33p |
| $C_3$ | 0.1µ |
| $C_4$ | 0.1µ |
| $C_5$ | 0.1µ |
| $C_6$ | 1.0µ |
| $C_7$ | 0.1µ |
| $C_8$ | 1.0µ |
| $C_9$ | 1.0µ |
| $C_{10}$ | 1.0n |
| $D_1$ | Small Signal |
| $X_1$ | 4MHz |

Component Tolerances
Resistors ± 10%
Capacitors ± 20%

*Fig.2 External Component Connections*

**Operational Truth Table** – Table 1 (below) illustrates the output paths and logic functions of the FX375 Private Squelch Circuit in both Receive and Transmit modes.

**Receive Operation** – (Rx/$\overline{Tx}$ = '1')
In the Rx mode Tx Tone and Tx Audio paths are held at bias.

| $D_0$ – $D_5$ | Notone | Private Enable | PTL | Rx Tone Detect | Rx Tone Decode | Receive Signal Path State | Receive Signal Path Condition |
|---|---|---|---|---|---|---|---|
| Tone | 1 | 0 | 1 | 0 | 1 | bias | X |
| Tone | 1 | 0 | 0 | 0 | 1 | open | Not Inverted |
| Tone | 1 | 0 | X | 1 | 0 | open | Inverted |
| Notone | 0 | 0 | X | X | 0 | open | Not Inverted |
| Tone | 1 | 1 | 1 | 0 | 1 | bias | X |
| Tone | 1 | 1 | 0 | 0 | 1 | open | Not Inverted |
| Tone | 1 | 1 | X | 1 | 0 | open | Not Inverted |
| Notone | 0 | 1 | X | X | 0 | open | Not Inverted |

**Transmit Operation** – (Rx/$\overline{Tx}$ ='0')
In the Tx mode the Rx audio path is held at bias and the Rx Tone Detect output at logic '0.'

| $D_0$ – $D_5$ | Notone | Private Enable | PTL | Transmitted Tone State | Transmitted Tone Phase | Transmit Signal Path State | Transmit Signal Path Condition |
|---|---|---|---|---|---|---|---|
| Tone | 1 | 0 | 1 | active | 0° | open | Inverted |
| Tone | 1 | 0 | 0 | active | 180° | open | Inverted |
| Notone | 0 | 0 | X | bias | X | open | Not Inverted |
| Tone | 1 | 1 | 1 | active | 0° | open | Not Inverted |
| Tone | 1 | 1 | 0 | active | 180° | open | Not Inverted |
| Notone | 0 | 1 | X | bias | X | open | Not Inverted |

**Notes**

1. The pre- and de-emphasis circuits remain in the Transmit path during Clear and Private operation.
2. Power remains applied to the CTCSS tone decoder at all times.
3. Carrier Frequency = 3333Hz during Private operation (Tx or Rx).
4. During Clear operation the carrier frequency is turned off to reduce spurious emissions.
5. Under Rx-Notone conditions the Notone output can be used to operate squelch circuitry.
6. The functions in this table are applicable when the device is connected as recommended in Figure 2.

*Table 1 Functions and Outputs*

## Operational Information

The logical inputs ($D_0 - D_5$) are used to programme the FX375 tone frequency (Rx/$\overline{Tx}$) as shown in Table 2 (below). Loading of data is carried out in either serial or parallel formats.

| Nominal Frequency (Hz) | FX375 Frequency (Hz) | Δfo (%) | Tone Data Programme Inputs | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ |
| 67.0 | 67.05 | + 0.07 | 1 | 1 | 1 | 1 | 1 | 1 |
| 71.9 | 71.9 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 74.4 | 74.35 | - 0.07 | 0 | 1 | 1 | 1 | 1 | 1 |
| 77.0 | 76.96 | - 0.05 | 1 | 1 | 1 | 1 | 0 | 0 |
| 79.7 | 79.77 | + 0.09 | 1 | 0 | 1 | 1 | 1 | 1 |
| 82.5 | 82.59 | + 0.1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 85.4 | 85.38 | - 0.02 | 0 | 0 | 1 | 1 | 1 | 1 |
| 88.5 | 88.61 | + 0.13 | 0 | 1 | 1 | 1 | 0 | 0 |
| 91.5 | 91.58 | + 0.09 | 1 | 1 | 0 | 1 | 1 | 1 |
| 94.8 | 94.76 | - 0.04 | 1 | 0 | 1 | 1 | 1 | 0 |
| 97.4 | 97.29 | - 0.11 | 0 | 1 | 0 | 1 | 1 | 1 |
| 100.0 | 99.96 | - 0.04 | 1 | 0 | 1 | 1 | 0 | 0 |
| 103.5 | 103.43 | - 0.07 | 0 | 0 | 1 | 1 | 1 | 0 |
| 107.2 | 107.15 | - 0.05 | 0 | 0 | 1 | 1 | 0 | 0 |
| 110.9 | 110.77 | - 0.12 | 1 | 1 | 0 | 1 | 1 | 0 |
| 114.8 | 114.64 | - 0.14 | 1 | 1 | 0 | 1 | 0 | 0 |
| 118.8 | 118.8 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 123.0 | 122.8 | - 0.17 | 0 | 1 | 0 | 1 | 0 | 0 |
| 127.3 | 127.08 | - 0.17 | 1 | 0 | 0 | 1 | 1 | 0 |
| 131.8 | 131.67 | - 0.1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 136.5 | 136.61 | + 0.08 | 0 | 0 | 0 | 1 | 1 | 0 |
| 141.3 | 141.32 | + 0.02 | 0 | 0 | 0 | 1 | 0 | 0 |
| 146.2 | 146.37 | + 0.12 | 1 | 1 | 1 | 0 | 1 | 0 |
| 151.4 | 151.09 | - 0.2 | 1 | 1 | 1 | 0 | 0 | 0 |
| 156.7 | 156.88 | + 0.11 | 0 | 1 | 1 | 0 | 1 | 0 |
| 162.2 | 162.31 | + 0.07 | 0 | 1 | 1 | 0 | 0 | 0 |
| 167.9 | 168.14 | + 0.14 | 1 | 0 | 1 | 0 | 1 | 0 |
| 173.8 | 173.48 | - 0.19 | 1 | 0 | 1 | 0 | 0 | 0 |
| 179.9 | 180.15 | + 0.14 | 0 | 0 | 1 | 0 | 1 | 0 |
| 186.2 | 186.29 | + 0.05 | 0 | 0 | 1 | 0 | 0 | 0 |
| 192.8 | 192.86 | + 0.03 | 1 | 1 | 0 | 0 | 1 | 0 |
| 203.5 | 203.65 | + 0.07 | 1 | 1 | 0 | 0 | 0 | 0 |
| 210.7 | 210.17 | - 0.25 | 0 | 1 | 0 | 0 | 1 | 0 |
| 218.1 | 218.58 | + 0.22 | 0 | 1 | 0 | 0 | 0 | 0 |
| 225.7 | 226.12 | + 0.18 | 1 | 0 | 0 | 0 | 1 | 0 |
| 233.6 | 234.19 | + 0.25 | 1 | 0 | 0 | 0 | 0 | 0 |
| 241.8 | 241.08 | - 0.30 | 0 | 0 | 0 | 0 | 1 | 0 |
| 250.3 | 250.28 | - 0.01 | 0 | 0 | 0 | 0 | 0 | 0 |
| Serial Input Mode | | | X | X | Clk | Data | 0 | 1 |
| Notone | | | 0 | 0 | 0 | 0 | 1 | 1 |

*Table 2 Tone Programming*

**Load/$\overline{Latch}$ and Control Functions** – The Load/$\overline{Latch}$ function regulates the loading of the FX375 tone frequency ($D_0 - D_5$, Table 2) in either the serial or parallel modes. The Control input enables the flexible use of the Rx/$\overline{Tx}$ and $\overline{Private\ Enable}$ functions, its use is illustrated in Table 3.

| Load Configuration | Load/$\overline{Latch}$ *Logic* | *and* Control *Logic* | Loading mode of :- $D_0 - D_5$ | Rx/Tx, Private Enable |
|---|---|---|---|---|
| Parallel | 1 | 0 | Transparent | Transparent |
| Parallel | 0 | 0 | Latched | Latched |
| Parallel | 1 | 1 | Transparent | Transparent |
| Parallel | 0 | 1 | Latched | Transparent |
| Serial | 0 | 1 | Load data in | Transparent |
| Serial | 0 – 1 – 0 | 0 | Latch data in | Latched |

**Notes**

***Glossary*** – Transparent — Data at the device inputs acts directly.
Latched — In this position data and/or functions are latched in.

'0 – 1 – 0' is a strobe pulse as shown in figures 3 and 4 (Timing).

*Table 3 Load/$\overline{Latch}$ and Control Functions*

**Timing Information...** Control instructions are input to the FX375 by serial (figure 3) or parallel (figure 4) means, using Data Inputs and Load/Latch as shown in the diagrams below.

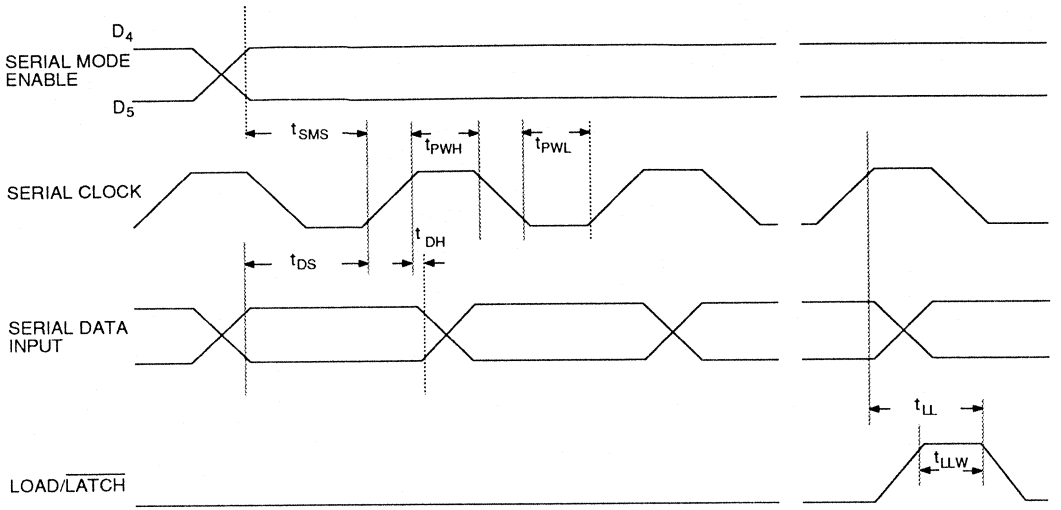



*Fig.3 Serial Load Timing*

| | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Serial** | Figure 3 | | | | |
| Serial Mode Enable Set Up Time – ($t_{SMS}$) | | 250 | – | – | ns |
| Clock 'High' Pulse Width – ($t_{pWH}$) | | 250 | – | – | ns |
| Clock 'Low' Pulse Width – ($t_{pWL}$) | | 250 | – | – | ns |
| Data Set Up Time – ($t_{DS}$) | | 150 | – | – | ns |
| Data Hold Time – ($t_{DH}$) | | 50 | – | – | ns |
| Load/Latch Set Up Time – ($t_{LL}$) | | 250 | – | – | ns |
| Load/Latch Pulse Width – ($t_{LLW}$) | | 150 | – | – | ns |
| **Parallel** | Figure 4 | | | | |
| Data Valid Time – ($t_{VP}$) | | 200 | – | – | ns |
| Load Time – ($t_L$) | | 150 | – | – | ns |
| Fall Time – ($t_F$) | | – | – | 50 | ns |
| Data Hold Time – ($t_H$) | | 50 | – | – | ns |

**Serial Loading Sequence** : With Load/Latch at logic '0' serial data is loaded in the sequence :- **$D_5$, $D_4$, $D_3$, $D_2$, $D_1$, $D_0$, Rx/Tx, Private Enable.** When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/Latch input – " 0 – 1 – 0 " (Figure 3).

*Table 4 Timing*

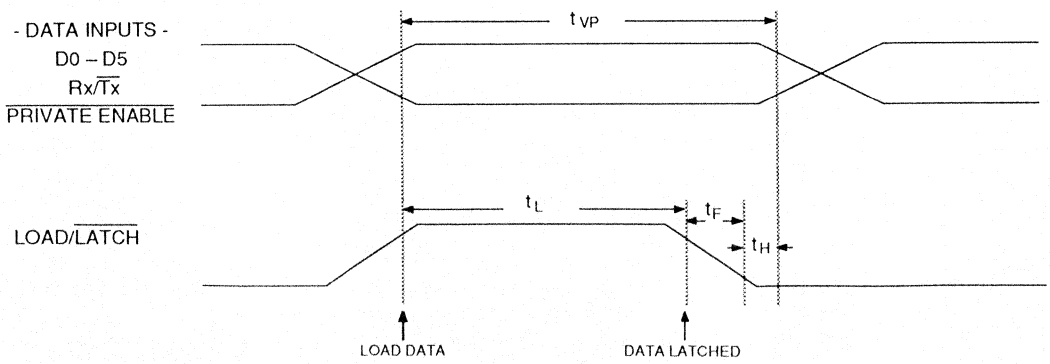



*Fig.4 Parallel Load Timing*

## Private Squelch Circuit... Application Notes

The FX375 Private Squelch Circuit utilizes Audio Frequency Inversion and Continuous Tone Controlled Squelch System (CTCSS) techniques to provide secure voice communication on a common radio channel.

**Clear/Private Switching** is controlled by the logic state of the Private Enable input. Table 1 shows that, in the receive condition the signal path will only be inverted when the programmed CTCSS tone is received. Although other logic actions will enable the receive path, privacy of the conversation is maintained at all times.

**Pre- and De-emphasis** (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

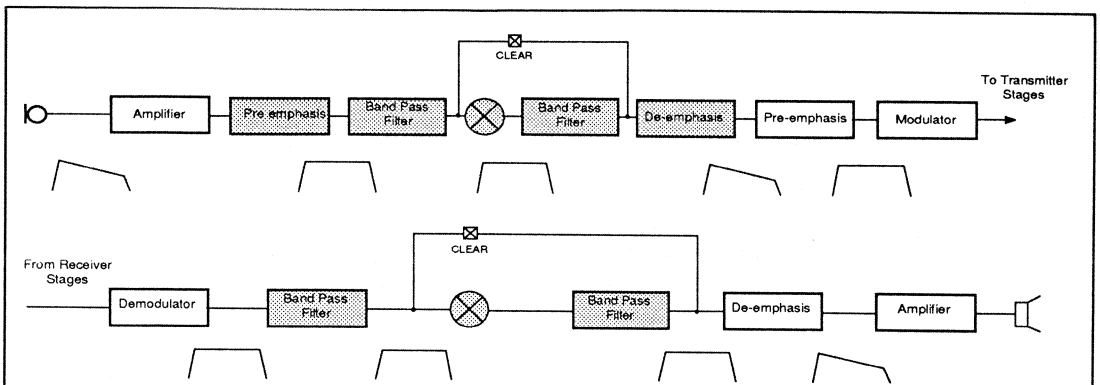



*Fig.5 The Private Squelch Circuit Installed within a Typical Audio Stage*

Figure 5 shows the recommended positioning of the FX375 (shaded areas) when installed within the audio stages of a typical transceiver system. The accompanying waveform diagrams indicate the relative "voice band amplitudes" at each stage of the receive or transmit process.

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**Installation Recommendations** – Care should be taken on the design and layout of the printed circuit board taking into consideration the points noted below.

(a) All external components (as recommended in Figure 2) should be kept close to the package.

(b) Tracks should be kept short, particularly the Audio and $V_{BIAS}$ inputs.

(c) Xtal/clock and digital tracks should be kept well away from analogue inputs and outputs.

(d) Inputs and outputs should be screened wherever possible.

(e) A "ground plane" connected to $V_{SS}$ will assist in eliminating external pick-up on input and output pins.

(f) It is recommended that the power supply rails have less than 1mV rms of noise allowed.

(g) Tx Tone Output loading – Large capacitive loads could cause this pin to oscillate. If capacitive loads in excess of 100pF are unavoidable, a resistor of 1kΩ or greater put in series with the load should minimise this effect.

## Specification

## Electrical Characteristics

### Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | - 0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | - 0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX375J** | - 30°C to + 85°C (ceramic) |
| | **FX375LG/LS** | - 30°C to + 70°C (plastic) |
| Storage temperature range: | **FX375J** | - 55°C to + 125°C (ceramic) |
| | **FX375LG/LS** | - 40°C to + 85°C (plastic) |

### Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C, Xtal/Clock $f_0$ = 4.0 MHz, Audio level 0dB ref: = 300mV rms.
Composite input signal = 0dB, 1kHz tone in –12dB (6kHz band limited) gaussian white noise with a –20dB CTCSS tone.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current : | | | | | |
| Rx /Tx (Operating) | | – | 8.0 | – | mA |
| Rx standby (No Decode) | | – | 2.8 | – | mA |
| Rx only (Decoding) | | – | 5.0 | – | mA |
| Analogue Input Impedance | | – | 0.5 | – | MΩ |
| Analogue Output Impedance | | – | 0.5 | – | kΩ |
| Tone Input Impedance | | – | 1.0 | – | MΩ |
| Digital Input Impedance | | – | 1.0 | – | MΩ |
| Input Logic '1' | | 3.5 | – | – | V |
| Input Logic '0' | | – | – | 1.5 | V |
| Output Logic '1' (I = 0.1mA) | | 4.0 | – | – | V |
| Output Logic '0' (I = 0.1mA) | | – | – | 1.0 | V |
| **Dynamic Values** | | | | | |
| Maximum Input Level | | – | + 10.5 | – | dB |
| **Decoder** | | | | | |
| Tone Input Signal Level | 1,4 | - 20 | – | – | dB |
| Response Time | 1,4,6 | – | – | 250 | ms |
| De-response Time | 1,4,6 | – | – | 250 | ms |
| Selectivity | 4 | ± 0.5 | – | ± 3.0 | %*fo* |
| **Encoder** | | | | | |
| Tone Output Level (relative 775mVrms) | | - 3.0 | 0 | + 3.0 | dB |
| Tone Frequency Accuracy | | - 0.3 | – | + 0.3 | %*fo* |
| Tone Harmonic Distortion | | – | 2.0 | 5.0 | % |
| Tone Output Load Current | 2 | – | – | 5.0 | mA |
| Output Level Variation between Tones | | – | 0.1 | – | dB |
| Rise Time (to 90% nominal level) | | | | | |
| (*fo* >100Hz) | 5 | – | 15 | – | ms |
| (*fo* <100Hz) | 5 | – | 45 | – | ms |

## Specification

### Frequency Characteristics

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Rx Clear** | | | | | |
| Total Harmonic Distortion | 3 | – | 2 | 5 | % |
| Output Noise Level | 7 | – | - 43 | – | dB |
| Passband Gain (300Hz – 3033Hz) | | – | 0 | – | dB |
| Passband Ripple (300Hz – 3033Hz) | 3 | – | – | 3 | dB |
| Audio Stopband Attenuation | | | | | |
| ($f$in > 3333Hz) | | – | 20 | – | dB |
| ($f$in > 3633Hz) | | – | 45 | – | dB |
| ($f$in < 250Hz) | | – | 42 | – | dB |
| **Rx Invert** | | | | | |
| Carrier Frequency | | – | 3333 | – | Hz |
| Total Harmonic Distortion | 3,8 | – | 4 | 10 | % |
| Baseband Breakthrough | | – | - 40 | – | dB |
| Carrier Breakthrough | | – | - 40 | – | dB |
| Output Noise Level | 7 | – | - 37 | – | dB |
| Passband Ripple (300Hz – 3033Hz) | 8 | – | – | 5 | dB |
| Audio Stopband Attenuation | | | | | |
| ($f$in > 3333Hz) | | – | 50 | – | dB |
| ($f$in > 3633Hz) | | – | 60 | – | dB |
| ($f$in < 250Hz) | | – | 60 | – | dB |
| **Tx Clear** | | | | | |
| Total Harmonic Distortion | 3 | – | 3 | 5 | % |
| Output Noise Level | 7 | – | - 43 | – | dB |
| Passband Gain (300Hz – 3033Hz) | 3 | – | 0 | – | dB |
| Passband Ripple (300Hz – 3033Hz) | 3 | – | – | 4 | dB |
| Audio Stopband Attenuation | | | | | |
| ($f$in > 3333Hz) | | – | 20 | – | dB |
| ($f$in > 3633Hz) | | – | 45 | – | dB |
| ($f$in < 250Hz) | | – | 42 | – | dB |
| Pre- and De-emphasis | | – | – | 6 | dB/octave |
| **Tx Invert** | | | | | |
| Carrier Frequency | | – | 3333 | – | Hz |
| Total Harmonic Distortion | 3,8 | – | 4 | 10 | % |
| Baseband Breakthrough | | – | - 40 | – | dB |
| Carrier Breakthrough | | – | - 40 | – | dB |
| Output Noise Level | 7 | – | - 37 | – | dB |
| Passband Ripple (300Hz – 3033Hz) | 3,8 | – | – | 5 | dB |
| Audio Stopband Attenuation | | | | | |
| ($f$in > 3333Hz) | 8 | – | 50 | – | dB |
| ($f$in > 3633Hz) | 8 | – | 60 | – | dB |
| ($f$in < 250Hz) | 8 | – | 60 | – | dB |
| Pre- and De-emphasis | | – | – | 6 | dB/octave |

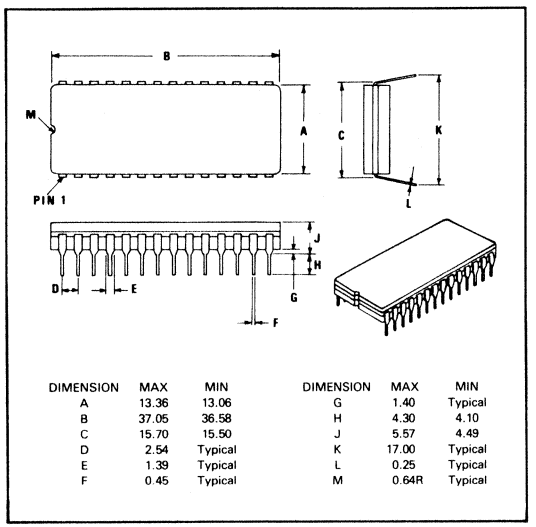
**Notes**

1. These values are obtained using the external integrator components as detailed in Figure 2.
2. An Emitter Follower output.
3. With an input signal of 1kHz @ 0dB.
4. Under Composite Signal test conditions.
5. Any programmed tone with RL = 600, CL = 15pF. Including any response to a phase reversal instruction.
6. $f$o > 100Hz, (for 100Hz > $f$o > 67Hz : t = [100/$f$o (Hz)] x 250ms).
7. Input a.c. short circuit, audio path enabled, measured in a 30kHz bandwidth.
8. Due to frequency inversion, this figures reflects the difference from the expected ideal response.

## Package Outline

The FX375J, the cerdip package is shown in Figure 6, the 'LG' version in Figure 7 and the 'LS' version in Figure 8.
Pin 1 identification marking is shown on the relevant diagram and pins on all packages number anti-clockwise when viewed from the top (indent side).

*Fig.6* ***FX375J*** *DIL Package*

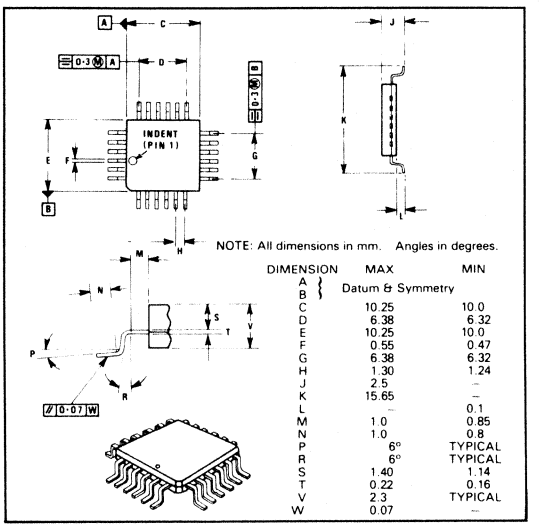



| DIMENSION | MAX | MIN | DIMENSION | MAX | MIN |
|---|---|---|---|---|---|
| A | 13.36 | 13.06 | G | 1.40 | Typical |
| B | 37.05 | 36.58 | H | 4.30 | 4.10 |
| C | 15.70 | 15.50 | J | 5.57 | 4.49 |
| D | 2.54 | Typical | K | 17.00 | Typical |
| E | 1.39 | Typical | L | 0.25 | Typical |
| F | 0.45 | Typical | M | 0.64R | Typical |

## Handling Precautions

The FX375 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

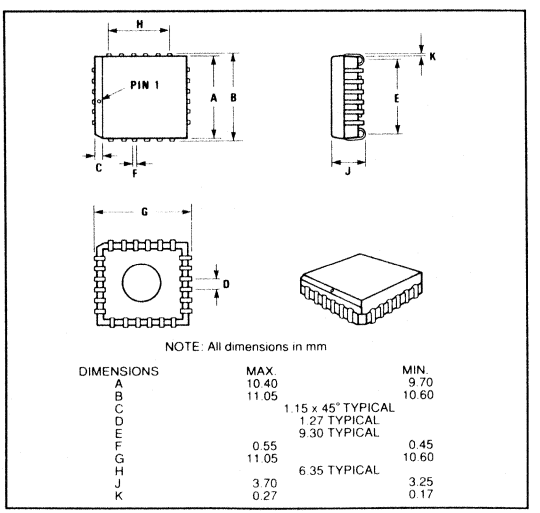
*Fig.7* ***FX375LG*** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig.8* ***FX375LS*** *Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

## Ordering Information

| | |
|---|---|
| **FX375J** | 28-pin cerdip DIL |
| **FX375LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX375LS** | 24-lead plastic leaded chip carrier |
| **FX375LH** | 28-lead plastic leaded chip carrier |

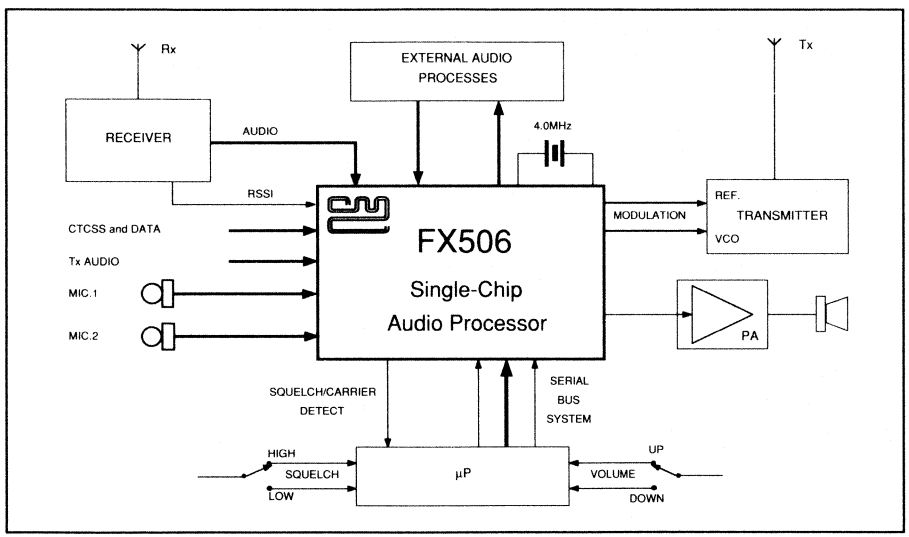
# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX506 Mobile Radio Audio Processor

Publication D/506/2 July 1991
Provisional Issue

## Features/Applications

- **Full Rx and Tx Filtering to CEPT Standards**
- **Digital Control of Volume, Noise Squelch and R.S.S.I.**
- **Tx VOGAD Circuitry**
- **Serial µP Control of ALL Chip Functions**
- **Deviation Limiter**
- **Military/Marine and Mobile Radio Applications**
- **FM/AM/SSB Applications**
- **16-kbit Data and Voice Scrambler Compatible**
- **Low-Power 5-Volt CMOS Process**




**FX506**

## Brief Description

The FX506 is a µProcessor-controlled, single-chip device containing ALL the circuit elements necessary to perform the audio functions of a mobile (or portable) radio system.

On-chip signal paths include: speech-band/pre-emphasis filters, variable gain/attenuation stages, voice-compression and deviation limiter circuitry.

Each function in the signal path can be addressed or by-passed — *providing "real-time," dynamic control* — by the µProcessor. This half-duplex device comprises two separate audio signal paths.

**The Pre-Process Path** performs filtering and level adjustment on audio (Rx or Tx) for use in auxiliary systems such as "Frequency Inversion Scrambling," "Sub-Audio" tone or "In-Band" data signalling. This path is output at the "Pre-Process Audio Output" pin. If no external processes are being used this output should be connected to the "Pre-process Audio Input" pin.

**The Post-Process Path** can adjust and prepare the input audio for output to the chosen transmitter driver or loudspeaker amplifier.

Suitably software configured, the FX506, which can operate on voice, direct-digital or tone-data and sub-audio frequencies, is compatible with FM, AM and SSB type transceivers. Digital gain elements are provided on-chip for dynamic control and balance of signal-path levels during manufacturing, test and operation.

**System Squelch**, a separate path, is sourced from either the incoming signal or Received Signal Strength Indication (R.S.S.I.) from the radio circuitry.

The FX506, a low-power 5-volt CMOS device, is available in 24-pin/lead plastic DIL and SMD packages.

## Pin Number Function

| DIL FX506P | Quad FX506LG FX506LS | |
|---|---|---|
| 1 | | **$\overline{\text{Xtal}}$:** The output of the 4.0MHz on-chip clock oscillator. |
| 2 | | **Xtal/Clock:** The input to the on-chip 4.0MHz clock oscillator inverter. All oscillator components are included on-chip. A 4.0MHz Xtal or externally derived clock should be connected here. See Figure 2. |
| 3 | | **$V_{DD}$:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the Audio Processor are dependent upon this supply. |
| 4 | | **Post Process Audio Input:** The analogue input to the Post-Process Path from external audio operations. Inputs to this pin should be a.c. coupled via a capacitor $C_7$. See Figures 2 and 4. |
| 5 | | **Pre-Process Audio Output:** The analogue output to external audio operations. See Figure 4. |
| 6 | | **Rx Audio Input:** The input from the radio receiver demodulator. This input, which requires to be a.c. coupled via capacitor $C_6$, is selected by serial data. Audio at this input will be available for use as a signal-squelch noise source. See Figures 2 and 4. |
| 7 | | **$V_{BIAS}$:** The output of the on-chip analogue bias circuitry, held internally at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ via capacitor $C_1$. See Figure 2. |
| 8 | | **CTCSS/Data Input:** To allow the introduction of sub-audio tones or data to the VCO drives. By manipulation of bits 17, 18 and 19 this input can be "mixed" into the signal path or added as a burst in between speech segments. |
| 9 | | **Tx Audio Input:** The pre-process transmit audio input. This input can be driven from an external source or from the FX506 Mic. input circuitry. See Figures 2, 3 and 4. |
| 10 | | **Mic. Output:** The output of the microphone multiplexer, selected by serial input data. If additional gain is required for the pre-process input, an external amplifier as shown in Figure 3 is recommended. |
| 11 | | **Mic.1 Input:** These separate microphone audio inputs are individually selected by the serial input data. See Figures 2, 3 and 4. |
| 12 | | **Mic.2 Input:** |
| 13 | | **$V_{SS}$:** Negative supply rail (GND). |

| Pin Number DIL FX506P | Pin Number Quad FX506LG FX506LS | Function |
|---|---|---|
| | 14 | **Compression Capacitor:** External components connected to this pin provide the required compression time-constant. See Figure 2. |
| | 15 | **Audio Output (Rx):** The received audio output from the Post-Process path. This output is data selected and when powersaved is held at $V_{BIAS}$. |
| | 16 | **VCO Ref. Drive (Tx) Output:** The output to drive the modulation reference oscillator. This output is data selected and when powersaved is held at $V_{BIAS}$. To prevent any d.c. level at this output causing incorrect frequency selection it is recommended that a.c. coupling components as shown in Figure 2 are employed. For modulation down to near d.c., these components should be by-passed. |
| | 17 | **VCO Drive (Tx) Output:** The output to drive the modulation VCO. This output is data selected and when powersaved is held at $V_{BIAS}$. |
| | 18 | **R.S.S.I.:** The input to the Squelch Selection circuitry from the radio's Received Signal Strength Indicator output. A data selected input. |
| | 19 | **Noise Input:** The noise level can be applied to this pin. This would be the Noise Output integrated by external components, as indicated in Figure 2, or an externally produced noise level. |
| | 20 | **Noise Output:** The output of the on-chip "squelch noise rectifier." This output is a half-wave rectified d.c. level that can be applied to the Noise Input via external integrating components. This output could also be used by an external signal detector circuit. This output level is at $V_{BIAS}$ for no input. See Figures 2, 3 and 4. |
| | 21 | **Squelch Drive:** A TTL compatible output. The inputs to the comparator are: the logically selected threshold level from the Digital-to-Analogue converter and the selected noise input. A logic "0" signifies that the noise threshold has been exceeded. |
| | 22 | **Serial Clock:** The externally produced serial data loading clock input. See Figure 5. This input has an internal 1MΩ pullup resistor. |
| | 23 | **Serial Data:** The controlling, 47-bit serial data input. With Chip Select maintained at a logic "0" the serial data is entered at this pin, loaded bit 46 first, bit 0 last. Detailed information on the allocation and function of serial data bits (0 to 46) is given in tabular form on later pages. Data load timing should be carried out as described in Figure 5. This input has an internal 1MΩ pullup resistor. |
| | 24 | **$\overline{\text{Chip Select}}$:** The data loading control function. During serial loading this input should be operated as shown in Figure 5. New data is latched on the rising edge of this waveform. This input has an internal 1MΩ pullup resistor. |

## External Components and Interfacing

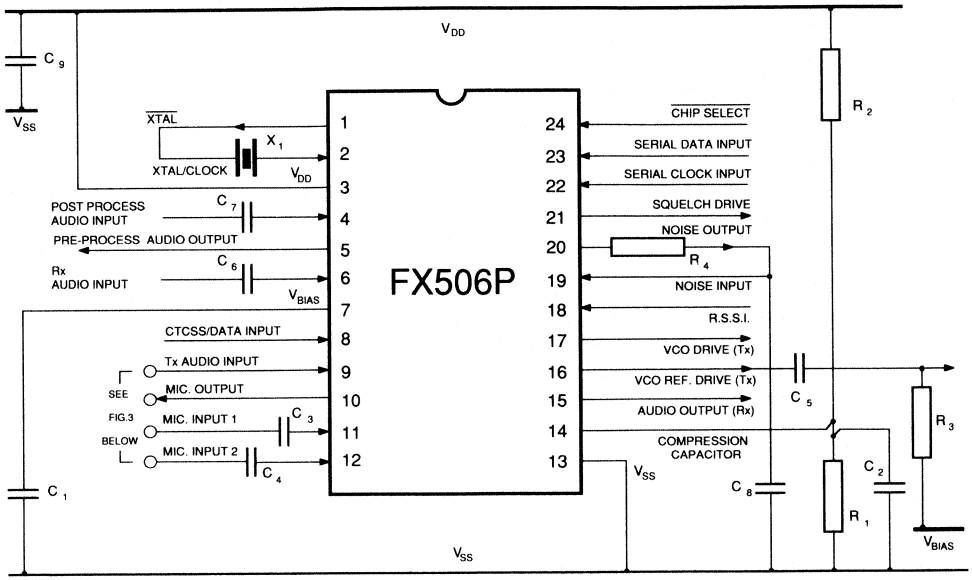



*Fig.2 Recommended External Components*

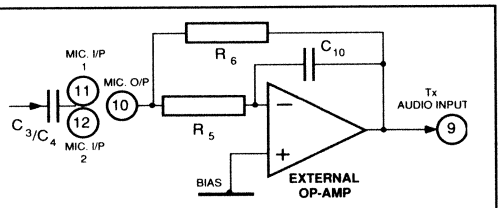



*Fig.3 Typical 2nd Order Pre-emphasis Input Circuit*

### Notes

For dual Tx inputs using both Mic.1 and Mic.2 inputs without pre-emphasis, capacitors $C_3$ and $C_4$ will be required at the inputs as shown in Figure 2.

If pre-emphasis is required, the external circuit shown in Figure 3 is recommended.

The Op-Amp selected for this application should be of a "low noise wide-bandwidth" type i.e. with at least 60dB of gain at 6kHz.

In addition to the components shown in Figure 2, it is recommended that the power and $V_{BIAS}$ lines to the external Op-Amp are decoupled to $V_{SS}$ *physically close to the amplifier*, by a 1.0µF capacitor.

## Circuit References

| Component | Value | Tolerance | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $R_1$ | 100kΩ | ±10% | $C_1$ | 1.0µF | ±20% | $C_7$ | 0.1µF | ±20% |
| $R_2$ | 390kΩ | ±10% | $C_2$ | 6.8µF | ±20% | $C_8$ | 0.1µF | ±20% |
| $R_3$ | 100kΩ | ±1% | $C_3$ | 1.0nF | ±1% | $C_9$ | 1.0µF | ±20% |
| $R_4$ | 10kΩ | ±10% | $C_4$ | 1.0nF | ±1% | $C_{10}$ | 12.0pF | ±1% |
| $R_5$ | 18.0kΩ | ±1% | $C_5$ | 15nF | ±1% | | | |
| $R_6$ | 2.7MΩ | ±1% | $C_6$ | 0.1µF | ±20% | $X_1$ | 4.0MHz | |

## Layout Recommendations

Audio microcircuit performance will be affected by external noise.

All external components should be kept as close to the device as possible.

Tracks to the device should be kept short, particularly the Audio and $V_{BIAS}$ inputs.

A "ground-plane" connected to $V_{SS}$ will help to eliminate external pick-up.

Ensure that all inputs (analogue and d.c.) are free from noise.

Xtal/clock and digital tracks should be kept well away from analogue circuitry. Analogue inputs and outputs should be screened wherever possible with high-level outputs isolated from very low-level inputs.

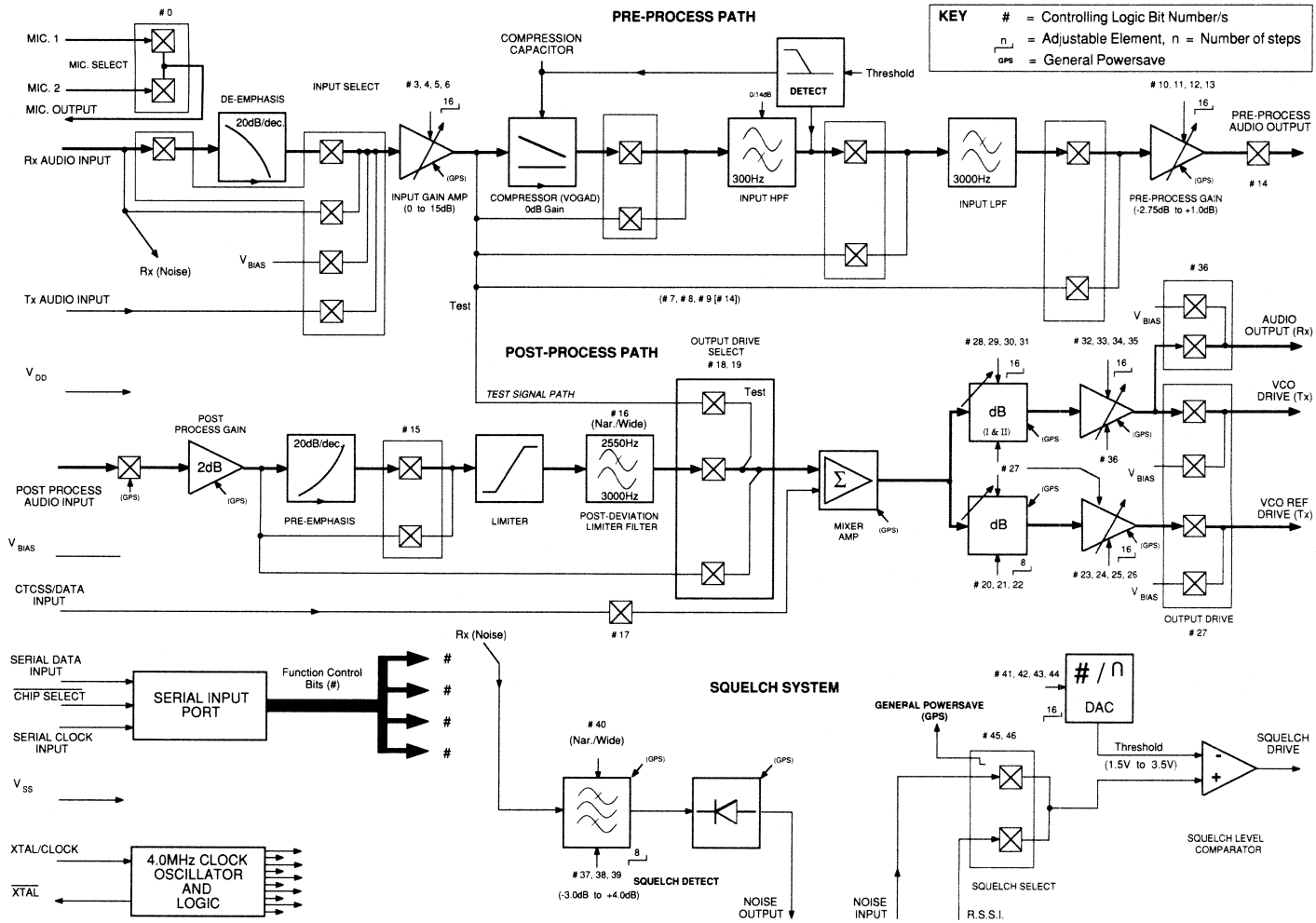



*Fig.4 PMR Audio Processor – Facilities*

| Control bits (LSB loaded last) | Function | Notes |
|---|---|---|
| **0** | **Mic. Select** | A multiplexed "microphone" input allowing the use of differing type and level voice inputs. |
| 0 | – Microphone Input 1 | |
| 1 | – Microphone Input 2 | |
| **1 2** | **Input Select** | Transmit or receive audio sources are selected, inserting the appropriate path gain for the chosen input.<br>The input path can be set to bias whilst allowing receiver noise monitoring. |
| 0 0 | – Rx Input<br>De-emphasis Bypass; HPF to 0dB | |
| 0 1 | – Rx Input<br>De-emphasis Select; HPF to 0dB | |
| 1 0 | – Tx Input<br>Powersave De-emphasis;<br>HPF to 14dB | |
| 1 1 | – Path Input to $V_{BIAS}$;<br>Powersave De-emphasis | |
| **3 4 5 6** | **Input Gain Amplifier** | A gain element intended to adjust the drive level to the compressor, catering for differing signal sources and microphone sensitivities. |
| 0 0 0 0 | – Gain Set 0.0dB | |
| 1 0 0 0 | 1.0dB | |
| 0 1 0 0 | 2.0dB | |
| 1 1 0 0 | 3.0dB | |
| 0 0 1 0 | 4.0dB | |
| 1 0 1 0 | 5.0dB | |
| 0 1 1 0 | 6.0dB | |
| 1 1 1 0 | 7.0dB | |
| 0 0 0 1 | 8.0dB | |
| 1 0 0 1 | 9.0dB | |
| 0 1 0 1 | 10.0dB | |
| 1 1 0 1 | 11.0dB | |
| 0 0 1 1 | 12.0dB | |
| 1 0 1 1 | 13.0dB | |
| 0 1 1 1 | 14.0dB | |
| 1 1 1 1 | 15.0dB | |

| *Compressor* | *HPF* | *LPF* | *Pre-Process Output* | *7 8 9 14* |
|---|---|---|---|---|
| Enabled | Enabled | Enabled | Enabled | 1 |
| Powersaved | Enabled | Enabled | Enabled | 1 |
| Powersaved | Powersaved | Enabled | Enabled | 1 |
| Powersaved | Powersaved | Powersaved | Enabled | 1 |
| Powersaved | Powersaved | Powersaved | Powersaved | 0 |

The Pre-Process Path LPF should be selected whilst CEPT 'Response to the Tx to Mod. frequencies exceeding 3kHz' tests are carried out.

| | | |
|---|---|---|
| **10 11 12 13** | **Pre-Process Gain** | An in-line output drive stage providing adjustable gain or attenuation to compensate for level tolerances in the external audio processes and peripherals.<br>The output of this amplifier stage is available for further voice (audio) processing such as "Frequency Inversion Voice Scrambling." |
| 0 0 0 0 | – Gain Set -2.75dB | |
| 1 0 0 0 | -2.50dB | |
| 0 1 0 0 | -2.25dB | |
| 1 1 0 0 | -2.00dB | |
| 0 0 1 0 | -1.75dB | |
| 1 0 1 0 | -1.50dB | |
| 0 1 1 0 | -1.25dB | |
| 1 1 1 0 | -1.00dB | |
| 0 0 0 1 | -0.75dB | |
| 1 0 0 1 | -0.50dB | |
| 0 1 0 1 | -0.25dB | |
| 1 1 0 1 | 0dB | |
| 0 0 1 1 | 0.25dB | |
| 1 0 1 1 | 0.50dB | |
| 0 1 1 1 | 0.75dB | |
| 1 1 1 1 | 1.00dB | |
| **14** | **Pre-Process Output** | Bit 14 is the Enable/Powersave function for the Pre-Process output stages.<br>See *Bits 7 8 9 14 .....* |
| 0 | – Disable Pre-Process Output<br>Output at $V_{BIAS}$ | |
| 1 | – Enable Pre-Process Audio Output | *Reference ..... Figure 4* |

| Control bits | Element | Notes |
|---|---|---|
| | **Post-Process Gain** | A fixed 2.0dB gain stage. |
| *15* | **Pre-emphasis** | A selectable pre-emphasis stage set around 1.0kHz, with a characteristic of 6dB per octave. It is available for use when transmitting data signals such as FFSK. See Table below for Powersave information. |
| | **Deviation Limiter** | A pre-set amplitude limiting stage for deviation control. |
| | **and** | |
| *16* | **Post-Deviation Limiter Filter** | This lowpass filter which is selected with the Deviation Limiter, is adjustable to Narrow (2550Hz) and Wide (3000Hz) bandwidths, allowing for different channel-spacing requirements. |
| 0 | – Narrow filter bandwidth, cut-off = 2550Hz. | |
| 1 | – Wide filter bandwidth, cut-off = 3000Hz. | |
| *17* | **CTCSS/Data Input** | |
| 0 | – Disable Input path to Mixer system | |
| 1 | – Enable Input path to Mixer system | |

| *15* | *18* | *19* | *Pre-Emphasis* | *Limiter and Post-Dev LPF* | *Drive Selected* |
|---|---|---|---|---|---|
| **X** | 0 | 0 | Powersaved | Powersaved | Test Path |
| **0** | 1 | 0 | Powersaved | Enabled | Post-ProcessPath |
| **1** | 1 | 0 | Enabled | Enabled | Post-Process Path |
| **X** | 1 | 1 | Powersaved | Powersaved | Post-Process Bypass |
| **X** | 0 | 1 | Powersaved | Powersaved | Bias |

| *20* | *21* | *22* | **VCO Reference Drive Attenuator** | |
|---|---|---|---|---|
| 0 | 0 | 0 | – Gain Set | -28dB |
| 1 | 0 | 0 | | -24dB |
| 0 | 1 | 0 | | -20dB |
| 1 | 1 | 0 | | -16dB |
| 0 | 0 | 1 | | -12dB |
| 1 | 0 | 1 | | -8.0dB |
| 0 | 1 | 1 | | -4.0dB |
| 1 | 1 | 1 | | 0.0dB |

The in-line control attenuator for the VCO reference channel drive output.

| *23* | *24* | *25* | *26* | **VCO Reference Drive Amplifier** | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | – Gain Set | -2.75dB |
| 1 | 0 | 0 | 0 | | -2.50dB |
| 0 | 1 | 0 | 0 | | -2.25dB |
| 1 | 1 | 0 | 0 | | -2.00dB |
| 0 | 0 | 1 | 0 | | -1.75dB |
| 1 | 0 | 1 | 0 | | -1.50dB |
| 0 | 1 | 1 | 0 | | -1.25dB |
| 1 | 1 | 1 | 0 | | -1.00dB |
| 0 | 0 | 0 | 1 | | -0.75dB |
| 1 | 0 | 0 | 1 | | -0.50dB |
| 0 | 1 | 0 | 1 | | -0.25dB |
| 1 | 1 | 0 | 1 | | 0dB |
| 0 | 0 | 1 | 1 | | 0.25dB |
| 1 | 0 | 1 | 1 | | 0.50dB |
| 0 | 1 | 1 | 1 | | 0.75dB |
| 1 | 1 | 1 | 1 | | 1.00dB |

The in-line control amplifier/attenuator for the VCO reference channel drive output.

| *27* | **Output Drive Control** | Used in conjunction with Bit 36 to control output functions. *Reference ..... Figure 4* |
|---|---|---|

| Control bits | Element | Notes |
|---|---|---|
| ***28 29 30***<br>0 0 0<br>1 0 0<br>0 1 0<br>1 1 0<br>0 0 1<br>1 0 1<br>0 1 1<br>1 1 1 | **VCO Drive Attenuator I**<br>– Gain Set -22.4dB<br>-19.2dB<br>-16.0dB<br>-12.8dB<br>-9.6dB<br>-6.4dB<br>-3.2dB<br>0dB | An in-line control attenuator for the VCO Tx channel drive output.<br><br>This channel is also selected as Audio Output (Rx) under the control of bit 36. This attenuator can be used in a volume control application. |
| ***31***<br>0<br>1 | **VCO Drive Attenuator II**<br>– Gain Set -25.6dB<br>0dB | An in-line control attenuator for the VCO Tx channel drive output. As an example, when bits 28 to 31 are set to "0," the gain set is -48.0dB (-22.4 + -25.6). |
| ***32 33 34 35***<br>0 0 0 0<br>1 0 0 0<br>0 1 0 0<br>1 1 0 0<br>0 0 1 0<br>1 0 1 0<br>0 1 1 0<br>1 1 1 0<br>0 0 0 1<br>1 0 0 1<br>0 1 0 1<br>1 1 0 1<br>0 0 1 1<br>1 0 1 1<br>0 1 1 1<br>1 1 1 1 | **VCO Drive Amplifier**<br>– Gain Set -2.75dB<br>-2.50dB<br>-2.25dB<br>-2.00dB<br>-1.75dB<br>-1.50dB<br>-1.25dB<br>-1.00dB<br>-0.75dB<br>-0.50dB<br>-0.25dB<br>0dB<br>0.25dB<br>0.50dB<br>0.75dB<br>1.00dB | The in-line control amplifier/attenuator for the VCO Tx channel drive output.<br>This channel is also selected as Audio Output (Rx) under the control of bit 36. This amplifier can be used in a volume control application. |
| ***27 36***<br>0 0<br>0 1<br>1 0<br>1 1 | | |

| *VCO Drive (Tx) Output* | *VCO Ref (Tx) Output* | *Audio Output (Rx)* |
|---|---|---|
| Bias | Bias | Bias |
| Bias | Bias | Enabled |
| Enabled | Enabled | Bias |
| Enabled | Enabled | Enabled |

The Drive and Ref. paths are powersaved by Bits 45 and 46 in the "Total Powersave" or "Listening Powersave" conditions. When making internal changes it is recommended that these outputs are disconnected *(placed in a bias condition)* from the relevant output (load) circuitry.

| | | |
|---|---|---|
| ***37 38 39***<br>0 0 0<br>1 0 0<br>0 1 0<br>1 1 0<br>0 0 1<br>1 0 1<br>0 1 1<br>1 1 1 | **Squelch Filter (Gain)**<br>– Gain Set -3.0dB<br>-2.0dB<br>-1.0dB<br>0dB<br>1.0dB<br>2.0dB<br>3.0dB<br>4.0dB | The squelch function is set by bits 45 & 46 (Squelch Source Selection).<br>The centre frequency gain of this element is 35dB, data selected gain variations (-3.0dB to 4.0dB) are around this value. |
| ***40***<br>0<br>1 | **Squelch Filter** (Narrow/Wide)<br>– Narrow ($fc \approx 18kHz \pm 6.5kHz$).<br>– Wide ($fc \approx 25kHz \pm 8.5kHz$). | For use in wide or narrow channel systems.<br>The squelch function is set by bits 45 & 46 (Squelch Source Selection). |

*Reference ..... Figure 4*

| Control bits | | | | Element | | Notes |
|---|---|---|---|---|---|---|
| *41* | *42* | *43* | *44* | **Squelch Threshold Voltage** | | The fine squelch adjustment level from the Digital-to-Analogue converter. These threshold levels are used as a comparison with the selected input noise voltage (bits 45 and 46). Variation in $V_{DD}$ will produce variation in threshold levels. |
| 0 | 0 | 0 | 0 | 3.500V d.c. | 70.0% $V_{DD}$ | |
| 1 | 0 | 0 | 0 | 3.366 | 67.3% | |
| 0 | 1 | 0 | 0 | 3.233 | 64.6% | |
| 1 | 1 | 0 | 0 | 3.100 | 62.0% | |
| 0 | 0 | 1 | 0 | 2.966 | 59.3% | |
| 1 | 0 | 1 | 0 | 2.833 | 56.6% | |
| 0 | 1 | 1 | 0 | 2.700 | 54.0% | |
| 1 | 1 | 1 | 0 | 2.566 | 51.3% | |
| 0 | 0 | 0 | 1 | 2.433 | 48.6% | |
| 1 | 0 | 0 | 1 | 2.300 | 46.0% | |
| 0 | 1 | 0 | 1 | 2.166 | 43.3% | |
| 1 | 1 | 0 | 1 | 2.033 | 40.6% | |
| 0 | 0 | 1 | 1 | 1.900 | 38.0% | |
| 1 | 0 | 1 | 1 | 1.766 | 35.3% | |
| 0 | 1 | 1 | 1 | 1.633 | 32.6% | |
| 1 | 1 | 1 | 1 | 1.500 | 30.0% | |
| | *45* | *46* | | **Squelch Source Selector** | | As well as selecting the input to the Noise Comparator, these two bits produce additional General Powersave (GPS) functions which control those elements not having individual serial control. |
| | 0 | 0 | | A "Total Powersave" condition | | **Powersaved:** Input Gain Amp – Post Process (2dB) Gain Amp – Mixer Amp – Noise BPF – Noise Rectifier – Squelch Comparator |
| | 1 | 0 | | Noise Input selected to Comparator | | |
| | 0 | 1 | | R.S.S.I. input selected to Comparator | | |
| | 1 | 1 | | Powersave but LISTENING condition R.S.S.I. input selected to Comparator | | **Powersaved:** Input Gain Amp – Post Process (2dB) Gain Amp – Mixer Amp – Noise BPF – Noise Rectifier |

**Rx Noise Path**

Any high-frequency noise (18kHz/25kHz) present at the Rx Audio Input will also be available at the Noise Output pin via the squelch filter and noise rectifier (when enabled) for use as a squelch detection level. This means that the FX506 can be set to "LISTEN" with the majority of circuit elements powersaved until an R.S.S.I. level is detected and produces a "Squelch Drive output."

**Test Signal Path**

This path, when selected, can be used as a direct path, via the Output Drive Selector (bits 18 and 19), to dynamically set and balance the VCO drive and reference output levels.

*Reference ..... Figure 4*

# Serial Control Bits – Loading and Timing Information

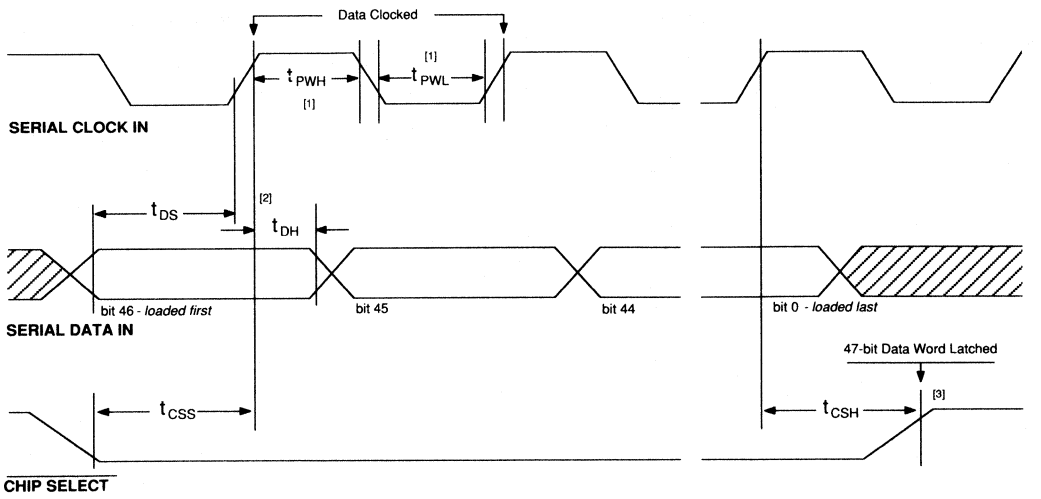



*Fig.5 Data Load Timing Diagram*

## Data Loading

Serial Data bits, whose functions are described on the previous pages, are loaded to the FX506 using the timing format illustrated on this page. All 47 bits must be loaded. Data is loaded bit 46 first, bit 0 last.

| Function | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Serial Clock** | [1] | | | | | |
| 'High' Pulse Width | | $t_{PWH}$ | 600 | – | – | ns |
| 'Low' Pulse Width | | $t_{PWL}$ | 600 | – | – | ns |
| **Serial Data** | [2] | | | | | |
| Data Set-Up Time | | $t_{DS}$ | 360 | – | – | ns |
| Data Hold Time | | $t_{DH}$ | 120 | – | – | ns |
| **Chip Select** | [3] | | | | | |
| Select Set-Up Time | | $t_{CSS}$ | 600 | – | – | ns |
| Select Hold Time | | $t_{CSH}$ | 600 | – | – | ns |

[1] The Serial Clock pulses do not have to be symmetrical, as shown above, but pulse lengths must conform to the "minimum" time specification.

[2] Individual data bits (logic "1" or "0") are loaded to the device on the rising edge of the input Serial *Data* Clock pulse. The data hold period ($t_{DH}$) is to ensure that the data level is steady when it is sampled.

[3] The full 47-bit data word is latched into the device on the rising edge of the Chip Select waveform, at this time the loaded data is acted upon and the circuit configuration/settings will change.

## System Response Characteristics

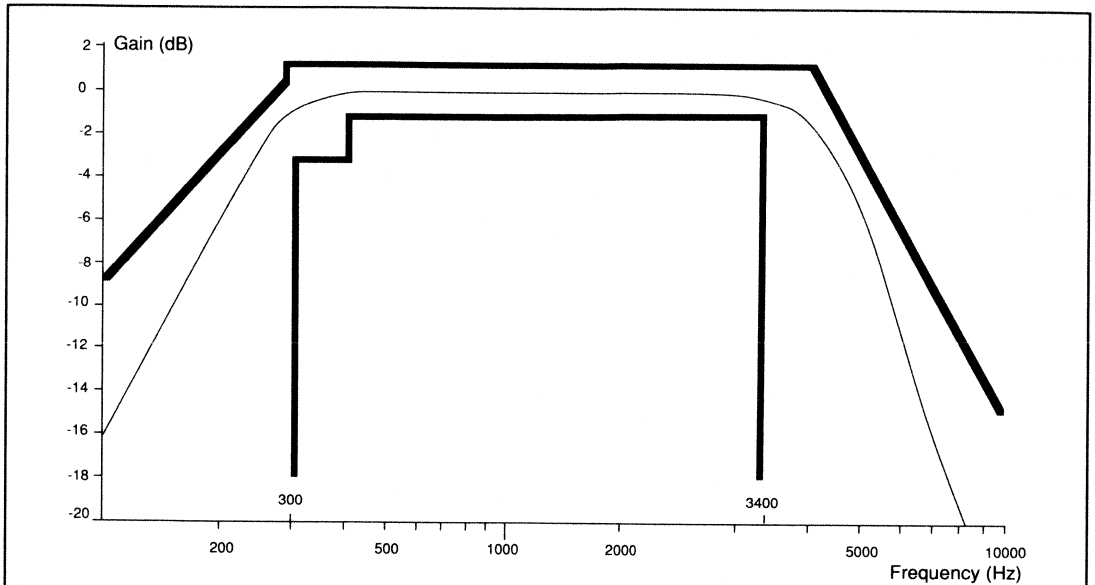



*Fig.6 Typical Pre-Process Path Frequency Response*

## System Frequency Characteristics

Figure 6 shows a typical, response curve of the Pre-Process Path, in receive mode, set against the device specification. The general characteristic shape is produced by the Input Highpass and Lowpass Filters, without the internal pre-emphasis element.

Figure 7 shows a typical response curve of the Post-Process Path set against the device specification. The general characteristic shape is produced by the Post-Deviation Limiter Filter, without the de-emphasis element.

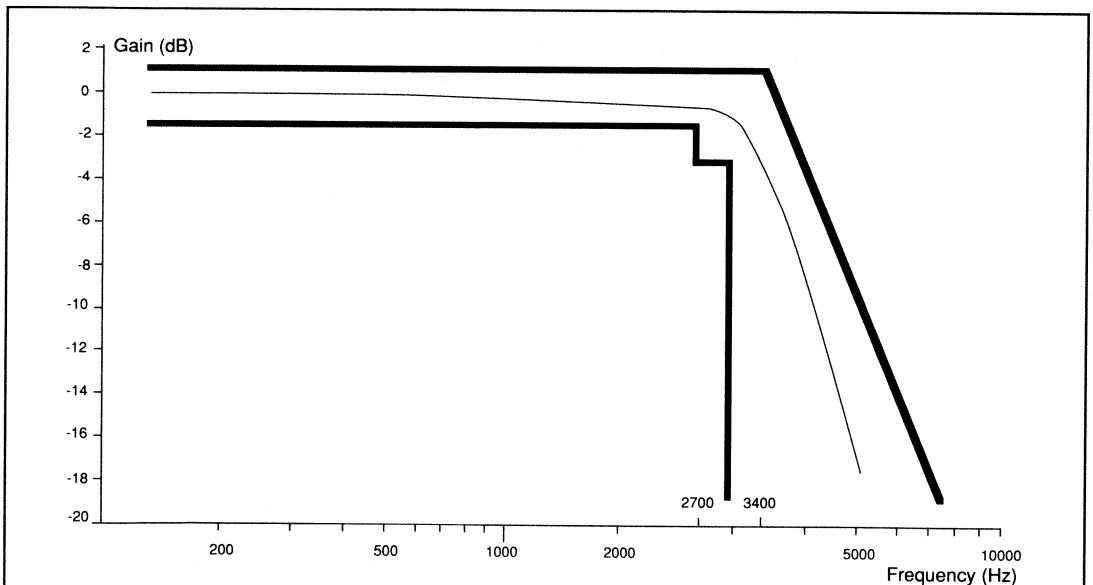



*Fig.7 Typical Post-Process Path Frequency Response*

# Application Information .....

## Suggested Evaluation Tests and Settings

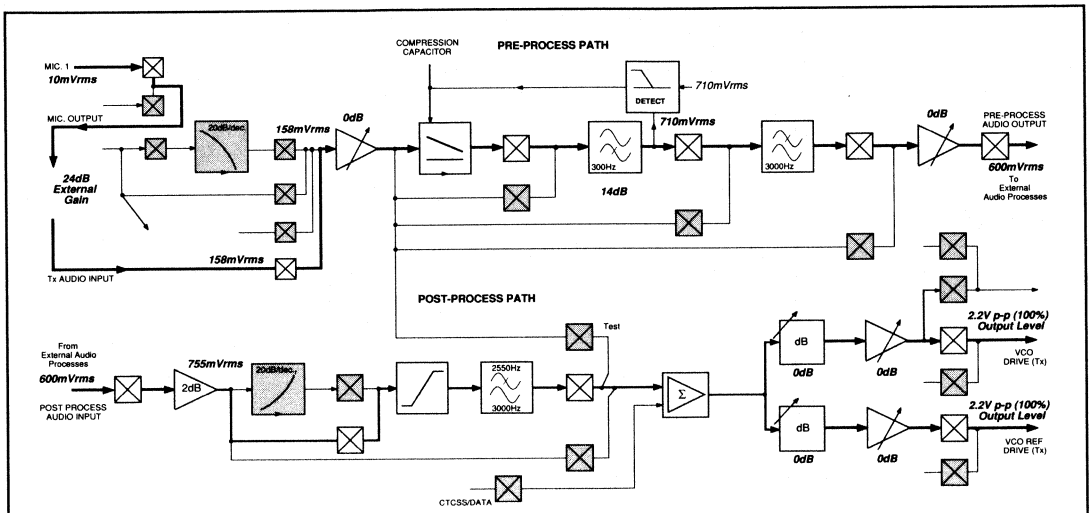



*Fig.8 Transmit Path – Suggested Test Settings*

Active elements used in the signal path.

Powersaved or by-passed elements that are not employed in the signal path.

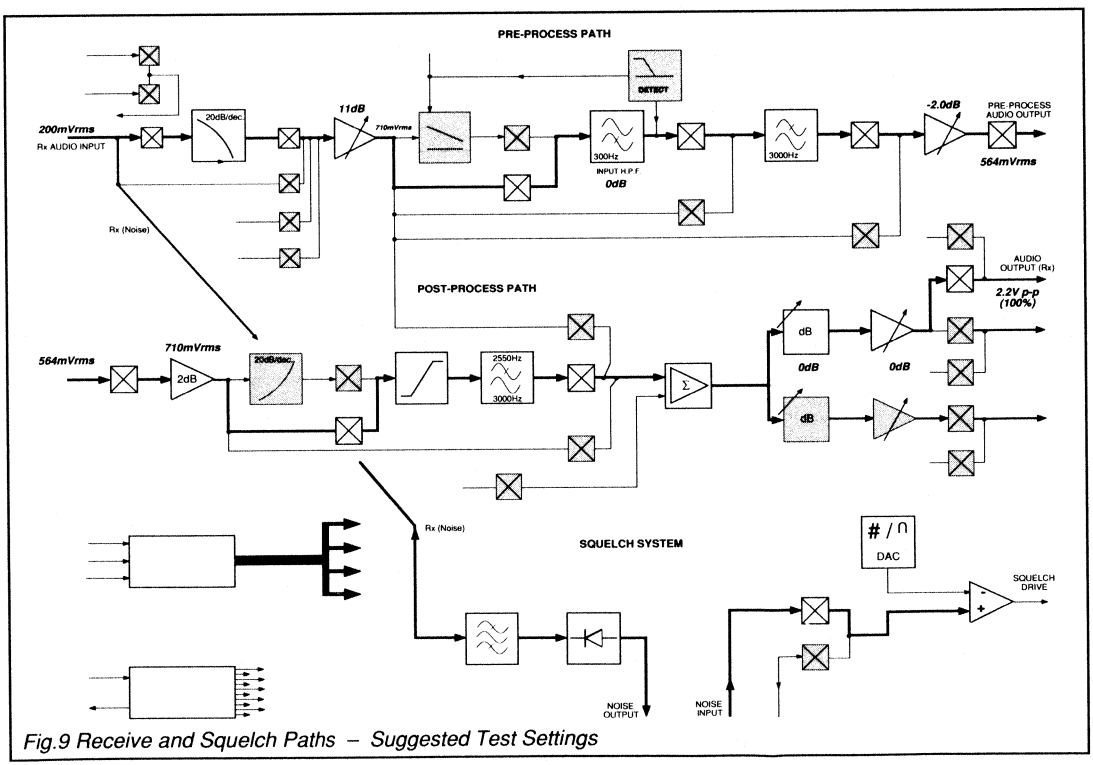



*Fig.9 Receive and Squelch Paths – Suggested Test Settings*

# Application Information

## Suggested Evaluation Tests and Settings

## Operational Information

The functions of the FX506 are selected and controlled using the 47-bit Serial Data Input. This application section assists in the familiarization of control by providing example operational paths and system confidence tests.

The signal levels employed in these examples are to demonstrate the functions of the device. Maximum and minimum operational signal levels are detailed in the "Specification" pages. A final output signal level of 2.2V p-p is considered, operationally, to be 100% (FM deviation).

Set-up and enter the example data word in accordance with Figures 2 and 4.
Test the FX506 using levels and points detailed in Tables 1, 2 and 3.

Experimentation will indicate the signal element configuration and required control settings for various input and output levels.

**Transmit Path** – *The Serial Data word below will produce the transmit element configuration shown in Figure 8.*

bit 0 – **01000001 11110110 X0101111 10111111 11010XXX XXXXX10** – bit 46

**0** = logic 0 **1** = logic 1 **X** = not important to the example

| Step | Input | – Level (mV rms @ 1kHz) | Output | – Level (mV rms @ 1kHz) | Note | Output Level Ref. to Max. |
|---|---|---|---|---|---|---|
| 1 | Mic. 1 | 10 | Pre-Process Audio | 750 | Ext +24.0dB | |
| 2 | Ext. Audio Process In | 750 | VCO Drive/Ref. | 1.54≤ $V_{OUT}$ ≤2.2Vp-p | | 70 – 100% |
| 3 | Mic. 1 | 4.8 | Pre-Process Audio | 410 | Ext +24.0dB | 60% |
| 4 | Ext. Audio Process In | 410 | VCO Drive and Ref. | 466 | | 60% |

*Table 1 Transmit Path Operational Check*

To establish a 100% level for this device inject a large amplitude audio signal into the Post Process Audio Input, with the Limiter enabled.

**Receive Path** – *The Serial Data word below will produce the receive element configuration shown in Figure 9.*

bit 0 – **X0111010 11110010 X010XXXX XXX01111 11011XXX XXXXX10** – bit 46

**0** = logic 0 **1** = logic 1 **X** = not important to the example

| Step | Input | – Level (mV rms @ 1kHz) | Output | – Level (mV rms @ 1kHz) | Note | Output Level Ref. to Max. |
|---|---|---|---|---|---|---|
| 1 | Rx Audio In | 200 | Pre-Process Audio | 564 | | |
| 2 | Ext. Audio Process In | 564 | Audio Out (Rx) | 1.54≤ $V_{OUT}$ ≤2.2Vp-p | | 70 -100% |
| 3 | Rx Audio In | 145 | Audio Out (Rx) | 466 | | 60% |
| 4 | Rx Audio In | 145 | Audio Out (Rx) | 466± | | 60%± |
| | | | | | vary bits 28 – 35 for Volume | |

*Table 2 Receive Path Operational Check*

To establish a 100% level for this device inject a large amplitude audio signal into the Post Process Audio Input, with the Limiter enabled.

**Squelch Path** – *The Serial Data word below will produce the squelch element configuration shown in Figure 9.*

bit 0 – **X00XXXXX XXXXXX0X X010XXXX XXX0XXXX XXXX1110 1110110** – bit 46

**0** = logic 0 **1** = logic 1 **X** = not important to the example

| Step | Input | – Level (mV rms @ 25kHz) | Output | – Level | Note |
|---|---|---|---|---|---|
| 1 | Rx Audio In | 0 | Squelch Drive | logic "1" | No noise – "Noise Out" = $V_{BIAS}$ |
| 2 | Rx Audio In | 50.0 | Squelch Drive | logic "0" | Noise In – "Noise Out" decreases |

*Table 3 Squelch Path Operational Check*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX506P** | -30°C to +70°C (plastic) |
| | **FX506LG/LS** | -30°C to +70°C (plastic) |
| Storage temperature range: | **FX506P** | -40°C to +85°C (plastic) |
| | **FX506LG/LS** | -40°C to +85°C (plastic) |

### Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.0MHz. Audio level 0dB ref: = 466mV rms @ 1.0kHz *(60% deviation, FM).*

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Values** | | | | | | |
| Supply Voltage | | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | (All Elements Enabled) | | – | 8.0 | – | mA |
| | (Listening Powersave) | | – | – | 1.0 | mA |
| | (Maximum Powersave) | | – | – | 1.0 | mA |
| **Dynamic Values** | | | | | | |
| Input Logic "1" | | 1 | 3.5 | – | – | V |
| Input Logic "0" | | 1 | – | – | 1.5 | V |
| **Input Impedances** | | | | | | |
| Digital | | | 0.1 | 1.0 | – | MΩ |
| Mic.1 or 2 | | | – | 0.5 | – | kΩ |
| Rx Audio | | | 30.0 | – | – | kΩ |
| Tx Audio | | | 30.0 | 56.0 | – | kΩ |
| CTCSS/Data | | | 50.0 | 100 | – | kΩ |
| External Audio Process | | | 1.0 | – | – | MΩ |
| Noise, R.S.S.I. | | | 1.0 | – | – | MΩ |
| **Output Impedances** | | | | | | |
| Pre-Process Audio | | | – | – | 3.0 | kΩ |
| Audio Out (Rx) | | | – | – | 3.0 | kΩ |
| VCO Drive and Ref. Out | | | – | – | 3.0 | kΩ |
| Squelch Drive | (Logic "1") | | – | 5.0 | – | kΩ |
| | (Logic "0") | | – | 500 | – | Ω |
| Noise Output | (Diode conducting) | | – | 1.0 | – | kΩ |
| | (Diode not conducting) | | – | 500 | – | kΩ |
| **Signal Path Switch Isolation** (Disabled) | | | | | | |
| Switches | | | 40.0 | – | – | dB |
| Test Path | | | – | 60.0 | – | dB |
| **Signal Input Levels** | | 10 | | | | |
| Mic.1 or 2 | | | 1.0 | – | 100 | mV rms |
| Rx Audio | | | – | 145 | 200 | mV rms |
| Tx Audio | | | – | – | 1414 | mV rms |
| CTCSS/Data | | | – | – | 4.0 | V p-p |
| Post Process | | | – | – | 1123 | mV rms |
| Noise, R.S.S.I. | | 2 | – | – | 4.0 | V p-p |
| **Signal Output Levels** | | 10 | | | | |
| Pre-Process Audio | (Compressor enabled) | | – | 600 | – | mV rms |
| VCO – (Drive, Ref.) | (Limiter in circuit) | | – | 2.2 | – | V p-p |
| Audio (Rx) | (Limiter in circuit) | | – | 2.2 | – | V p-p |
| **Variable Element Step** | | | | | | |
| Input Gain Amp | | | 0.7 | | 1.3 | dB |
| Pre-Process Gain | | | 0.2 | | 0.3 | dB |
| VCO Ref. Attenuator | | | 3.5 | | 4.5 | dB |
| VCO Drive Attenuator I | | | 2.7 | | 3.7 | dB |
| VCO Drive Attenuator II | | | 25.0 | | 26.2 | dB |
| VCO Amplifiers (Drive and Ref.) | | | 0.2 | | 0.3 | dB |

# Specification .....

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Output Distortion** | | | | | | |
| Output Signal-to-Noise Ratio | | 3, 12 | 48.0 | 52.0 | – | dBp |
| Total Harmonic Distortion Level | | 4, 11 | – | -40.0 | -30.0 | dB |
| **Compressor** | | | | | | |
| Dynamic Range | | | – | 30.0 | – | dB |
| Attack Time | | | – | 7.0 | – | ms |
| Decay Time | | | – | 1000 | – | ms |
| **Deviation Limiter** | | | | | | |
| Input Thresholds | | 4 | – | 2.0 | – | V p–p |
| **Frequency Responses** | | | | | | |
| **Pre-Process Path** | | 6 | | | | |
| Passband Frequencies | | | | | | |
| -3dB (Lower) | | | – | 240 | – | Hz |
| -3dB (Upper) | | | – | 4.7 | – | kHz |
| Passband Ripple | (300Hz - 400Hz) | 5 | -3.0 | – | 1.0 | dB |
| | (400Hz - 3400Hz) | 5 | -1.5 | – | 1.0 | dB |
| Stopband Attenuation | ($f$ = 5kHz) | | 3.0 | 4.2 | – | dB |
| High Frequency Roll-off | ($f$ = >5kHz, <20kHz) | | 12.0 | – | – | dB/oct. |
| Stopband Attenuation | ($f$ = 250Hz) | | – | 2.3 | – | dB |
| Low Frequency Roll-off | ($f$ = <250Hz) | | 6.0 | – | – | dB/oct. |
| **Post-Process Path** | | 7 | | | | |
| Wideband : Lowpass Frequency (-3dB) | | | – | 3.4 | – | kHz |
| Passband Ripple | (< 2700Hz) | 8 | -1.5 | – | 1.0 | dB |
| | (2700Hz - 3000Hz) | 8 | -3.0 | – | 1.0 | dB |
| Stopband Attenuation | ($f$ = 5kHz) | | 12.2 | 17.0 | – | dB |
| High Frequency Roll-off | ($f$ = >3kHz, <20kHz) | | 18.0 | – | – | dB/oct. |
| Narrowband: Lowpass Frequency (-3dB) | | | – | 2.9 | – | kHz |
| Passband Ripple | (< 2300Hz) | | -1.5 | – | 1.0 | dB |
| | (2300Hz - 2550Hz) | | -3.0 | – | 1.0 | dB |
| Stopband Attenuation | ($f$ = 4.25kHz) | | 12.2 | 17.0 | – | dB |
| High Frequency Roll-off | ($f$ = >2.3kHz, <5.1kHz) | | 18.0 | – | – | dB/oct. |
| Pre-emphasis: Passband Frequencies | | | 300 | | 3000 | Hz |
| Gain at 1kHz | | | – | 0 | – | dB |
| Slope Characteristic | | | – | 6.0 | – | dB/oct. |
| De-emphasis: Passband Frequencies | | | 300 | | 3000 | Hz |
| Gain at 1kHz | | | – | 0 | – | dB |
| Slope Characteristic | | | – | 6.0 | – | dB/oct. |
| **Squelch Bandpass Filter** | | | | | | |
| Centre Frequency Gain | (Wide and Narrow) | | – | 35.0 | – | dB |
| Selectable Gain | (8 x 1.0dB steps) | 9 | -3.0 | – | 4.0 | dB |
| Narrow Band: | | | | | | |
| Centre Frequency | ($fc$) | | – | 18.75 | – | kHz |
| Bandwidth | ($fc$ ±) | | – | 6.5 | – | kHz |
| Wideband: | | | | | | |
| Centre Frequency | ($fc$) | | – | 25.5 | – | kHz |
| Bandwidth | ($fc$ ±) | | – | 8.5 | – | kHz |

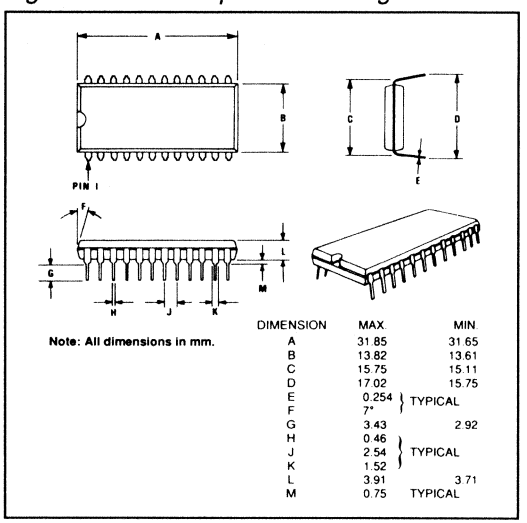
**Notes**

1. A percentage of the applied $V_{DD}$ (70% or 30%).
2. These inputs are compared internally with the Digital-to-Analogue converter.
3. With a minimum signal input level of 50mVrms at the Tx I/P or 65mVrms at the Rx I/P and an output level of 466mVrms.
4. Levels at the input of the Limiter element, centred about $V_{BIAS}$ (Note 2).
5. This parameter remains within specification when pre-emphasis is employed.
6. With both Input HPF and LPF in circuit, but without pre-emphasis.
7. With Limiter LPF, but without de-emphasis characteristics.
8. This parameter remains within specification when de-emphasis is employed.
9. The gain variation around the centre frequency ($fc$).
10. See Application Information pages (Suggested Evaluation Tests) for information on gain element settings.
11. Mode: Tx with Compressor "OFF;" or in Rx, signal below limiter thresholds; Output level 466mVrms. Measured in a 30kHz bandwidth.
12. In the Tx mode with the Input Gain Amp set to ≤ 4.0dB.

## Package Outline

The FX506P, the dual-in-line package is shown in Figure 10. The 'LG' version is shown in Figure 11 and the 'LS' version in Figure 12.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).

*Fig.10* ***FX506P*** *24-pin DIL Package*




Note: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 31.85 | 31.65 |
| B | 13.82 | 13.61 |
| C | 15.75 | 15.11 |
| D | 17.02 | 15.75 |
| E | 0.254 | TYPICAL |
| F | 7° | |
| G | 3.43 | 2.92 |
| H | 0.46 | TYPICAL |
| J | 2.54 | |
| K | 1.52 | |
| L | 3.91 | 3.71 |
| M | 0.75 | TYPICAL |

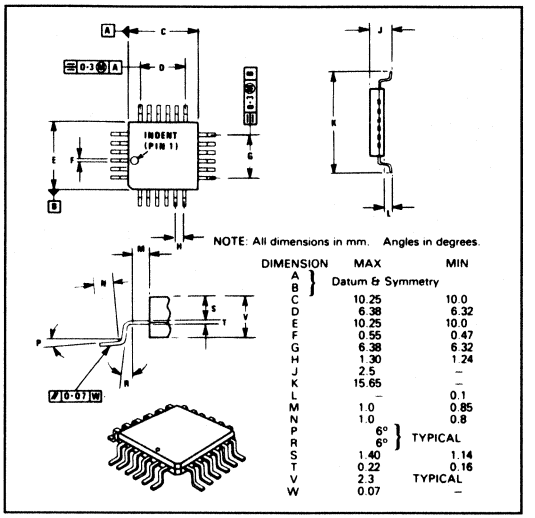
## Ordering Information

| | |
|---|---|
| **FX506P** | 24-pin plastic DIL |
| **FX506LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX506LS** | 24-lead plastic leaded chip carrier |

## Handling Precautions

The FX506 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

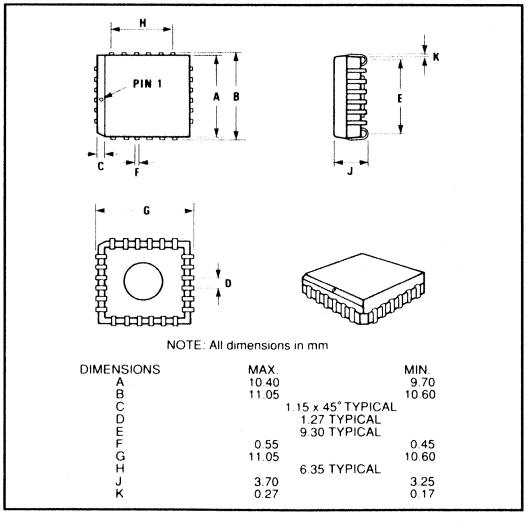
*Fig.11* ***FX506LG*** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

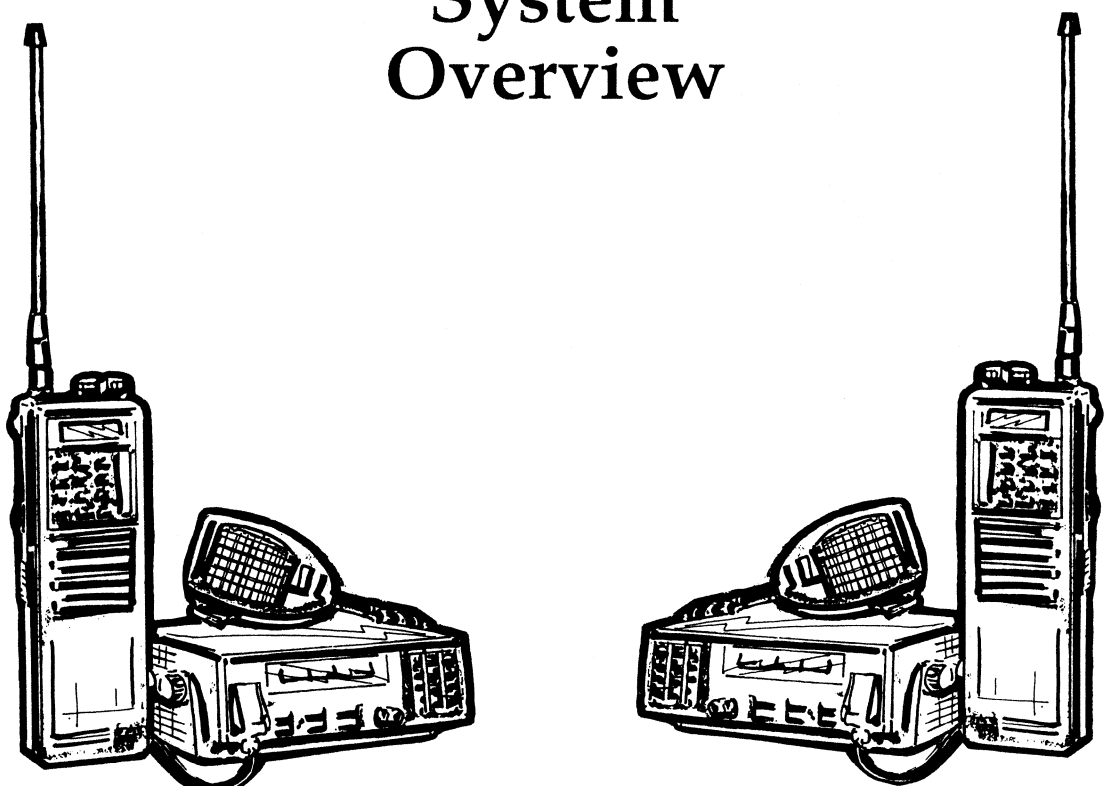
*Fig.12* ***FX506LS*** *24-lead Package*




NOTE: All dimensions in mm

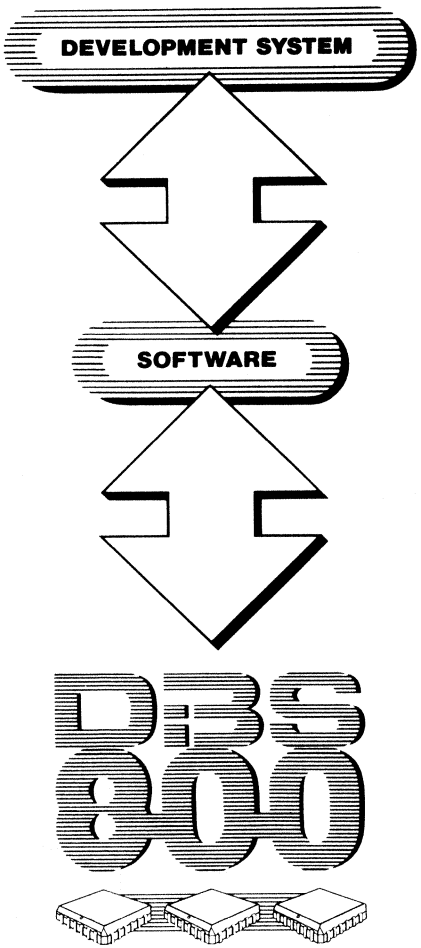
| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

# System Overview



Publication D/800/Intro/3 December 1991

# Concept




## DBS 800 Concept

The World's first **D**igitally-Integrated **B**aseband **S**ystem consisting of audio processing and signalling devices for use within a two-way mobile or trunked radio. Whilst supporting all internationally mandated or system specific requirements for processing and signalling, DBS 800 incorporates many powerful higher-level functions which offer a flexible and low-cost route to the "Added Value" opportunities in the PMR market.

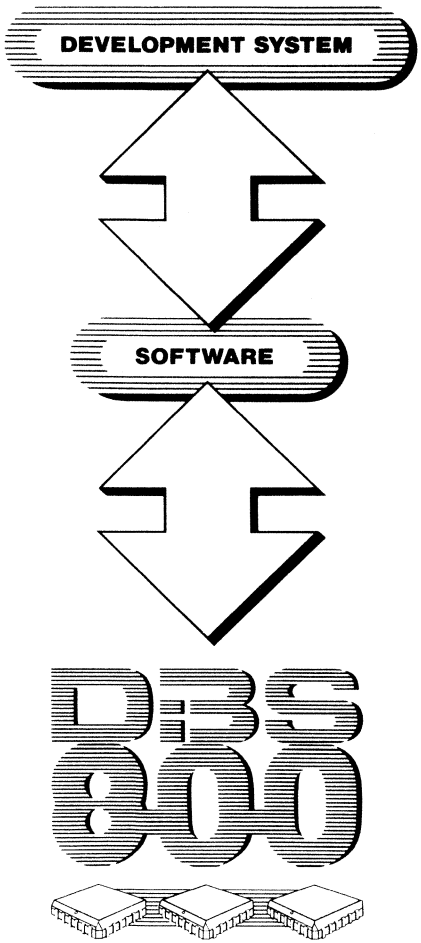
In support of the products functions, a development kit including all DBS 800 integrated circuits, together with a support microprocessor and software, allows evaluation, demonstration and software development to be completed in a fraction of the time normally taken.

DBS 800 has been conceived with the mobile radio hardware and software development engineer in mind. All ICs have been designed as peripherals to the radio's host microprocessor and require the minimum amount of software to control them. A single Address and Data hardware bus ("C-BUS") is used on all ICs, ensuring ease of connection to the host microprocessor and minimum track layout.

The advanced features offered by DBS 800 will have implications in reducing design, test, manufacture and service time whilst offering new and advanced facilities to the user and service provider.

In summary, DBS 800 provides a single, low-cost, fast turn-around design approach for simple or the most sophisticated multi-mode mobile or trunked radios intended for world-wide markets.

# Features




## DBS 800 Features

- Complete audio processing (CEPT, EIA, etc.)
- Universal Signalling
  *Selcall (CCIR, ZVEI I, II, III, EEA etc.)*
  *CTCSS (EIA, EEA)*
  *DPL™, Digital Coded Squelch (DCS)*
  *Digital Selcall 1200 BAUD FFSK (MPT1317/1327)*
  *DTMF encode*
  *LTR™, NRZ Data*
  *2-Tone, Special Tones*
- Data communications with data storage and buffering
- Voice/Data Scrambling
- Voice Management
  *Voice storage, Mailbox, delay, busy buffer, alarms and status – Reduced airtime usage – Increased spectrum efficiency – VOX/Handsfree operation*
- System Management
  *Over-air programming/re-configuration and cloning – Call billing/monitoring/blocking – Tx time-out/selective lockout – Repeater access/control – Direct control of all system radio units*
- ANI (automatic number ident)
- Half-duplex repeater
- Common Control and Data Bus ("C-BUS")
- Hardware Development Kit
- Software Support
  *Evaluation – Demonstration – Development*
- Electronic digital trimming and volume control
- Adaptive compensation for non-linear and temperature effects
- Two-Point Modulation for trunked/scanning schemes
- Fully automated test/alignment/servicing
- Self-Test mode
- Single hardware design approach
  *software reconfigurable*
- Fully integrated solution reduces PCB area
- Greatly reduced development time
- Multi-level powerdown modes
- -40°C to +85°C operating range
- +5-volt low-power CMOS
- Surface Mount packaging

# Benefits

## Design Electronic

- **DBS 800** offers a single design approach for all mandatory and system specific audio processing and signalling requirements. Inherent value-added features are provided for future upgrades, purely by modifying software.
- Single Address/Data/Audio I/O bus simplifies electronic interconnections between devices. Future 'option' upgrades can be added by simple connection to the "C-BUS" structure.
- Development Kit greatly reduces timescales, from initial mobile radio concept to pre-production stage, by utilizing the following software support.

  1. Evaluation software - allows the design engineer to check within a few hours the electrical performance of all DBS 800 devices, e.g. Dynamic range, SNR, current consumption etc.

  2. Demonstration software - offers a quick route to demonstrate the advanced features offered by DBS 800.

  3. Application software - offers numerous software routines which perform standard functions such as Selcall, Scrambling, Voice storage etc. These software packages may be used as part of the final operating software of the mobile radio.

  **NOTE.** This software is provided in a high-level language allowing ease of modification/addition and ultimate compilation for the chosen host microprocessor.
- Single design concept can be used for all models of mobile radio with differing features or market destinations: Software reconfigurable.
- One microprocessor is required to control all radio functions, DBS 800 devices contain additional hardware to minimize software overhead.
- Digitally controlled trimmers allow for 'adaptive adjustment' of non-linear "VCO conversion gain," and temperature effects. This allows use of cheaper, lower-tolerance components.
- "Non-predictive decoding of signalling" devices gives total design flexibility.
- Integrated solution offers higher relability.

## Design Mechanical

- Fully integrated processing and signalling design approach, offered by DBS 800, minimizes PCB area.
- Adaptive trimming removes need for electro-mechanical trimmers, volume control etc. Trimmer tool access is no longer required through metal shielding.
- Fully electronic solution offers ease of design for harsh environments - waterproofing, intrinsic safety, vibration, etc.
- Smaller, lighter equipment design possible - handhelds.
- Surface mount packages allows fully automated assembly.
- "C-BUS" simplifies PCB layout and reduces tracking space.

## System Operator

- By far the greatest advantage of DBS 800 to the system operator is the system management and control functions leading to more efficient airtime usage. The result being more users per channel and therefore higher revenue.
- Total system control and management; Selective lockout 'stun,' call-barring, call monitoring, billing, user specific Tx-timing etc.
- DBS 800 is compatible with all existing signalling schemes such as Selcall, CTCSS, DPL™, DCS, 2-Tone, DTMF, LTR™,/MPT1327 Trunking.
- Advanced signalling; Digital Selcall, ANI, overair re-configuration, cloning, channel dependent signalling.

# Benefits .....

- Voice Compression and Pause Elimination may be used to reduce air-time usage.
- Non-predictive decoding offers features such as recognition and identification of own repeater CTCSS tone, multiple group call etc.
- Value-added voice management features voice security, voice mailbox, voice status, voice alarm, voice buffering when channel busy.
- Repeater use; adaptive signalling, software controlled selective Tx delay/timeout. Lower cost repeaters through use of non-predictive decoding. Additional sub-audible/ Selcall signalling schemes offers a greater coding capability.
- MPT1317/1327 trunking capability.

## User

- Smaller, lower cost multi-feature mobile radios.
- Voice buffering allows user to speak into microphone at will regardless if channel is busy. The stored voice is transmitted automatically on channel clear down.
- Voice mailbox offers an answering machine facility to the mobile radio user.
- Handsfree/VOX facility, particularly in trunked radio applications having long call set-up times.
- Voice security, Call security for little or no hardware overhead, i.e. 'low cost Scrambling.'
- Data communications - ability to connect directly to mobile radio, with no external interface, laptop PC's, printers etc. RS232 interface or others possible. Data storage and security are purely software dependant.
- Integrated solution will result in greater equipment reliability and fewer service/repair intervals.

## Manufacture

- Fully integrated surface mount packaged devices with few external passive components allows fully automated assembly.
- Low component count reduces manufacturing time/cost.
- Simplified inventory by using standard DBS 800 chip-set thus further reducing costs.
- Minimum labour content in manufacture and test.

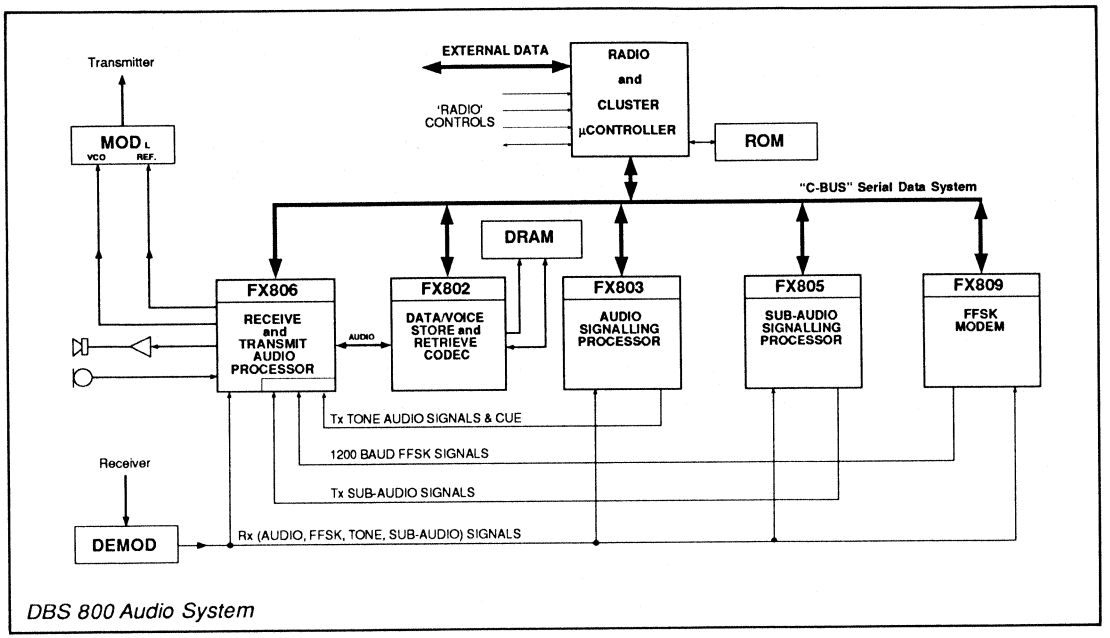
## Test

- All radio parameters can be adjusted by ATE without the need for any manual adjustments, leading to; Tighter control, repeatability, higher quality/fully automated reporting.
- Radios can be calibrated and tested when completely assembled by using a single external audio/data/RF connection only.
- Simplified ATE design.
- Reduced test and alignment times - fully automated.

## Servicing

- Fully computerized 'fast fault' diagnosis.
- Automated testing reduces service time.
- Radio test, re-calibration and reprogramming of radio functions can be carried out without need for removal of radio equipment.
- Self-test modes with audible/visual alert outputs.
- Lower service costs - "While-U-Wait" servicing or customer self-testing.
- Simple field-test unit can be used to test or reconfigure radios incorporating DBS 800.

# System Introduction




*DBS 800 Audio System*

## DBS 800

### Digitally-integrated Baseband System

A family of digitally controlled low-power CMOS audio microcircuits with supporting evaluation/design hardware and software for use collectively or individually within the audio and auxilliary stages of Private Mobile Radio (PMR) communications systems.

As a system, the DBS 800 microcircuits will perform the "core" audio functions shown below, producing a true "multi-mode" radio.

### DBS 800 Functions

- **FX802 DVSR Codec**

Voice Digitization, Data and Voice Storage and Retrieval, using Continuously Variable Slope Delta Modulation. Data buffering and transfer is via an on-chip Dynamic RAM Controller, addressing up to 4Mbits of externally connected DRAM.

- **FX803 Audio Signalling Processor**

In-Band Audio Signal processing. 2-/5-/6-/Multi-Tone Selective Call encoding/decoding. Dual-Tone Multi-Frequency (DTMF) encoding.

- **FX805 Sub-Audio Signalling Processor**

Sub-Audio Tone (CTCSS) and Digitally Controlled Squelch (DCS) Signal processing.

- **FX806 Audio Processor**

Audio, Speech and Data processing, using selective-gain, VOGAD and filter stages. Multiplexing of other DBS 800 audio outputs providing a common drive to transmitter modulation stages.

- **FX809 FFSK Modem**

Intelligent 1200 baud data modulation/demodulation, compatible with MPT1317/1327 and other similar systems.

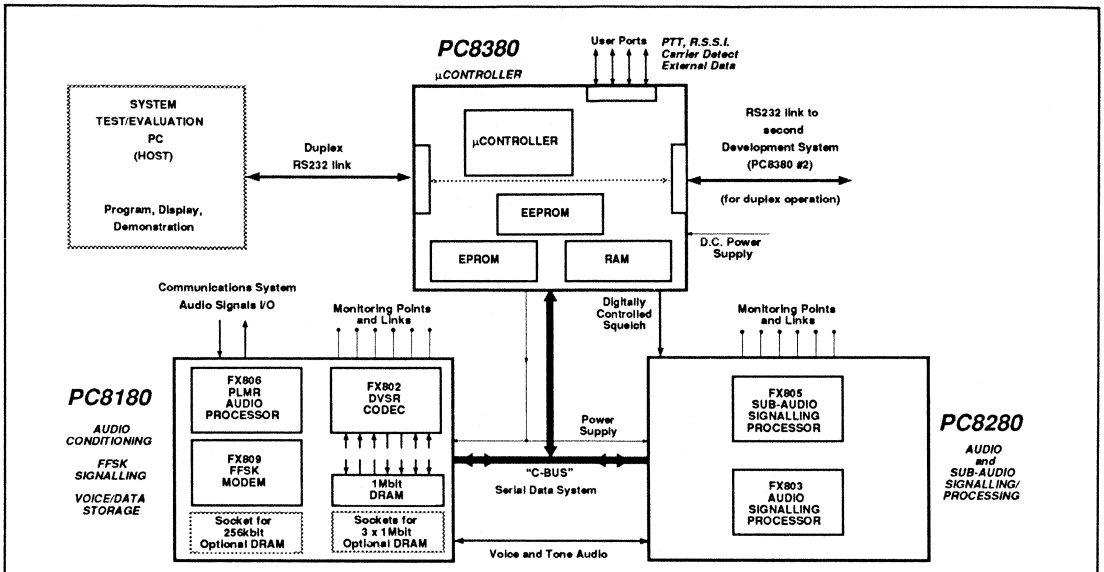
Management and operation of all system functions is under the control of a µProcessor. Communication and control is by means of a simple, two-way serial data system, the "C-BUS."

By this method, DBS 800 will fulfil the mandatory requirements of national communication specifications, such as CEPT, EIA, FTZ, MPT, as well as application-specific or system requirements.

To enable development and design with DBS 800, a Development System is provided, comprising printed circuit boards and operating software – thus ensuring that design time cycles are minimized.

All DBS 800 low-power 5-volt CMOS integrated circuits incorporate "Powersaving" modes to ensure maximum system efficiency.

# System Development




*DBS 800 "System Development" Hardware*

## DBS 800 Development System

A complete system designed to enable radio equipment designers to evaluate and design with DBS 800 integrated circuits.

The DBS 800 Development System is a combination of hardware and software. The hardware consists of 3 populated printed circuit boards described below:

- **PC8180**
  Audio Conditioning, Data/Voice Storage and Retrieval, FFSK Signalling. Provided on-board is the facility to install up to 4Mbit of optional DRAM.

- **PC8280**
  Audio and Sub-Audio Signal Processing.

- **PC8380**
  The development µController with supporting software and interface circuitry. Intended to run with an evaluation processor, this µController PCB can also be used stand-alone. The PC8380 will run integral PROM-based or modified/new example programmes. Additional user ports are provided to facilitate radio, communication functions and prompts; PTT, R.S.S.I., Carrier Detect, etc.

Monitor and test points are provided on all PCBs to enable ease of access to relevant data and audio signals. Each PCB has its own on-board Xtal/clock circuitry.

Development software is provided in EPROM and as example listings on floppy disk, and takes the form of:

- **Microcircuit Evaluation** Software
  Measurement and functional tests of DBS 800 devices. Enabling the designer to set-up, step-through and run evaluation tests.

- **System Demonstration** Software
  External control of development application programmes, running PMR based routines, such as; Audio Processing, Signalling, Voice Messaging, Data Storage and Transmission.

- **Design Application** Software
  Functional software and listings are provided to operate PMR orientated routines. From these the Mobile Radio designer is able to create application sub-routines for use in specific radio system projects.

The DBS 800 Development System, which contributes to faster evaluation and design cycles by providing total flexibilty in the investigation of PMR applications, ensures that the Mobile Radio designer can:

(1) Quickly evaluate the electrical performance of each individual microcircuit, and
(2) Demonstrate some of the new features offered by DBS 800, and
(3) Investigate usable Application Specific software routines in a high-level language, suitable for modification and translation to the ultimate choice of µController.

# System Applications

| Application | 802 | 803 | 805 | 806 | 809 | Example |
|---|---|---|---|---|---|---|
| ● **Direct Voice** All mandatory audio filtering, gain adjustment, VOGAD and limiter blocks required for audio signal processing within a PMR Radio. | | | | ■ | | Basic two-way radio, operating open channel with carrier squelch only. |
| ● **Voice Mailbox** (Open Channel) Receipt and storage of voice calls for instant replay. | ■ | | | ■ | | Taxi companies or Police to replay the last received message e.g. customer or incident address. |
| ● **Voice Mailbox** (Personal Call) Storage of selectively called voice message during unattended vehicle operation. | ■ | | | ■ | | Service engineer may receive information regarding the next call whilst away from the vehicle. |
| ● **Voice Status Announcement** Transponding a pre-recorded voice 'status' message when selectively addressed. | ■ | | | ■ | | Security companies can leave a recorded message in the vehicle as to their present location. |
| ● **Voice Alarm** Automatically transmit a pre-recorded voice message when externally triggered. | ■ | | | ■ | | Security vehicle under attack may send a distress message and a 'voice status' noting last known location. |
| ● **Voice Buffer** Storing speech temporarily until a transmission channel is free. Used to buffer speech during 'busy channel' periods or 'link establishment' delays encountered on Trunked and Common Base Station systems. | ■ | | | ■ | | Allows the operator to talk immediately, regardless if the transmission channel is free. The initial voice, once stored, is sent when the link is established. Squelch Tail elimination can be performed by delaying speech and muting the unwanted section. |
| ● **VOX** Voice Buffering allows speech to be delayed, allowing the VOX to operate with an effective ZERO attack time. | ■ | | | ■ | | Trunked systems with long 'link establishment' times can be operated "hands free" using 'buffered' VOX. |
| ● **Speech Delay** A fixed delay introduced into speech. (similar to 'voice buffering') | ■ | | | ■ | | 'Skip' play-back features or delay equalization of speech in 'Quasi-Sync' systems. |
| ● **Answering Machine Facility** A combination of Voice Status and Voice Mailbox applications to give a complete Answering Machine facility. | ■ | | | ■ | | Offers Trunked radio users similar voice messaging facilities to those available to Cellular radio users. |
| ● **Voice Security** (Time Domain) Digitising and scrambling voice information according to a cryptographic key code and then re-combining the scrambled digits into an analogue signal for onward transmission. Synchronization is achieved using the 1200 baud FFSK Modem. | ■ | | | ■ | ■ | Police, Military and other commercial applications requiring radio communications with no fear of eavesdropping. |

## System Applications .....

| Application | 802 | 803 | 805 | 806 | 809 | Example |
|---|---|---|---|---|---|---|
| **● Voice Compression**<br>Time compressing segments of speech for injection of signalling information into the inter-segment gaps. | ■ | | | ■ | ■ | Continuous ANI or synchronization systems for scramblers. Simultaneous transmission of data and speech over a standard 3000Hz bandwidth. |
| **● Pause Elimination**<br>Using VOX feature - store only "voiced" sounds for transmission. This method eliminates pauses and gaps in speech. | ■ | | | ■ | ■ | Efficient use of both the storage medium and the air time by sending the voice with short, standard length gap where required. |
| **● Two-Way Mobile Relay**<br>By storing speech, a half-duplex radio may be converted into a repeater station. Storing incoming voice for re-transmission when the message ends. | ■ | | | ■ | ■ | Temporary repeater function. "Over the hill" communication from a base station to a handheld radio via a mobile radio. |
| **● Mobile Data Transmission**<br>Transmission and Reception of data using a 1200 baud, or other speed modem. Faster data from or to an external peripheral may use the DVSR and memory to buffer data prior to transfer using the 1200 baud Modem product. | ■ | | | ■ | ■ | Connection of a 'laptop' PC dumping data at 19kbits/s to the radio's 1200 baud modem. Formatting, packeting and error correction/detection achieved by the µC whilst data is buffered in RAM using the DVSR product. |
| **● Sub-Audio Signalling**<br>Transmission and non-predictive detection of analogue or digital Sub-Audio signalling for Mobile and Trunked Radio. | | | ■ | ■ | | CTCSS –<br>Non-Predictive Decode and Encode<br>DCS – Digitally Coded Squelch<br>DPL™ – Motorola Digital Private Line<br>LTR™ – Logic Trunked Radio<br>Multi-standard squelch and repeater access schemes. |
| **● In-Band Tone Signalling**<br>Transmission and non-predictive detection of Selective Call or Single tone systems. Generation of DTMF or "Special" tones. | | ■ | | ■ | | Selcall – (CCIR, ZVEI {I, II and III} and EEA)<br>2-/5-/6-/Multi-Tone signalling<br>Dual Tone Multi-Frequency (DTMF) transmission<br>Group/All Call/Data/Status/ANI<br>Over-Air unit assignment/ reconfiguration<br>Special Tone generation/Reception<br>Radio Telemetry/Alarms |
| **● 1200 Baud Signalling**<br>Transmission and reception of data in the form of audio tones (1200Hz, 1800Hz) at 1200 baud. Checksum and Synchronization word provision and detection. | | | | ■ | ■ | 1200 Baud FFSK<br>MPT1317/1327 Trunked Radio signalling (Band III UK)<br>Data-Over-Air.<br>Mobitex, MCA, ANI, Scrambler Synchronization etc. |

**● Microcircuits**

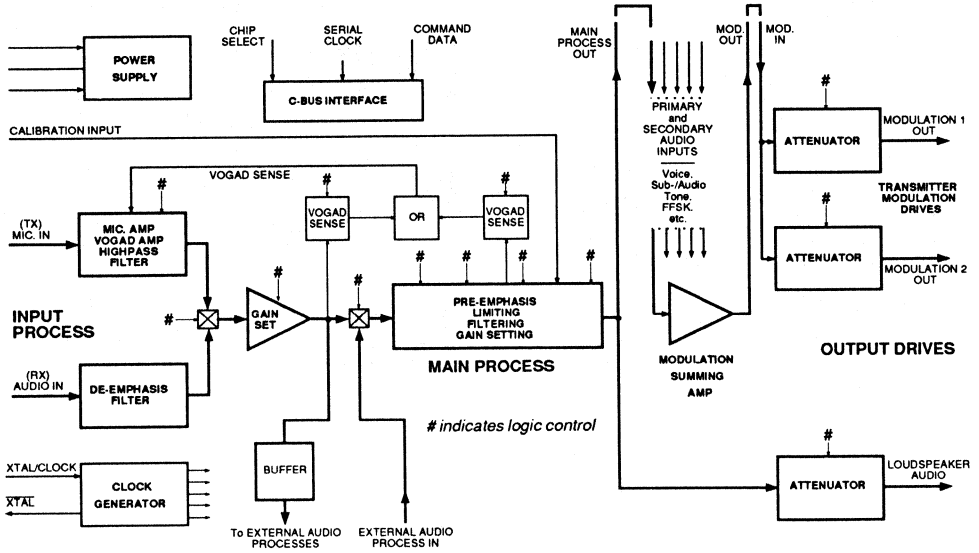
**FX802 DVSR Codec**
**FX803 Audio Signalling Processor**
**FX805 Sub-Audio Signalling Processor**
**FX806 Audio Processor**
**FX809 FFSK Modem**

**● Key:**

■ Recommended microcircuits required to achieve the illustrated application.

□ Alternative signalling options.

# FX806A
# Audio Processor




*FX806 – Audio Processor*

## FX806A Audio Processor

All DBS 800 system signal conditioning and filtering requirements for both transmit and receive paths are carried out by this half-duplex audio processor.

In transmit the FX806 conditions input voice-band audio and combines this with in-band/sub-audio signalling and data for transmitter modulation. The FX806 in receive processes audio from the radio discriminator for presentation to the loudspeaker drive circuitry.

The signal path of the FX806 can be divided into three sections:

- **Input Process**

  This stage has a selectable transmit and receive path. Transmit signals pass through microphone pre-amplifier, VOGAD and highpass filter stages. The receive audio passes through a de-emphasis stage.
  This initial audio, after gain adjustment, may be switched to external audio processes (such as scrambling) or the Main Process block.

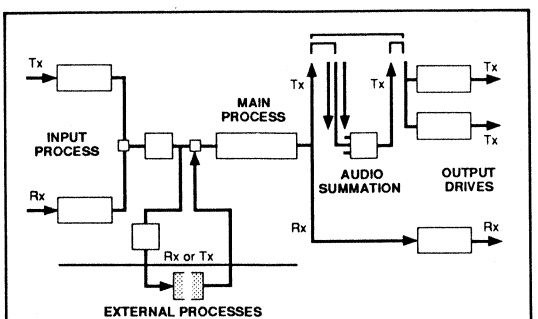
- **Main Process**

  Conditioning for the input or external process signals. Comprising pre-emphasis, high and lowpass switched-capacitor filtering and a deviation limiter. Conditioned audio is now presented to the output stages.

- **Summation and Output Drives**

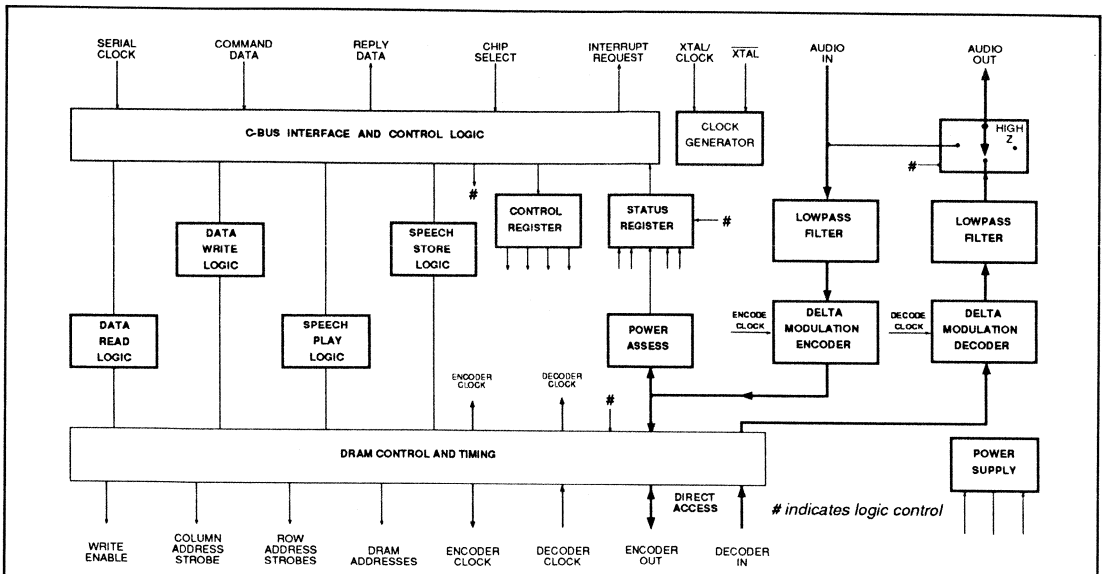
  Main audio for transmission is combined with signalling and data from external sources to provide the transmitter modulation drives. Received audio is level adjusted for output to loudspeaker circuitry.

FX806 circuit elements and signal paths are controlled and digitally adjusted by the µController using the "C-BUS" protocol.
Signal levels can therefore be dynamically controlled offering 'dynamic-compensation' for factors such as, temperature drift, VCO non-linearity etc.




*Audio Flow*

# FX802
# DVSR Codec




*FX802 – DVSR Codec*

## FX802 Data/Voice Storage Codec (DVSR)

A Continuosly Variable Slope Delta Modulation encoder and decoder with the abilty to store, retrieve and control data within external Dynamic Random Access Memory (DRAM). This microcircuit includes, on-chip, all address and refresh circuitry for control of up to 4Mbits of external DRAM.

The FX802 has four primary functions:

- **Speech Digitization**
  Digitally encoding an analogue (voice) input signal and presenting the resulting bit stream for output as a digital signal.
- **Speech (Data) Decoding**
  Producing an analogue (voice) signal from an input digital bit stream.
- **Data Storage**
  Storing in DRAM, either encoded speech data or data loaded from "C-BUS."
- **Data Recovery**
  Recovery of data from DRAM for output to either the Delta Decoder or the µController via "C-BUS."

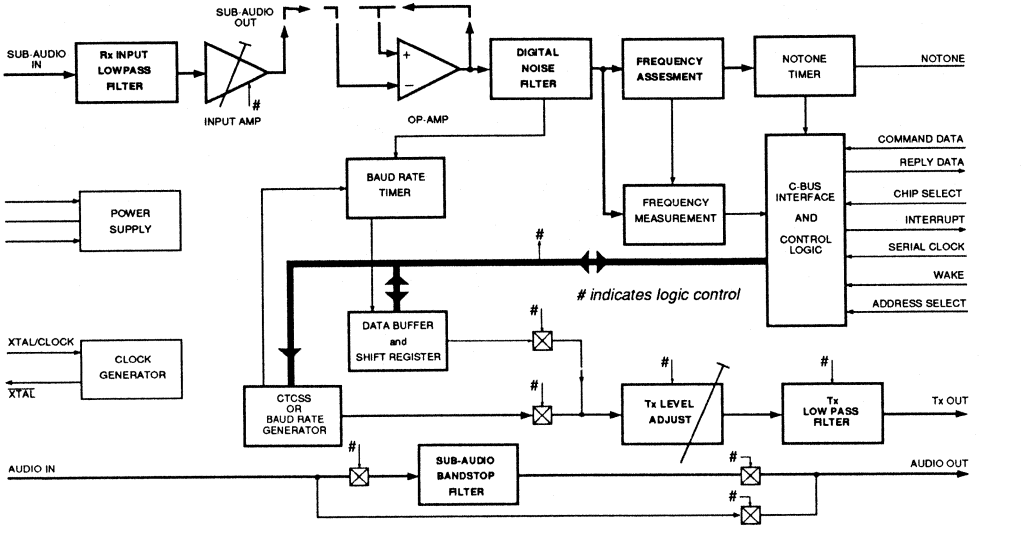
Encoded speech is available for transmission or storage in the connected DRAM. Input (speech-band) data from either the received signal or DRAM, is decoded, shaped and available for output to loudspeaker circuitry via the Audio Processor.

On-chip, the Delta Codec is supported by; input and output analogue switched-capacitor filters, switching control circuitry, input analogue power assessment circuitry (for pause-management or VOX systems) and DRAM control (refresh and timing logic).

The storage, recovery and replay functions of this device are ideal for "Time Domain Scrambling," "Temporary Voice (Busy) Buffering," "Answering Machine" and "Temporary Data Storage (fast in – slow out to the FX809 FFSK Modem)" applications. A Force Idle instruction provides a 10101010.....1010 perfect idle pattern to the decoder input.

"C-BUS" commands can be 'buffered' (stored temporarily) to allow instruction continuity.

# FX805 Sub-Audio Signalling Processor




*FX805 – Sub-Audio Signalling Processor*

## FX805 Sub-Audio Signalling Processor

A sub-audio frequency signalling processor to provide an outband audio and digital signalling facility for PMR radio systems.

This half-duplex device, which caters for the transmission and non-predictive reception of:

- Continuous Tone Controlled Squelch (CTCSS) tones and other non-standard frequencies.
- Digitally Coded Squelch – DCS/DPL™.

comprises:

- A non-predictive CTCSS Tone Decoder and DCS demodulator.
- A CTCSS/DCS Tone Encoder with Tx level adjustment and lowpass filter output stage.
- A selectable sub-audio bandstop filter.

The CTCSS tone data for transmission is loaded to this device, via "C-BUS," encoded and output from the Tx Lowpass filter.

Received non-predicted CTCSS input tone frequencies are measured and the resulting data presented to the µController for matching against a 'look-up' table.

Noise filtering is provided to improve the signal quality prior to measurement.

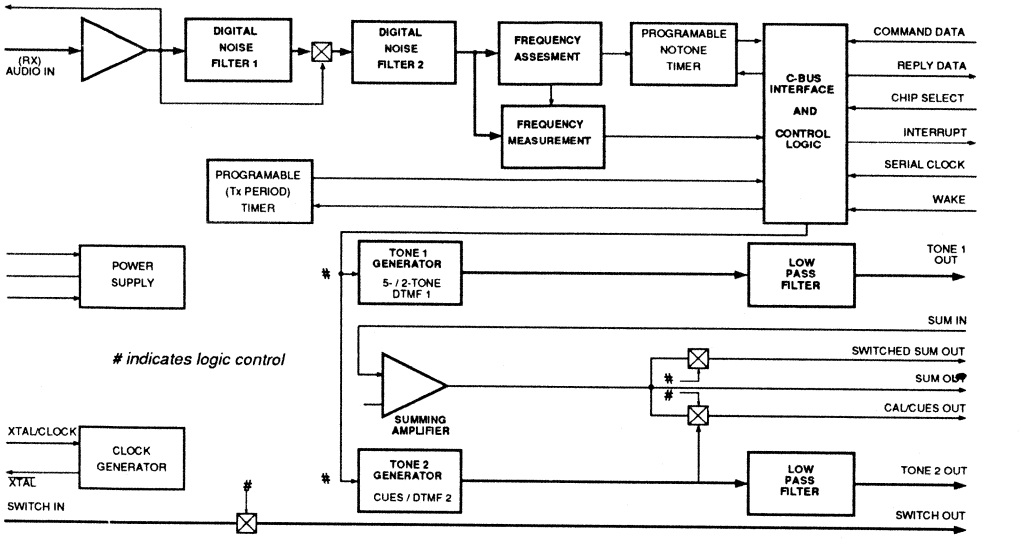
DCS coded data for transmission is loaded to the shift register and output, in bytes, through the tone output circuitry as sub-audio frequencies. DCS coding is produced by the µController.

Received DCS frequencies are filtered, detected and transfered in bytes from the shift register to the µController for decoding by software. Clock extraction circuitry is provided on chip.

Provision is made in both hardware and system software allocations to address two FX805 Sub-Audio Signalling Processors consecutively to achieve full-duplex operation.

Powersaving may be controlled by software or a dedicated input.

# FX803 Audio Signalling Processor




*FX803 – Audio Signalling Processor*

## FX803 Audio Signalling Processor

An audio signalling processor to provide an inband tone signalling facility for PMR radio systems. Signalling systems supported include selcall (CCIR, ZVEI I, II and III, EEA), 2-tone selcall and DTMF encode.

Using a non-predictive decoder and versatile encoder gives the FX803 the capability to work in any standard or non-standard tone system.

This full-duplex device consisting of;

- A tone decoder with programmable NOTONE timer.
- Two individual tone encoders and a programmable (Tx) period timer.
- An on-chip summing amplifier

For use with Single Tone or Selective Call systems.

Under the control of the µController, via "C-BUS," the FX803 will encode and transmit 1 or 2 audio tones simultaneously, and detect, decode and indicate the frequency of the non-predicted input tones. The transmit frequency range available is 208Hz to 3kHz and the receive frequency range is 313Hz to 6kHz.

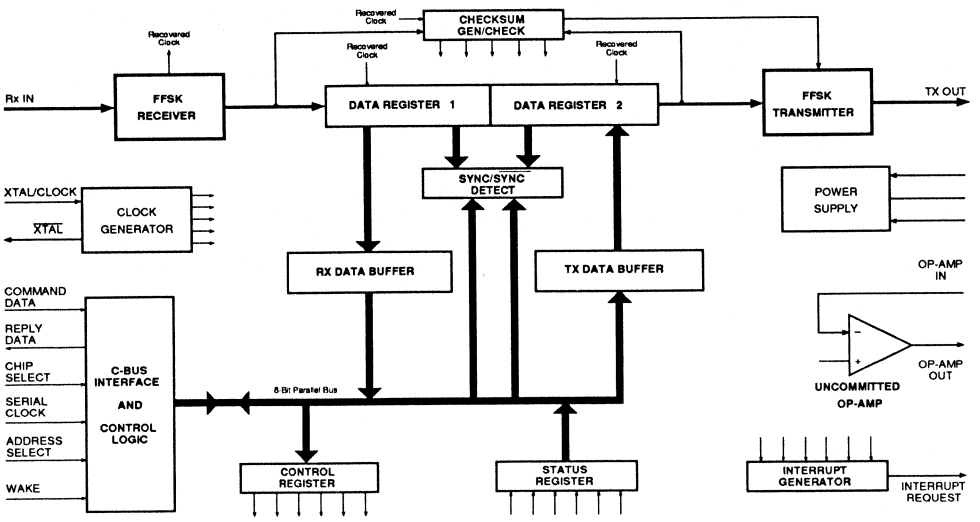
The output frequencies are produced from data loaded to the device, with the tone transmit period indicated by the programmable on-chip timer.

A Dual Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This is also available for level correction.

Tones produced by the FX803 can be used in the system as modulation calibration inputs and as "CUE" audio indications to the operator.

Received tones are measured and their frequency indicated to the µController in the form of a received data word. A poor quality or incoherent tone will indicate NOTONE.

# FX809
# FFSK Modem




*FX809 – 1200 Baud FFSK Modem*

## FX809 FFSK Modem

An intelligent, half-duplex, 1200 baud FFSK/MSK modem which under "C-BUS" control can transmit and receive data directly input. In addition this modem provides automatic checksum generation and error checking, in accordance with MPT1327, with the facility to load a customer-specific synchronization word.

Fully "C-BUS" compatible, this device, using Interrupt and Status Register procedures, will load and transmit preamble, synchronization and 8-bit data words (bytes) producing a 16-bit checksum if instructed.

In the Receive mode synchronization (SYNC) word detection is carried out, and received data bytes made available to the "C-BUS interface. Received input tones are demodulated in the FFSK Receiver and placed as 8-bit words into the Rx Data Buffer for transfer to the serial Reply Data line.

Information (data) for transmission is written to the Tx Data Buffer from the Command Data line, to be modulated as 1200Hz (logic "1") and 1800Hz (logic "0") tones.

Checksum generation (Tx) and checking (Rx) is enabled by software control.

Provision is made in the FX809 and "C-BUS" protocol to address 2 x FX809 Modems consecutively to produce "full-duplex" data operation.

The FX809 has a non-committed Op-Amp on-chip for general applications in the DBS 800 "cluster."

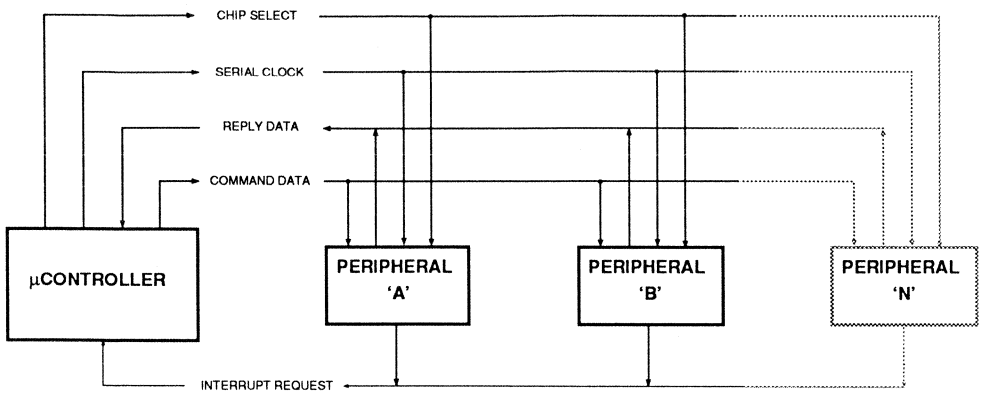
This modem is designed to interrupt (the µController) for the following events:

*Received Data Ready*
*Transmit Data (Buffer) Ready*
*SYNC Detected*
*$\overline{\text{SYNC}}$ Detected*
*Transmitter Idle*

Input timing is carried out by a 1200 baud clock recovered from the input bit stream and the output tones timed to the transmit clock. On-Chip filter, register clocks and tone frequencies are derived from an external Xtal or clock input.

Interrupt, SYNC Detection and Checksum functions can be enabled or disabled by software commands.

# "C-BUS" Serial Interfacing




*The "C-BUS" Hardware Concept*

## "C-BUS"

The software and hardware interface for all members of the DBS 800 family. "C-BUS" enables the serial, bi-directional transfer of commands and data throughout the system, allowing total flexibility of operational control and data handling. System upgrades can be achieved by a simple software or firmware change.

### Hardware Interface

Physically, the Bus consists of 5 lines as described below:

- **"Serial Clock"** – Driven by the µController to all peripherals. All "C-BUS" commands and data transfers are synchronized to this clock.
- **"Command Data"** – to Address/Command and transfer data from µController to an addressed peripheral, in serial format.
- **"Reply Data"** – transfer of "requested (commanded)" data from an addressed peripheral, in serial format.
- **"Chip Select" (CS)** – carrying the CS timing command to the peripheral, from the µController. DBS 800 audio microcircuits are designed to work with a common CS line, using the Address/Command as a chip identifier. Transfer sequences are initiated, completed or aborted by the CS signal.
- **Interrupt Requests (IRQ)** – interactive peripheral devices have an output for connection to the µController Interrupt input.

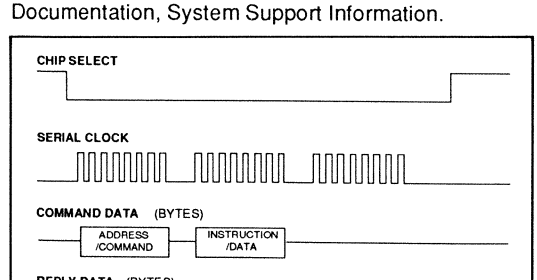
All future DBS 800 integrated circuits will be "C-BUS" compatible.

### Software and Protocol

"C-BUS" protocol consists of 3 categories of transaction:

- **"Address/Command"**
  *i.e. Modem X – Enable Tx.*
- **"Address/Command, and data byte/s"**
  *i.e. DVSR – Write to Tx Data Buffer – 'n' data byte/s.*
- **"Address/Command (Request) and reply data bytes"**
  *i.e. Modem X – Read Rx Data Buffer – 'n' data byte/s.*

A complete description of all "C-BUS" Address/Commands is provided in Document 2 of the DBS 800 Documentation, System Support Information.




*A Typical "C-BUS" Transfer*

# Controlling System

## "C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's PLMR microcircuits — The FX802, FX803, FX805, FX806 and FX809.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

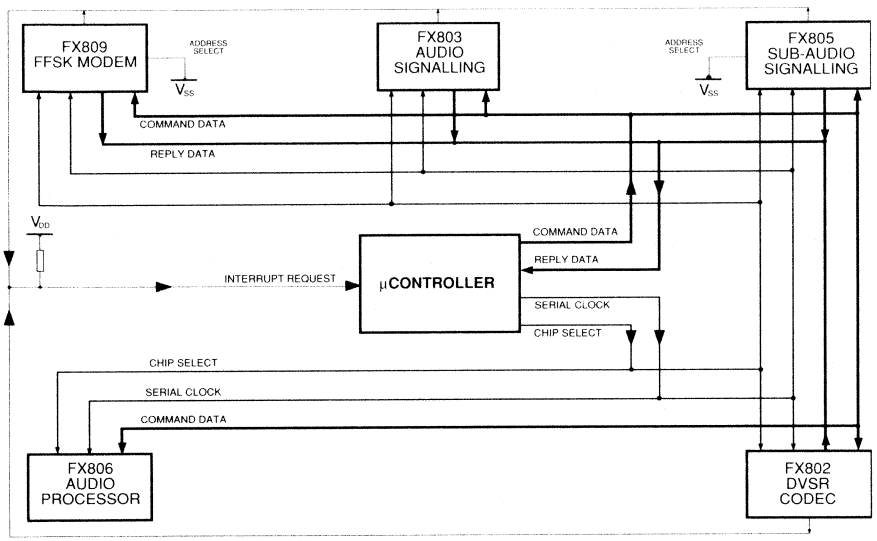



*Fig.1 Example "C-BUS" Hardware Interconnections*

### "C-BUS" Hardware Interface

Physically, the "BUS" consists of the 5 lines shown in Figure 1 and described below:

- **"Serial Clock" line** – driven by the µController and connected to all DBS 800 microcircuits.
- **"Command Data" line** – driven by the µController and connected to all DBS 800 microcircuits.
- **"Reply Data" line** – connected to the µController and driven by the 3-state outputs of relevant DBS 800 microcircuits.
- **"$\overline{\text{Chip Select}}$" ($\overline{\text{CS}}$) line** – driven by the µController and connected to all DBS 800 microcircuits.
- **"$\overline{\text{Interrupt Request}}$" ($\overline{\text{IRQ}}$) line** – interactive DBS 800 microcircuits have a 'wire-or'-able Interrupt Request output (IRQ) for connection to the µController's Interrupt input.

Publication D/800/Sys/2 December 1991

### Configurations for Full-Duplex Signalling

Figure 2 shows how two FX809 FFSK Modems may be connected to the "C-BUS" to provide full-duplex FFSK signalling. Two FX805 Sub-Audio Signalling Processors may be connected in a similar manner when full-duplex sub-audio and NRZ signalling is required.

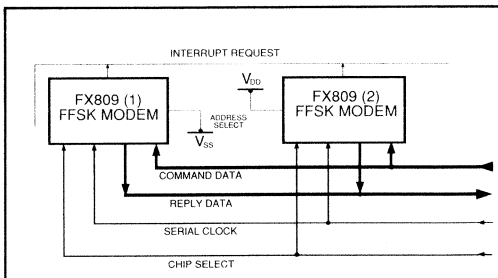



*Fig.2 FX809 Modems for Full-Duplex Operation*

# Controlling Protocol

## The Use of "C-BUS" Software and Protocol

Each individual DBS 800 Data Sheet contains a table listing the "C-BUS" commands and instructions relevant to that peripheral. Table 1 gives an abridged list of all DBS 800 Address allocations. All "C-BUS" data transfer is based on the serial transmission of 8-bit bytes, sent to the BUS MSB (bit 7) first, LSB (bit 0) last, and synchronized to a burst of 8 Serial Clock pulses generated by the µController.

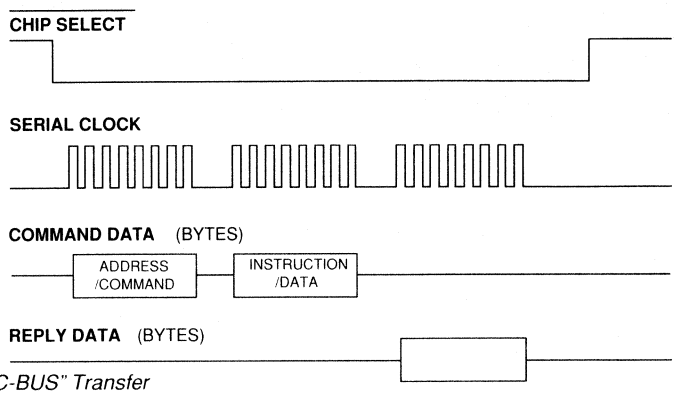



*Fig.3 A Typical "C-BUS" Transfer*

### Address/Command (A/C) Byte

Under the "C-BUS" protocol, this byte is the first to be transmitted on the Command Data line after the Chip Select line becomes active (logic "0"), and is an 'Address' specifying which chip is selected for a particular "C-BUS" transaction.

A particular chip may recognise more than one address. Each address recognised by a chip signifies a particular command.

Three types of "C-BUS" transaction are possible:

**A** Transmission of a single Address/Command byte.

**B** Transmission of an Address/Command byte followed by one or more Command Data bytes.

**C** Transmissions of an Address/Command byte (plus possibly one or more data bytes) resulting in one or more Reply bytes being sent back from the selected DBS 800 microcircuit to the µController.

With the Chip Select line being used to define the beginning and end of each transaction. The Timing Diagrams (Figures 4 and 5) show the transfer procedure.

When transaction types 'B' or 'C' involve the transmission of more than one data byte, then the Most Significant data Byte is transmitted first, the Least Significant data Byte last.

### System Addressing

Table 1 (a) shows the present allocation of Address/Command byte values to "C-BUS" compatible chips, some Address/Command byte values have been reserved for specific general commands such as General Reset and "C-BUS" performance testing. These particular values may be recognised by more than one chip.

In general, however, the exact effect of an Address/Command byte value will depend on the detailed specification for the particular DBS 800 microcircuit, and are explained in detail in the relevant current DBS 800 Data Sheet.

### Command Data Bytes to DBS 800 Microcircuits

Under the "C-BUS" protocol, the Address/Command byte sent from the µController may be followed by one or more data bytes to be loaded into register(s) on the selected DBS 800 microcircuit (transactions type 'B' and "C").

The exact number, destination and effect of these data bytes is determined by the Address/Command byte value and the specification of the particular peripheral microcircuit.

The µController must always transmit the correct number of data bytes - as each byte is received by the peripheral it may have an immediate effect, or may not take effect until the Chip Select line goes high (inactive), (see Timing Figures 4 and 5) at the end of the transaction, depending on the specification for that particular peripheral microcircuit.

### Reply Data Bytes from DBS 800 Microcircuits

Are transmitted from the selected DBS 800 peripheral to the µController and are clocked into the µController when the Serial Clock is 'high.'

Under the "C-BUS" protocol, the format of the Address/Command byte may request that the selected chip responds by sending one or more Reply Data bytes to the µController (transaction type 'C').

The exact number, source, and meaning of these byte(s) is determined by the Address/Command byte value and the specifications of the particular peripheral microcircuit.

The transmission of each byte from the peripheral microcircuit is governed by the Serial Clock pulse generated by the µController. In some cases, the µController may not wish to read-in all of the bytes which the peripheral would normally expect to transmit. In these cases, the µController will raise the Chip Select line to a high (inactive) level as soon as it has read in sufficient bytes, and on detecting the Chip Select line going high the peripheral microcircuit will abort its transmission sequence.

## Controlling Protocol...

### The Use of "C-BUS" Software and Protocol .....

#### Serial Clock Pulses

Are generated by the µController to synchronize the transfer of data bits between the µController and DBS 800 microcircuits as illustrated in Figures 3, 4 and 5. For each 8-bit byte, Command or Reply, the µController must generate 8 Serial Clock pulses taking into account the inter-byte period ($t_{NXT}$).

To allow for differing µController capabilities, "C-BUS" compatible ICs are able to work with either 'polarity' of Serial Clock, ie. the Serial Clock line may be at a 'high' or a 'low' level at the start of each transaction, as long as:

(i) Data sent from the µController is clocked into the DBS 800 ICs on the rising edge of the Serial Clock pulses.

(ii) Reply Data sent from a DBS 800 IC to the µController is clocked into the µController when the Serial Clock is 'high.'

#### "C-BUS" Serial Clock Rate

Generally "C-BUS" Serial Clock rates that are harmonically related to the 'XTAL/CLOCK ÷ 32'–FREQUENCY cannot produce alias effects within a microcircuit, therefore employment of a "C-BUS" Serial Clock rate at this frequency is preferable.

If it proves impractical to select a synchronous "C-BUS" clock, coupling between sensitive analogue inputs (such as the FX806 Mic. inputs) and the "C-BUS" should be avoided.

#### Chip Select ($\overline{CS}$)

Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. This input, provided by the µController to all DBS 800 microcircuits, is active at a logic "0" and inactive at a logic "1." See Figure 4.

## "C-BUS" Specifications

### Operating Limits

All "C-BUS" characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5 Volts d.c. $T_{AMB}$ = 25°C. Reply Data Line loaded with 50pF//200kΩ to $V_{SS}$.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Logic Levels | | | | | |
| Logic "1" | 1 | 3.5 | – | – | V |
| Logic "0" | 1 | – | – | 1.5 | V |
| $I_{IN}$ (logic "1" or "0") | 1 | – | – | 1.0 | µA |
| Output Logic Levels | | | | | |
| Logic "1" (-120µA) | 2 | 4.6 | – | – | V |
| Logic "0" (360µA) | 3 | – | – | 0.4 | V |
| $I_{Out}$ Tristate (logic "1" or "0") | 3 | – | – | 4.0 | µA |
| Input Capacitance | 1 | – | – | 7.5 | pF |
| IOX ($V_{Out}$ = 5V) | 4 | – | – | 4.0 | µA |

#### Notes

1. Serial Clock, Command Data and Chip Select inputs.
2. Reply Data output.
3. Reply Data and IRQ outputs.
4. Leakage current into the "Off" IRQ output.

# Controlling Protocol...

## "C-BUS" Addressing

To assist in the efficient use of "C-BUS" and System addressing, Table 1 shows the distribution of the DBS 800 Address allocations.

**(a) "C-BUS" Address Listing** – "C-BUS" Addresses (HEX) currently allocated to DBS 800 microcircuits

| | |
|---|---|
| "C-BUS" Performance Testing | 00 |
| General (all device) Reset | 01 |
| **Audio Processor** | **FX806** |
| Control Command | 10 |
| Mode Command | 11 |
| Modulator Levels Set | 12 |
| Volume Set | 13 |
| **Audio Signalling Processor** | **FX803** |
| Write to Control Register | 30 |
| Read Status Register | 31 |
| Read Rx Tone Frequency | 32 |
| Write to NOTONE Timer | 33 |
| Write to Tx Tone Generator 1 | 34 |
| Write to Tx Tone Generator 2 | 35 |
| Write to G/Purpose Timer | 36 |
| **FFSK Modem 1** | **FX809** |
| Write to Control Register | 40 |
| Read Status Register | 41 |
| Read Rx Data Buffer | 42 |
| Write to Tx Data Buffer | 43 |
| Write to Sync Program | 44 |
| **FFSK Modem 2** | **FX809** |
| Write to Control Register | 48 |
| Read Status Register | 49 |
| Read Rx Data Buffer | 4A |
| Write to Tx Data Buffer | 4B |
| Write to Sync Program | 4C |
| "C-BUS" Performance Testing | 55 |

| | | | |
|---|---|---|---|
| **DVSR Codec** | | | **FX802** |
| Write to Control Register | | | 60 |
| Read Status Register | | | 61 |
| Store 'N' pages, | Start page 'X' | (immediate) | 62 |
| Store 'N' pages, | Start page 'X' | (buffered) | 63 |
| Play 'N' pages, | Start page 'X' | (immediate) | 64 |
| Play 'N' pages, | Start page 'X' | (buffered) | 65 |
| Write Data, | Start page 'P' | | 66 |
| Read Data, | Start page 'P' | | 67 |
| Write Data, | Continue | | 68 |
| Read Data, | Continue | | 69 |
| **Sub-Audio Signalling Processor 1** | | | **FX805** |
| Write to Control Register | | | 70 |
| Read Status Register | | | 71 |
| Read CTCSS Rx Data | | | 72 |
| Write to CTCSS/NRZ Tx | | | 73 |
| Read NRZ Rx Data | | | 74 |
| Write to NRZ Data Tx | | | 75 |
| Write to Gain Set | | | 76 |
| **Sub-Audio Signalling Processor 2** | | | **FX805** |
| Write to Control Register | | | 78 |
| Read Status Register | | | 79 |
| Read CTCSS Rx Data | | | 7A |
| Write to CTCSS/NRZ Tx | | | 7B |
| Read NRZ Rx Data | | | 7C |
| Write to NRZ Data Tx | | | 7D |
| Write to Gain Set | | | 7E |
| "C-BUS" Performance Testing | | | AA |
| "C-BUS" Performance Testing | | | FF |

**(b) Reserved Addresses** – "C-BUS" Addresses (HEX) reserved for future DBS 800 microcircuit/system use

| | | | | | |
|---|---|---|---|---|---|
| General Functions | 02 | to | 07 | Future Sub-Audio Signalling Processors | 77 |
| Future Audio Processors | 14 | to | 1F | Future Sub-Audio Signalling Processors | 7F |
| Future Speech Products | 20 | to | 2F | Future Products | 80 to 8F |
| Future Audio Signalling Processors | 37 | to | 3F | Future Products | 90 to 9F |
| Future FFSK Modems | 45 | to | 47 | Future Products | D0 to DF |
| Future FFSK Modems | 4D | to | 4F | Future Products | E0 to EF |
| Future DVSR Codecs | 6A | to | 6F | | |

**(c) Spare Addresses** – "C-BUS" Addresses (HEX) that will not be allocated for DBS 800 microcircuit/system use and are available for custom use

| | | | |
|---|---|---|---|
| 08 to 0F | 50 to 54 | 56 to 5F | A0 to A9 |
| AB to AF | B0 to BF | C0 to CF | F0 to FE |

*Table 1 DBS 800 "C-BUS" Address Allocations*

### "C-BUS" Performance Testing

To enable the effect of "C-BUS" activity on audio microcircuit noise levels to be assessed 4 addresses are allocated for "C-BUS" performance testing:

| | | |
|---|---|---|
| $00_H$ | 0 0 0 0 0 0 0 0 | – all 0's |
| $55_H$ | 0 1 0 1 0 1 0 1 | – bit reversals |
| $AA_H$ | 1 0 1 0 1 0 1 0 | – bit reversals |
| $FF_H$ | 1 1 1 1 1 1 1 1 | – all 1's |

These 'Performance' Address/Command bytes, when following an active Chip Select are ignored by the DBS 800 chip-set.

## Controlling Protocol...

### "C-BUS" Timing Information

Figure 4 shows the timing parameters for two-way communication between the µController and DBS 800 peripherals on the "C-BUS." Figure 5 shows the timing relationships between the Serial Clock and Data.

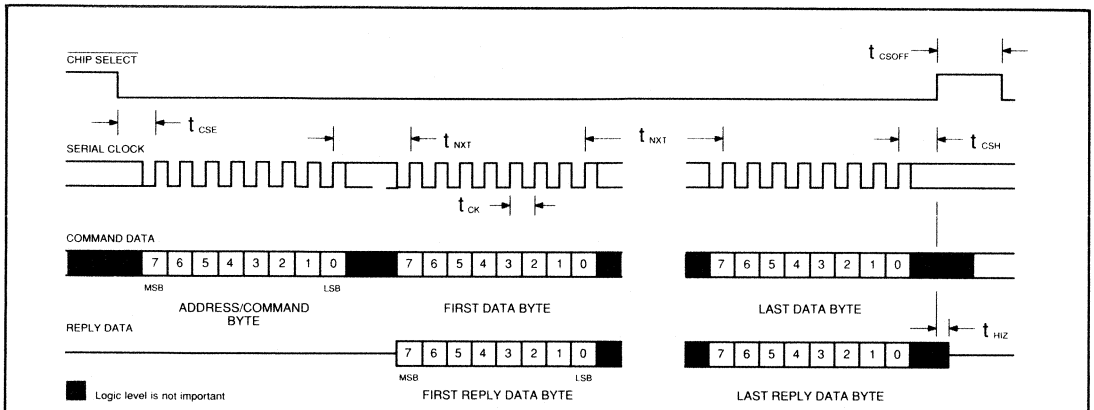



*Fig.4 "C-BUS" Timing Information*

*NOT TO SCALE*

Timing Specification – Figures 4 and 5

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CSE}$ | "CS-Enable to Clock-High" | 1 | 2.0 | – | – | µs |
| $t_{CSH}$ | Last "Clock-High to CS-High" | 1 | 4.0 | – | – | µs |
| $t_{HIZ}$ | "CS-High to Reply Output Tri-state" | | – | – | 2.0 | µs |
| $t_{CSOFF}$ | "CS-High" Time between transactions | 1 | 2.0 | – | – | µs |
| $t_{CK}$ | "Clock-Cycle" Time | 1 | 2.0 | – | – | µs |
| $t_{NXT}$ | "Inter-Byte" Time | 1 | 4.0 | – | – | µs |
| $t_{CH}$ | "Serial Clock-High" Period | | 500 | – | – | ns |
| $t_{CL}$ | "Serial Clock-Low" Period | | 500 | – | – | ns |
| $t_{CDS}$ | "Command Data Set-Up" Time | | 250 | – | – | ns |
| $t_{CDH}$ | "Command Data Hold" Time | | 0 | – | – | ns |
| $t_{RDS}$ | "Reply Data Set-Up" Time | | 250 | – | – | ns |
| $t_{RDH}$ | "Reply Data Hold" Time | | 50.0 | – | – | ns |

**Notes**

1. These Minimum "C-BUS" Timing values are altered during operation of the FX802 DVSR Codec.
2. When addressing DBS 800 microcircuits on the "C-BUS," always use the information published in current Data Sheet documents.

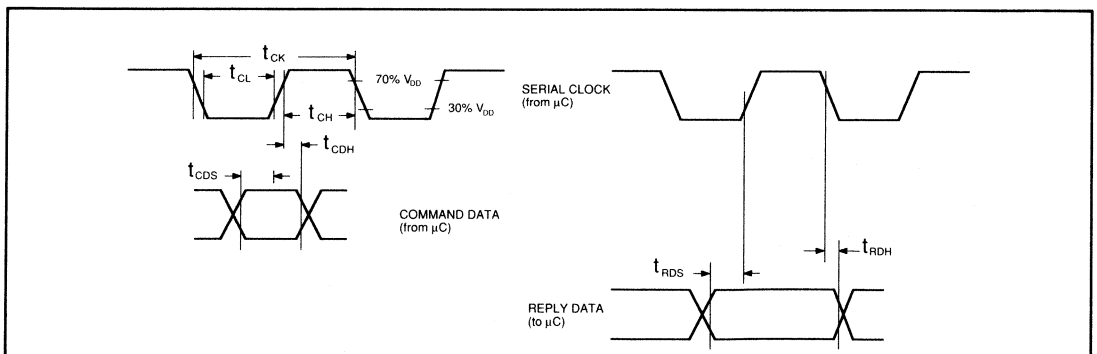



*Fig.5 "C-BUS" Timing Relationships*

*NOT TO SCALE*

# System Audio Interconnections

Figure 6 gives an example of DBS 800 microcircuit transmit and receive audio paths and interconnections.

External components shown are those recommended in the individual Data Sheet documents. Components identified by an "S" are viewed in this diagram as System Components, which are calculated to perform a specific function within the overall DBS 800 audio system. Table 2 shows recommended System Component values together with brief notes on their calculation.

| System Component | Recommended Value | Remarks – *with reference to Figure 6* |
|---|---|---|
| $SC_1$<br>$SC_2$<br>$SC_3$ | See Remarks | These capacitor values should be chosen with regard to the desired frequency response and input impedances of the modulation and loudspeaker amplifier circuits. |
| $SR_1$ | 100kΩ | The feedback resistor of the FX806 Modulation Summing Amplifier. This amplifier satisfies the input gain and matching requirements of the remaining DBS 800 devices. |
| $SR_2$ | 1.0MΩ | Chosen, in conjunction with $SR_1$, to provide a sub-audio signal level of -20.0dB to the Modulator. |
| $SR_3$<br>$SR_4$ | 100kΩ<br>100kΩ | Chosen, in conjunction with $SR_1$, to present audio and in-band signalling levels of 0dB to the Modulator. |
| $SR_5$ | 100kΩ | The feedback resistor of the FX803 Summing Amplifier. This amplifier regulates the signal level output of Tone Generators 1 and 2 which in turn are input to the Transmit Audio BUS by Switch 2 and $SR_4$. |
| $SR_6$<br>$SR_7$ | 82.0kΩ<br>120kΩ | Chosen, in conjunction with $SR_5$, to produce a 3.0dB tone-differential (twist) when the FX803 is employed as a DTMF decoder. For selcall applications different output levels may be required, or the signal level from Tone Generator 1 attenuated by the FX806 Modulator Drivers. |
| $SR_8$ | 100kΩ | Chosen, in conjunction with $SR_1$, to provide an FFSK signalling level of 0dB to the Modulator. |

*Table 2 Recommended "System Component" Values*

**Notes** – *with reference to Figure 6*

(1) The Audio Switch (Sw1) of the FX803 is used, in this example application, to allow interruption of the transmitter modulation path if it is required to provide a CUE (beep) from the tone generator to the loudspeaker.

(2) To demonstrate the versatility of the FX806 microphone input stage, microphone input components are shown in a single-ended configuration. The current FX806 Data Sheet shows a differential input configuration. Relevant component values are the same for both applications.

(3) It is recommended that, to improve screening and reduce noise levels around DBS 800 microcircuits, any unused pins are connected to $V_{SS}$. This includes inputs to on-chip amplifiers and switches if not employed within an application.

(4) Table 3 gives a guide to the relevant signal levels used in the DBS 800 System.

| Signal Level (dB) | Amplitude (mVrms) | Tx Deviation (%) |
|---|---|---|
| -30.0 | 9.7 | |
| -20.0 | 30.8 | |
| -15.5 | 51.3 | 10 |
| -9.6 | 102 | 20 |
| -6.0 | 154 | 30 |
| -3.5 | 205 | 40 |
| -1.6 | 256 | 50 |
| 0 | 308 | 60 |
| 1.3 | 359 | 70 |
| 2.5 | 410 | 80 |
| 3.5 | 462 | 90 |
| 4.4 | 513 | 100 |

*Table 3 Audio Signal Levels*

## System Audio Interconnections...

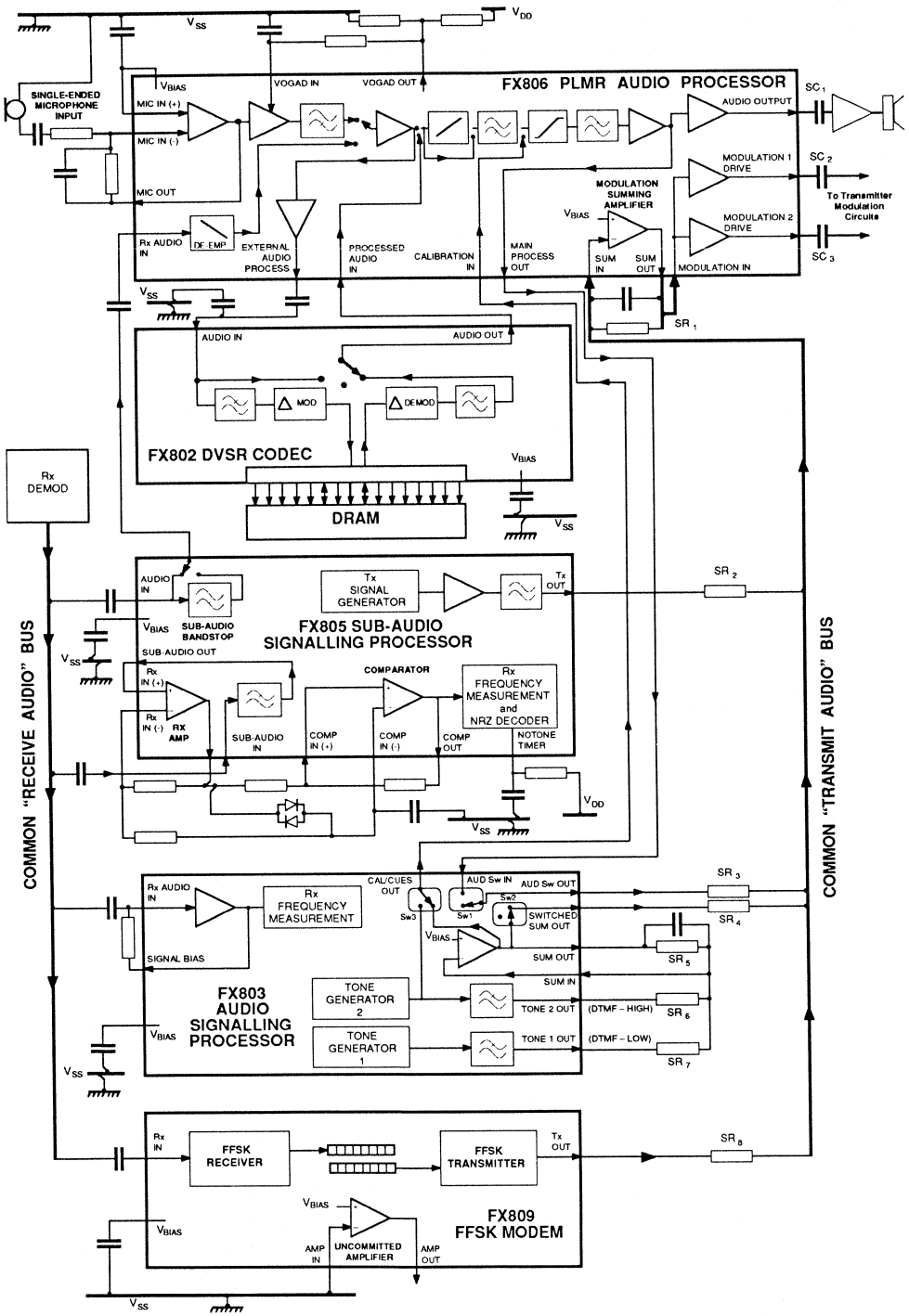



*Fig.6 Example "DBS 800 System" Analogue Signal Connections*

# Application Information

## Xtal Oscillator Circuits

These Application Notes, which are derived from CML Application Note *D/XT/1 April 1986*, discuss a general Xtal oscillator circuit applicable to most individual CML microcircuits, and a recommended oscillator configuration that can be used with the DBS 800 Series microcircuits.

Figure 7 shows the standard Xtal oscillator circuit from which most recommended Data Sheet circuits, including DBS 800, are derived.

The standard on-chip CML CMOS oscillator circuit will function correctly with the majority of Xtals, however the use of this circuit with a few Xtal types may cause the following problems:

1 Excessive drive level to the Xtal.

2. Excessive over-voltage, outside the device maximum ratings, at the oscillator input pin. This over-voltage may show itself as degraded microcircuit performance.

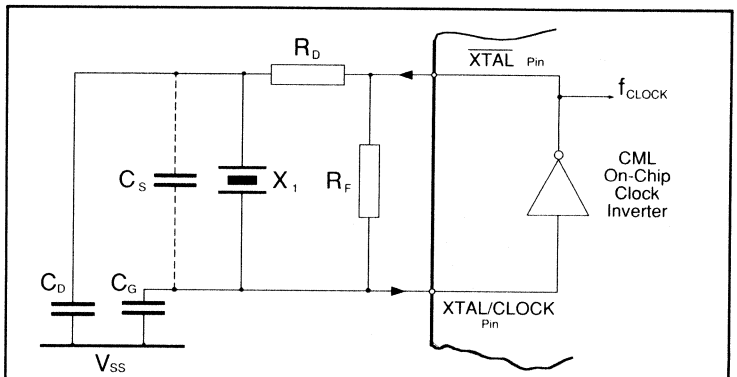



*Fig.7 Standard Xtal Oscillator Circuit*

## Standard Xtal Oscillator Components

**$R_F$ Feedback Resistor**

To set the bias point of the internal amplifier. Low values of $R_F$ will reduce loop-gain and disturb the phase of the feedback network. *Typical value = 1.0MΩ ± 20% in a range of 1.0MΩ to 20MΩ.* In the DBS 800 series, this resistor is included within the FX806.

**$R_D$ Drive Resistor**

Used to limit the Xtal drive level by forming a voltage-divider between $R_D$ and $C_D$. $R_D$ also stabilizes the oscillator against changes in the output impedance of the inverter. To verify that the maximum operating supply voltage does not overdrive the Xtal, observe the output frequency as a function at the buffered output. Under proper operating conditions the frequency should increase slightly (a few ppm) as the supply voltage increases. If the Xtal is being overdriven, an increase in supply will normally cause a decrease in frequency or instability. If the latter is the case (i.e. Xtal being overdriven), increase the value of $R_D$ *(refer to the Xtal manufacturers recommendations).*

**$X_1$ Xtal**

A parallel resonant Xtal to the value recommended in the relevant Data Sheet.

**$C_D$ Drain Capacitor**

To provide phase shift and reduce Xtal drive. Large values of $C_D$ tend to stabilize the oscillator against variations in power supply voltage but also reduce the tuning capability of the oscillator and overtone activity. *A typical value is 33.0pF ± 20% (Xtal manufacturer may recommend 5 – 40pF).*

**$C_G$ Gate Capacitor**

To provide phase shift and input voltage for the amplifier. In some oscillator circuits $C_G$ is used to adjust the oscillator to frequency although this generally may not be required. Large values of $C_G$ reduce loop-gain and increase stability. $C_G$ may be used to reduce over-voltage at the inverter input. However, the reduction in loop-gain may cause oscillator start-up problems. *$C_G$ value will be typically 5 – 65pF ± 20%, (refer to Xtal manufacturers recommendations).*

**$C_S$ Stray Capacitance**

Due to the low motional capacitance of small Xtals and the high inverter input impedance, the designer should be concerned with circuit board layout. For best oscillator performance $C_S$ should be less than 1.0pF.

# Application Information...

## DBS 800 Xtal Oscillator Configurations

It is recommended that the standard Xtal Oscillator circuit shown in Figure 8 be used for all stand-alone DBS 800 microcircuits, whilst noting that the FX806 PLMR Audio Processor has the feedback resistor $R_F$ incorporated on-chip.

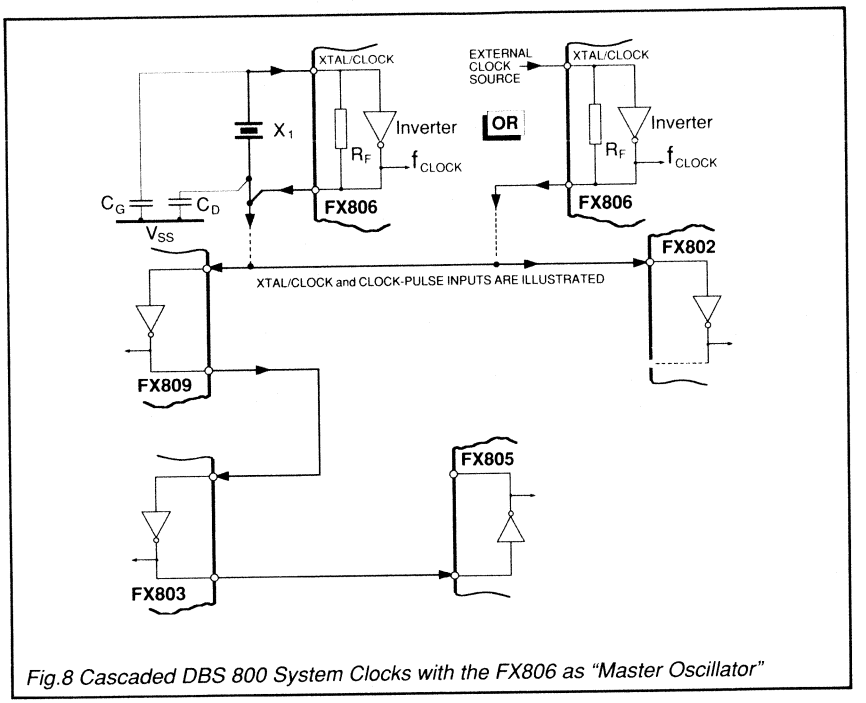



*Fig.8 Cascaded DBS 800 System Clocks with the FX806 as "Master Oscillator"*

### Xtal/Clock Distribution

Although all DBS 800 microcircuits (with the exception of the 24-pin/lead versions of the FX802 DVSR Codec) have on-chip oscillator inverters and may therefore operate independently, there are obvious advantages to driving all of the microcircuits in a system from a single Xtal/clock source.

Figure 8 (above) shows a typical Xtal/clock configuration for a complete DBS 800 Audio System employing a single Xtal at the FX806 "Master," and using this output clock signal (Xtal) to supply the remaining microcircuit inverters in cascade.

Note that the value of $C_D$ should be reduced by about 10pF to allow for the input capacitance of the driven microcircuits.

The Xtal input to the FX806, in the above example, could be replaced by a clock-pulse input to the Xtal/clock pin.

# Application Information...

## DBS 800 Xtal/Clock Frequencies

The DBS 800 family of microcircuits can be driven from either a Xtal circuit or an externally derived clock-pulse input, such as the output from a µProcessor or system clock oscillator. Table 4 shows the Sample Clock Rates employed within DBS 800 microcircuits relative to Xtal/clock input frequencies.

All DBS 800 microcircuits will operate with Xtal/clock frequencies of between 4.00MHz and 4.10MHz, it should be noted that:

(a) a 4.032MHz Xtal/clock input will produce an accurate 1200 baud rate in the FX809 FFSK Modem.

(b) a 4.096MHz Xtal/clock input will generate an accurate 16kb/s and 32kb/s sampling clock rate in the FX802 DVSR Codec.

(c) driving all DBS 800 microcircuit clock generators (and if possible, the µController) from a single clock source prevents possible 'beat-frequencies' and is therefore preferable.

DBS 800 microcircuit audio frequency responses and internal sampling clock rates will vary with respect to Xtal/clock frequency.

| | | Xtal/Clock Frequencies (MHz) | | |
|---|---|---|---|---|
| | | 4.000 | 4.032 | 4.096 |
| **Microcircuit Functions** | | **Sample Clock Rates (kHz)** | | |
| **FX802 DVSR Codec** | | | | |
| Voice Filters | at 16, 32 & 64kbit/s | 125 | 126 | 128 |
| Voice Filters | at 25 & 50kbit/s | 100 | 100.8 | 102.4 |
| Voice Sample Rates *(Nominal)* | 16.0kbit/s | 15.625 | 15.75 | 16.0 |
| | 25.0kbit/s | 25.0 | 25.2 | 25.6 |
| | 32.0kbit/s | 31.25 | 31.5 | 32.0 |
| | 50.0kbit/s | 50.0 | 50.4 | 51.2 |
| | 64.0kbit/s | 62.5 | 63.0 | 64.0 |
| **FX803 Audio Signalling Processor** | | | | |
| Tone Filters | Max. | 166 | 168 | 170 |
| | Min. | 13.15 | 13.26 | 13.47 |
| Digital Filters | High | 13.8 | 14.0 | 14.2 |
| | Mid. | 6.9 | 7.0 | 7.1 |
| | Ext. | 27.0 | 28.0 | 28.4 |
| **FX805 Sub-Audio Signalling Processor** | | | | This Xtal/clock frequency (4.096MHz), if employed with these microcircuits (FX805 or FX806), may produce sampling clock rates that place the voice-filter passband frequencies outside CEPT specifications. |
| Voice Filters | | 125 | 126 | |
| Tx Filters | Max. | 62.5 | 63.0 | |
| | Min. | 12.5 | 12.6 | |
| Rx Filters | | 35.7 | 36.0 | |
| | or | 25.0 | 25.2 | |
| Digital Filters | | 1.04 | 1.05 | |
| **FX806 PLMR Audio Processor** | | | | |
| Voice Filters | | 125 | 126 | |
| **FX809 FFSK Modem** | | | | |
| Tx Filters | | 250 | 252 | 256 |
| | or | 166 | 168 | 170 |
| Rx Filters | | 125 | 126 | 128 |

*Table 4 Examples of DBS 800 Microcircuit Sample Rates*

# FX802
# DVSR CODEC

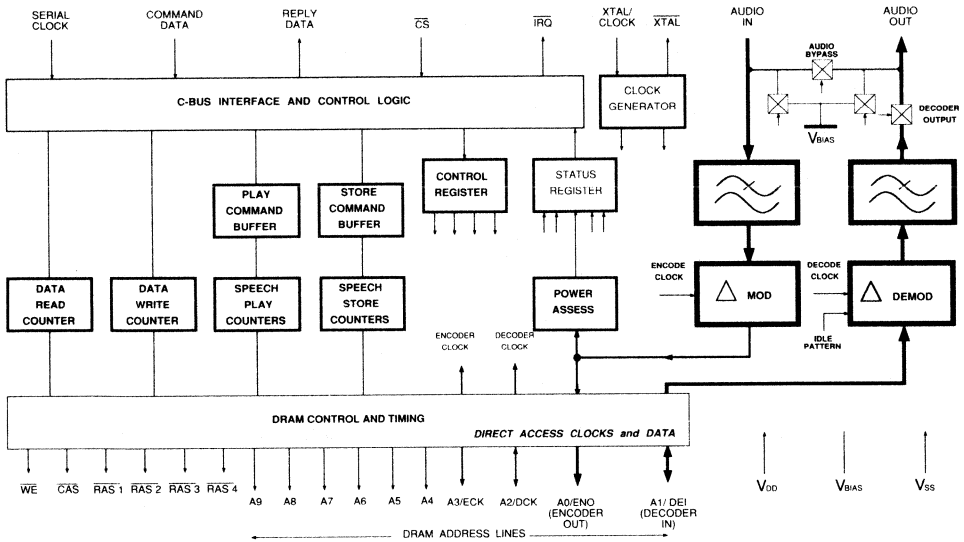



*Fig.1 FX802 DVSR Codec*

## Brief Description

The FX802 DVSR Codec contains:

A Continuously Variable Slope Delta Modulation (CVSD) encoder and decoder.

Control and timing circuitry for up to 4Mbits of external Dynamic Random Access Memory (DRAM).

"C-BUS" µProcessor interface and control logic.

When used with external DRAM, the FX802 has four primary functions:

- **Speech Storage**
  Speech signals present at the Audio Input may be digitized by the CVSD encoder, and the resulting bit stream stored in DRAM. This process also provides readings of input power level for use by the system µController.
- **Speech Playback**
  Previously digitized speech data may be read from DRAM and converted back into analogue form by the CVSD decoder.
- **Data Storage**
  Digital data sent over the "C-BUS" from the system µController may be stored in DRAM.
- **Data Retrieval**
  Digital data may be read from DRAM and sent over "C-BUS" to the system µController.

Speech storage and playback may be performed concurrently with data storage or retrieval.

The FX802 may also be used without DRAM (as a "stand-alone" CVSD Codec), in which case direct access is provided to the CVSD Codec digital data and clock signals.

All functions are controlled by "C-BUS" commands from the system µController.

The Storage, Recovery and Replay functions of the FX802 can be used for:

- Answering Machine applications, where an incoming speech message is stored for later recall.
- Busy Buffering, an outgoing speech message is stored temporarily until the transmit channel becomes free.
- Automatic transmission of pre-recorded 'Alarm' or status announcements.
- Time Domain Scrambling of speech messages.
- VOX control of transmitter functions.
- Temporary Data Storage applications, such as buffering of over-air data transmissions.

On-chip the Delta Codec is supported by input and output analogue switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control and refresh signals to interface to external DRAM.

The FX802 DVSR Codec is a low-power 5-volt CMOS LSI device and is available in 24-pin/lead SMD, 28-pin DIL and 28-lead SMD packages.

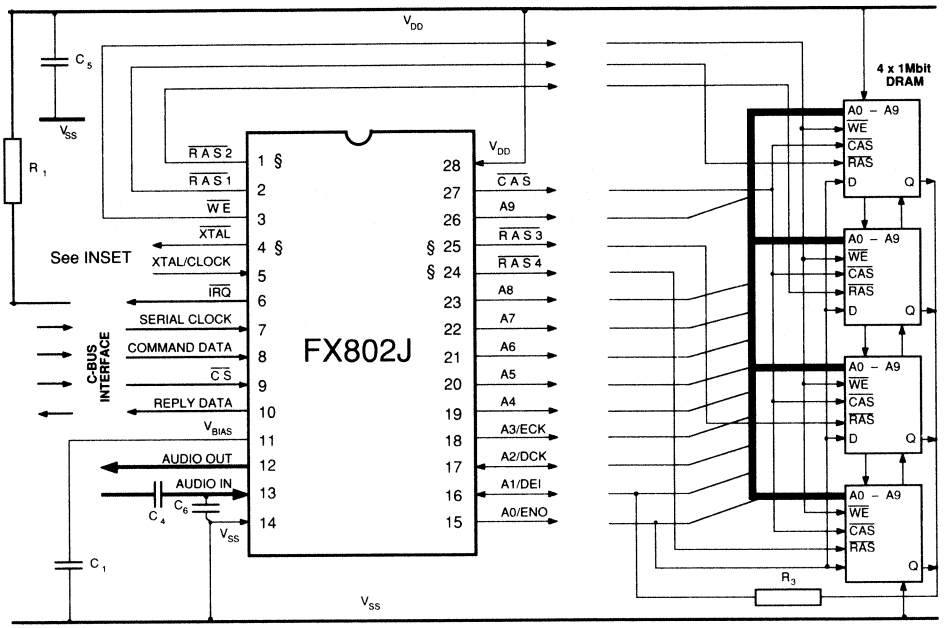
Publication D/802/2 January 1991
Provisional Issue

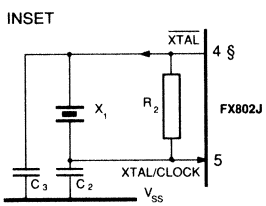
## Pin Number Function

| FX802 J/LH | FX802 LG/LS | Function |
|---|---|---|
| 1 | | **Row Address Strobe 2 ($\overline{RAS2}$):** Should be connected to the Row Address Strobe input of the second 1Mbit DRAM chip (if fitted). |
| 2 | 1 | **Row Address Strobe 1 ($\overline{RAS1}$):** Should be connected to the Row Address Strobe input of the first DRAM chip. |
| 3 | 2 | **Write Enable ($\overline{WE}$):** The DRAM Read/Write control pin. |
| 4 | | **$\overline{Xtal}$:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal is employed. A Xtal cannot be used with the 24-pin version. |
| 5 | 3 | **Xtal/Clock:** The input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here, see Figure 2. This clock provides timing for on-chip elements, filters etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device, see Table 3 for the sampling clock rate variations. |
| 6 | 4 | **Interrupt Request ($\overline{IRQ}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. The pin has a low-impedance pulldown to logic "0" when active and a high impedance when inactive.<br>Conditions indicated by this function are:<br>Power Reading Ready, Play Command Complete, Store Command Complete. |
| 7 | 5 | **Serial Clock:** The "C-BUS," serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the DVSR Codec. See Timing Diagrams and System Support Document, Document 2. The clock-rate requirements vary for differing FX802 functions. |
| 8 | 6 | **Command Data:** The "C-BUS," serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams and System Support Document, Document 2. |
| 9 | 7 | **Chip Select ($\overline{CS}$):** The "C-BUS", data transfer control function, this input is provided by the µController. Command Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagrams and System Support Document, Document 2. |
| 10 | 8 | **Reply Data:** The "C-BUS," serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams and System Support Document, Document 2. |
| 11 | 9 | **$V_{BIAS}$:** The output of the on-chip analogue circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ by a capacitor $C_1$, See Figure 2. |
| 12 | 10 | **Audio Out:** The analogue signal output. |
| 13 | 11 | **Audio In:** The audio (speech) input. The signal to this pin must be a.c. coupled by a capacitor $C_4$ and decoupled to $V_{SS}$ by an HF bypass capacitor $C_6$. For optimum noise performance this input should be driven from a source impedance of less than 100Ω. |
| 14 | 12 | **$V_{SS}$:** Negative supply rail (GND). |

| Pin Number | | Function |
|---|---|---|
| FX802 J/LH | FX802 LG/LS | |
| 15 | 13 | **DRAM Data In/A0/ (Direct Access – Encoder Out (ENO)):** Connected to the DRAM data input and address line A0. With no DRAM employed this output is available (in Direct Access mode) as the Delta Encoder digital data output. Direct Access control is achieved by Control Register byte 1 – bit 6. |
| 16 | 14 | **DRAM Data Out/ A1/ (Direct Access – Decoder In (DEI)):** Connected to the DRAM data output and address line A1. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Decoder digital data input. Direct Access control is achieved by Control Register byte 1 – bit 6. |
| 17 | 15 | **DRAM A2/ (Direct Access – Decoder Clock (DCK)):** DRAM address line A2. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Decoder Clock input. Direct Access control is achieved by Control Register byte 1 – bit 6. |
| 18 | 16 | **DRAM A3/ (Direct Access – Encoder Clock (ECK)):** DRAM address line A3. With no DRAM employed this pin is available (in Direct Access mode) as the Delta Encoder Clock output. Direct Access control is achieved by Control Register byte 1 – bit 6. |
| 19 | 17 | **DRAM A4:** DRAM address line A4. |
| 20 | 18 | **DRAM A5:** DRAM address line A5. |
| 21 | 19 | **DRAM A6:** DRAM address line A6. |
| 22 | 20 | **DRAM A7**: DRAM address line A7. |
| 23 | 21 | **DRAM A8:** DRAM address line A8. |
| 24 | | **Row Address Strobe 4 ($\overline{RAS4}$):** Should be connected to the Row Address Strobe input of the fourth 1Mbit DRAM chip (if fitted). |
| 25 | | **Row Address Strobe 3 ($\overline{RAS3}$):** Should be connected to the Row Address Strobe input of the third 1Mbit DRAM chip (if fitted). |
| 26 | 22 | **DRAM A9:** DRAM address line A9. This pin is not connected when a 256kbit DRAM is employed. **Note:** To simplify PCB layout, the DRAM address inputs A0 – A8 may be connected in any physical order to the DVSR Codec output pins A0 – A8. |
| 27 | 23 | **Column Address Strobe ($\overline{CAS}$):** The DRAM Column Address Strobe pin. Should be connected to the CAS pins of all DRAM chips. |
| 28 | 24 | $V_{DD}$: Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the DVSR Codec are dependant upon this supply. |

## External Components




| Component | | Value | | | |
|---|---|---|---|---|---|
| $R_1$ | = | 22.0kΩ | $C_4$ | = | 1.0µF |
| $R_2$ | | 1.0MΩ | $C_5$ | | 1.0µF |
| $R_3$ | | 1.0kΩ | $C_6$ | | 1.0nF |
| $C_1$ | | 1.0µF | $X_1$ | | 4.00MHz |
| $C_2$ | | 33.0pF | | or | 4.032MHz |
| $C_3$ | | 33.0pF | | or | 4.096MHz |

Tolerance: R = ±10% C = ±20%

*Fig.2 Recommended Component and DRAM Connections*

## Notes

1. Xtal circuitry shown INSET is in accordance with CML Application Note D/XT/1 April 1986.

2. External Xtal circuitry is not applicable to the 24-pin/lead versions of this device, only a clock pulse input can be used.

3. Functions whose pins are marked § above are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.

4. Table 3 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.

5. $R_1$ is used as the DBS 800 system common-pullup for the "C-BUS" Interrupt Request (IRQ) line, the optimum value will depend upon the circuitry connected to the IRQ line. Up to 8 peripherals may be connected to this line.

6. Recommended DRAM Parameters:
   256kbit x 1 or 1Mbit x 1 Dynamic Random Access Memory with 'CAS before RAS' refresh mode, maximum Row Address Access time = 200nsec.
   Example DRAM types:
   256kbit (262,144bits)
   Texas Instruments TMS4256–20
   Hitachi HM51256–15
   1Mbit (1,048,576bits)
   Texas Instruments TMX4C1024–15
   Hitachi HM511000–15

7. Figure 2 (above) shows connections to 4 x 1Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0 to A8 may be connected in any order to the FX802 DVSR Codec output pins A0 to A8. Connections to 256kbit DRAM are similar, but A9 unconnected.

8. When using the FX802 "stand-alone (Direct Access)," no DRAM should be connected.

## Controlling Protocol

Control of the functions of the FX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions or data to and from the system µController (see Figure 5). The use and content of these instructions is detailed in the following paragraphs and tables.

| Command Assignment | Address/Command (A/C) Byte Hex. | Binary MSB LSB | + | Data Byte/s |
|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | |
| Write to Control Register | 60 | 0 1 1 0 0 0 0 0 | + | 2 byte Instruction to Control Register |
| Read Status Register | 61 | 0 1 1 0 0 0 0 1 | + | 1 byte Reply from Status Register |
| Store 'N' pages. Start page 'X' | 62 | 0 1 1 0 0 0 1 0 | + | 2 bytes Command – Immediate |
| Store 'N' pages. Start page 'X' | 63 | 0 1 1 0 0 0 1 1 | + | 2 bytes Command – Buffered |
| Play 'N' pages. Start page 'X' | 64 | 0 1 1 0 0 1 0 0 | + | 2 bytes Command – Immediate |
| Play 'N' pages. Start page 'X' | 65 | 0 1 1 0 0 1 0 1 | + | 2 bytes Command – Buffered |
| Write Data. Start page 'P' | 66 | 0 1 1 0 0 1 1 0 | + | 2 bytes 'P' + Write data |
| Read Data. Start page 'P' | 67 | 0 1 1 0 0 1 1 1 | + | 2 bytes 'P' + Read data |
| Write Data – Continue | 68 | 0 1 1 0 1 0 0 0 | + | Write data |
| Read Data – Continue | 69 | 0 1 1 0 1 0 0 1 | + | Read data |

*Table 1 "C-BUS" Address/Commands*

## Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data, or
(ii) a Status or data Reply.

Control and configuration is by writing instructions from the µController to the Control Register ($60_H$).
Reporting of FX802 configurations is by reading the Status Register ($61_H$). Instructions and data are transferred, via "C-BUS," in accordance with the timing information given in Figures 5 and 6.
A complete list of DBS 800 "C-BUS" Address locations is published in the System Support Document, Document 2.

## Speech

The delta encoder and decoder sampling rates are independently set, via the Control Register (Table 4), to (nominally) 16, 25, 32, 50 or 64kbits/s (see Tables 2 and 3), allowing the user to choose between speech-quality and storage-time, whilst providing for time-compression or expansion of the speech signals.

The DVSR Codec can handle from 256kbits to 4Mbits of DRAM, giving, in the case of 32kbit/s sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into 'pages' of 1024 bits each, corresponding to 32ms at a 32kbit/s sampling rate.

| | |
|---|---|
| A 256kbit DRAM contains | 256 pages. |
| A 1Mbit DRAM contains | 1024 pages. |
| 4Mbit of DRAM contains | 4096 pages. |

The Delta Codec may be used without DRAM, when the decoder sampling rate (8 to 64 kbits/s) is determined by an external clock source applied to the Decoder Clock pin.

## Operation with DRAM

The FX802 can operate with up to 4Mbits of DRAM. When used with DRAM the DVSR Codec performs four main functions under the control of commands received over the "C-BUS" interface from the µController:

**Stores Speech** by digitally encoding the analogue input signal and writing the resulting digital data into the associated Dynamic RAM (DRAM).

**Plays** stored speech by reading the digital data stored in the DRAM and decoding it to provide an analogue output signal.

**Writes** data sent over the "C-BUS" from the µController to DRAM.

**Reads** data from DRAM, sending it to the µC over the "C-BUS".

'Data' is directed to and from DRAM by the on-chip DRAM Controller.

### Store and Play Speech Commands

Speech storage and playback may take place simultaneously.

These commands are transmitted, via "C-BUS," to the FX802, in the form:

**STORE or PLAY 'N' (1024-bit) pages (of encoded speech data) starting at page 'X.'**

**'N'** is any number from 1 to 16 (pages) and **'X'** from (page) 0 to 4095 (4Mbit DRAM), as illustrated below.
Preceded by the A/C, this command writes 16-bits (byte 1 (first) and byte 0) of data from the µC to the FX802 Store or Play Command Buffer.

| MSB Byte 1 | | | | | | | | Byte 0 | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 'N' | | | | | | | | 'X' | | | | | | | |

## Store and Play Speech

### Speech Store Commands

$62_H$ STORE 'N' PAGES – START PAGE 'X' (immediate).

$63_H$ STORE 'N' PAGES – START PAGE 'X' (buffered).

The digitised speech from the Delta Encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete 'pages' stored since the start of execution of the command.
As soon as the command has terminated the following events take place:

(1) The "Store Command Complete" bit in the Status Register (Table 6) is set.

(2) An "Interrupt Request" (IRQ) is sent (if enabled) to the µC.

(3) The next Speech Store command (if present) is immediately taken from the Store Command Buffer and execution of the new command commences.

The IRQ output is cleared by reading the Status Register.

$61_H$ READ STATUS REGISTER (Table 6).

To provide continuity of speech commands, both Store and Play commands can be presented to the FX802 in one of two formats; *Immediate or Buffered.*

An *Immediate* command will be started on completion of its loading, irrespective of the condition of the current command.

A *Buffered* command will be acted upon on the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps, even though the µController may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the Status Register will be cleared.

---

**Speech Playback** is controlled by similar commands:

$64_H$ PLAY 'N' PAGES – START PAGE 'X' (immediate).

$65_H$ PLAY 'N' PAGES – START PAGE 'X' (buffered).

using the Speech Play Counters and Play Command Buffer.

As soon as the Play Command has completed, the "Play Command Complete" bit in the Status Register is set and an Interrupt Request generated (if enabled).

If no 'next' command is waiting in the Play Command Buffer when a speech Play command finishes, a continuous idle code (0101.....0101) will be fed to the Delta Decoder.

Speech "data" is stored or recovered at the selected Encode or Decode sample rate (Table 3).
Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play command received from the µC, or by a General Reset command.

**Store/Play Speech Synchronization** – (Table 4)

This facility is provided, primarily, for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

**No Speech Sync Set;** Store and Play operations may take place completely independently.

**Store after Play;** The next "buffered" Store command will start *on completion of a Play operation*, whilst the next Play command (if any) sequence continues normally.

**Play after Store;** The next "buffered" Play command will start *on completion of a Store operation*, whilst the next Store command (if any) sequence continues normally.

These actions will continue whilst 'Speech Sync' bits remain set.

---

### DRAM Speech Capacity

28-pin/lead versions of the FX802 may be used with a single 256kbit DRAM or with up to 4 x 1Mbit DRAM.
24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different Encode and Decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 2 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reverse sequence, see Control Register for details.

| DRAM Size | Available Bits | "Speech Pages" | Nominal Sample Rates (kbits/s) 16 | 25 | 32 | 50 | 64 |
|---|---|---|---|---|---|---|---|
| 256kbits | 262144 | 256 | 16.0 | 10.0 | 8.0 | 5.0 | 4.0 |
| 1024k | 1048576 | 1024 | 65.0 | 42.0 | 32.0 | 20.0 | 16.0 |
| 2Mbits | 2097152 | 2048 | 131.0 | 84.0 | 65.0 | 42.0 | 32.0 |
| 3M | 3145728 | 3072 | 196.0 | 126.0 | 98.0 | 63.0 | 49.0 |
| 4M | 4194304 | 4096 | 262.0 | 168.0 | 131.0 | 84.0 | 65.5 |
| | | | Store and Play Times (seconds) | | | | |

*Table 2 Sampling Clock Rates vs Speech Storage/Playback Times*

# Controlling Protocol...

## Data Operations

### Data Storage and Recovery

For the purpose of storing data sent via "C-BUS" from the µC, the memory (DRAM) is divided into 'data-pages' of 64-bits (8-bytes).

A single 256kbit DRAM contains
4096 data-pages.
A single 1Mbit DRAM contains
16384 data-pages.
4Mbit DRAM contains
65536 data-pages.

In accordance with "C-BUS" timing specifications, data is handled 8-bits (1-byte) at a time although any number of 8-bit blocks of data may be written-to or read-from the DRAM by a single command.

The data transfer action is terminated by the Chip Select line being taken to a logic "1.

### "C-BUS" Data Transfer Limitations

For those commands which transfer data over the "C-BUS" between DRAM and the µController (Write and Read Data) the "C-BUS" Serial Clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing Store and Play commands.

250kHz if no speech Store or Play commands are active.

All other commands and replies (Control, Status, General Reset) may use a maximum clock rate of 500kHz. See Figure 5.

Read and Write Data actions are explained below

**Read Data**

$67_H$ READ DATA – START PAGE "P"

Sets the Data Read Counter to "P" page and then reads data bytes from successive DRAM locations, sending them to the µC as Reply Data bytes incrementing the Data Read Counter by 1 for each bit read.

$69_H$ READ DATA – CONTINUE

Reads data bytes from successive DRAM locations determined by the Data Read Counter incrementing the counter by 1 for each bit read.

**Write Data**

$66_H$ WRITE DATA – START PAGE "P"

Sets the Data Write Counter to "P" page and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the "C-BUS."

The Start Page "P," is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data-page addresses from 0 to 65535 (4Mbits DRAM).

$68_H$ WRITE DATA – CONTINUE

Writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the "C-BUS."

## Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 3 shows the range of sampling rates available for differing Xtal/clock input frequencies, and the counter ratios used to produce them.
If different "Store and Play" sampling rates are used in a single operation, only combinations of 25kb/s with 32kb/s or 50kb/s with 64kb/s will give correct output levels in accordance with current specifications. Consideration should be given to the effect of differing Xtal/clock frequencies upon the audio frequency performance of the device.

| | | | | Xtal/clock Frequency (MHz) | | |
|---|---|---|---|---|---|---|
| **Control Register** *Byte 0, Bits* | | | | **4.0** | **4.032** | **4.096** |
| **5** | **4** | **3** | **Dec.** | **Internal Counter** | | |
| **2** | **1** | **0** | **Enc.** | **Division Ratio** | **Sampling Rate (kbits/s)** | |
| 0* | 1 | 1 | | 256 | 15.625 | 15.75 | 16.0 |
| 1 | 0 | 0 | | 160 | 25.0 | 25.20 | 25.60 |
| 1 | 0 | 1 | | 128 | 31.25 | 31.50 | 32.0 |
| 1 | 1 | 0 | | 80 | 50.0 | 50.4 | 51.20 |
| 1 | 1 | 1 | | 64 | 62.50 | 63.0 | 64.0 |

*Table 3 Sampling Clock Rates Available*

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use it should be noted that:
(a) a 4.032MHz Xtal/clock input will produce an accurate 1200 baud rate for the FX809 FFSK Modem
(b) a 4.096MHz Xtal/clock input will generate exactly 16kb/s and 32kb/s Codec sampling clock rates.

## "Write to Control Register" — Address/Command $60_H$, followed by 2 bytes of Command Data

| Setting | Function |
|---|---|
| ***Byte 1*** | ***First Byte for Transmission*** |
| ***(MSB) Bit 7*** | Not used – Set to "0" |
| ***6*** | **Direct Access** |
| 1 | – Encoder Data Out to A0/ENO<br>– Encoder Clock to A3/ECK<br>– Decoder Input from A1/DEI<br>– Decoder Clock from A2/DCK |
| 0 | Normal DVSR Operation |
| ***5*** | **Play Counter** |
| 1 | Decrement |
| 0 | Increment |
| ***4*** | **DRAM Control** |
| 1 | Disable DRAM |
| 0 | Enable DRAM |
| ***3*** | **Codec Powersave** |
| 1 | Powersave Delta Codec |
| 0 | Enable Delta Codec |
| ***2*** | **Store Command Interrupt** |
| 1 | Enable Interrupt |
| 0 | Disable |
| ***1*** | **Play Command Interrupt** |
| 1 | Enable Interrupt |
| 0 | Disable |
| ***0*** | **Power Reading Interrupt** |
| 1 | Enable Interrupt |
| 0 | Disable |
| ***Byte 0*** | ***Last Byte for Transmission*** |
| ***(MSB) 7 6*** | **Store/Play Speech Sync** |
| 0 0 | No Sync |
| 0 1 | No Sync |
| 1 0 | Sync – Play after Store |
| 1 1 | Sync – Store after Play |
| ***5 4 3*** | **Decoder Control** |
| 0 0 0 | Idle (32kbit/s); Aud O/P via L.P.F. |
| 0 0 1 | Idle (32kbit/s); Aud By-Pass |
| 0 1 0 | Idle (32kbit/s); Aud O/P at High Z |
| 0 1 1 | On – Sampling Rate 16kbit/s |
| 1 0 0 | On – " 25kbit/s |
| 1 0 1 | On – " 32kbit/s |
| 1 1 0 | On – " 50kbit/s |
| 1 1 1 | On – " 64kbit/s |
| ***2 1 0*** | **Encoder Control** |
| 0 0 0 | I/P at $V_{BIAS}$ – F/Idle (32kbit/s) |
| 0 0 1 | I/P at High Z – F/Idle (32kbit/s) |
| 0 1 0 | I/P at High Z – F/Idle (32kbit/s) |
| 0 1 1 | On – Sampling Rate 16kbit/s |
| 1 0 0 | On – " 25kbit/s |
| 1 0 1 | On – " 32kbit/s |
| 1 1 0 | On – " 50kbit/s |
| 1 1 1 | On – " 64kbit/s |

*Table 4 Control Register*

### General Reset

Upon Power-Up the "bits" in the FX802 registers will be random (either "0" or "1"). A General Reset command ($01_H$) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX802:

Control Register Set as $00_H$
Status Register Set as $00_H$
Clear Store and Play Command Buffers

### Direct Access

Allows external circuitry "Direct Access" to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the FX802 to be used as a "stand-alone" delta modulation voice encoder and decoder.

Input Audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

The following points, with respect to Control Register settings, should be considered. Analogue output switching remains under the control of the Control Register, but the Decoder sampling clock rate (8kbit/s to 64kbit/s) must be provided from an external source to the Decoder Clock (DCK) pin. To ensure correct filter setting, Decoder Control bits (Byte 0, Bits 5, 4, 3) should be set to (binary) 1, 1, 1, where the required rate approximates to a multiple of 16kb/s, or (binary) 1, 1, 0, where the required rate approximates to a multiple of 25kb/s.

Both the Encoder internal sampling clock rate and input switching (Table 5) remain under the control of the Control Register. The sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

### Play Counter

The Play Counter direction may be set to run backwards as well as forwards. This can be used in a scrambling system by replaying speech data in reverse order.

### DRAM Control

A logic "1" will disable the DRAM Control timing circuits and associated counters. The "C-BUS" Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic "1" when the FX802 is used in the Direct Access mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to a logic "1."

### Codec Powersave

A logic "1" puts the Delta Codec and filters into a Powersave mode, with $V_{BIAS}$ maintained.

The Clock Generator, "C-BUS" Interface and DRAM Control and Timing remain active.

### Command Interrupt Enable

A logic "1" set at the relevant bit will enable Interrupt Requests to the µController when that command operation is complete.

### Store and Play Speech Synchronization

Intended, primarily, for Time Domain Scrambling.

### Decoder and Encoder Control

Sets individually, decoder and encoder sampling clock rates and the source of the Audio Output.

## Decoder and Encoder Control

### Analogue Input and Output Switching

The Control Register, Byte 0 – bits 0 to 5, are used, in conjunction with the codec Powersave Bit (Byte 1 – bit 3) to control codec input/output conditions and sample rates. Figure 3 shows the codec functional situation.

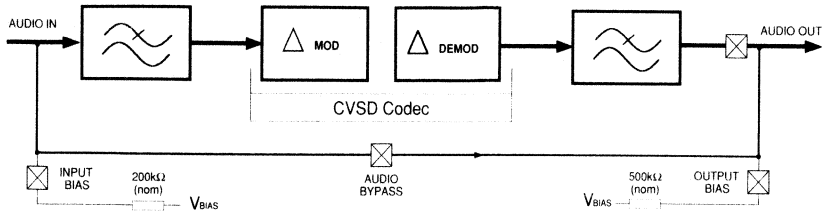



*Fig.3 Analogue Control – with reference to Fig.1*

| Control Register | | | | Circuit Switches | | | OFF = Switch Open<br>ON = Switch Closed | |
|---|---|---|---|---|---|---|---|---|
| Codec Powersave Bit | Decoder Control "5" | "4" | "3" | Audio By-Pass | Audio Out | Output Bias | | Note |
| 0 | 0 | 0 | 0 | OFF | ON | OFF | Decoder 'idling' fed with "1010101 ...." pattern at 32kb/s. | 1 |
| 0 | 0 | 0 | 1 | ON | OFF | OFF | | |
| 0 | 0 | 1 | 0 | OFF | OFF | OFF | | |
| 0 | 0 | 1 | 1 | OFF | ON | OFF | Decoder running at the selected sampling rate. | 1 |
| – | – | – | – | – | – | – | | |
| 0 | 1 | 1 | 1 | OFF | ON | OFF | | |
| 1 | 0 | 0 | 0 | OFF | OFF | ON | Decoder circuits Powersaved | |
| 1 | 0 | 0 | 1 | ON | OFF | OFF | | |
| 1 | 0 | 1 | 0 | OFF | OFF | ON | | |
| 1 | 0 | 1 | 1 | OFF | OFF | ON | | |
| – | – | – | – | – | – | – | | |
| 1 | 1 | 1 | 1 | OFF | OFF | ON | | |
| | Encoder Control "2" | "1" | "0" | | Input Bias | | | 2 |
| 0 | 0 | 0 | 0 | | ON | | Encoder running at 32kb/s but Encoder Data Output forced to 'idle' pattern "01010 ..." | |
| 0 | 0 | 0 | 1 | | OFF | | | |
| 0 | 0 | 1 | 0 | | OFF | | | |
| 0 | 0 | 1 | 1 | | OFF | | Encoder running at selected Sampling Rate | |
| – | – | – | – | | – | | | |
| 0 | 1 | 1 | 1 | | OFF | | | |
| 1 | 0 | 0 | 0 | | ON | | Encoder circuits Powersaved | |
| – | – | – | – | | – | | | |
| 1 | 1 | 1 | 1 | | ON | | | |

*Table 5 Analogue Control – with reference to Fig.3*

**Notes**

1. If the Delta Codec is in the Direct Access mode, these sampling rates will be as provided by the externally applied clock.
2. The Input Bias switch is operated by the Control Register Codec Powersave' and 'Encoder Control' bits to provide a relatively low impedance path for $V_{BIAS}$ to charge the input coupling capacitor whenever the codec is powersaved, or the Encoder control bits are set to "0," so that input bias can be established quickly prior to operation.

## Time Compression of Speech

The 25kb/s and 50kb/s sampling rate options are provided for time compression (and subsequent expansion) of speech signals.

For example, 1.0 second of speech stored at 50kb/s may be transmitted in 0.8 seconds if played out at 64kb/s, and finally restored to its original speed at the receiver by storing at 64kb/s and playing out at 50kb/s. A similar result (with a degraded SINAD) may be achieved by using 25kb/s and 32kb/s sampling rates.

However, the speech frequencies are raised by time compression, and since the signal transmitted to air must be band limited to 3400Hz, the effective end-to-end bandwidth is 0.8 x 3400Hz, which is approximately 2700Hz.

## "Read Status Register" – Address/Command, $61_H$, followed by 1 byte of Reply Data.

| Reading | | | | | Function | |
|---|---|---|---|---|---|---|
| | | | | | | |
| *MSB* | | | | | | |
| *Bit 7* | | | | | **Power Reading** | |
| 1 | | | | | Ready | |
| | | | | | | |
| *6* | | | | | **Store Command** | |
| 1 | | | | | Complete | |
| | | | | | | |
| *5* | | | | | **Play Command** | |
| 1 | | | | | Complete | |
| | | | | | | |
| | | | | | **Power Register** | |
| *4* | *3* | *2* | *1* | *0* | **Pwr** | **Compand Bits**/page |
| 0 | 0 | 0 | 0 | 0 | | 0 |
| 0 | 0 | 0 | 0 | 1 | | 1 |
| 0 | 0 | 0 | 1 | 0 | | 2 |
| 0 | 0 | 0 | 1 | 1 | | 3 |
| 0 | 0 | 1 | 0 | 0 | | 4 |
| 0 | 0 | 1 | 0 | 1 | | 5 |
| 0 | 0 | 1 | 1 | 0 | | 6 |
| 0 | 0 | 1 | 1 | 1 | | 7 |
| 0 | 1 | 0 | 0 | 0 | -39.0 dB | 8 |
| 0 | 1 | 0 | 0 | 1 | | 10 |
| 0 | 1 | 0 | 1 | 0 | -36.0 | 12 |
| 0 | 1 | 0 | 1 | 1 | | 14 |
| 0 | 1 | 1 | 0 | 0 | -33.5 | 16 |
| 0 | 1 | 1 | 0 | 1 | | 18 |
| 0 | 1 | 1 | 1 | 0 | -30.0 | 20 |
| 0 | 1 | 1 | 1 | 1 | | 22 |
| 1 | 0 | 0 | 0 | 0 | -28.0 | 24 |
| 1 | 0 | 0 | 0 | 1 | | 32 |
| 1 | 0 | 0 | 1 | 0 | -25.0 | 40 |
| 1 | 0 | 0 | 1 | 1 | | 48 |
| 1 | 0 | 1 | 0 | 0 | -22.0 | 56 |
| 1 | 0 | 1 | 0 | 1 | | 64 |
| 1 | 0 | 1 | 1 | 0 | -19.0 | 72 |
| 1 | 0 | 1 | 1 | 1 | | 80 |
| 1 | 1 | 0 | 0 | 0 | -16.0 | 88 |
| 1 | 1 | 0 | 0 | 1 | | 128 |
| 1 | 1 | 0 | 1 | 0 | -10.0 | 192 |
| 1 | 1 | 0 | 1 | 1 | | 256 |
| 1 | 1 | 1 | 0 | 0 | -6.0 | 320 |
| 1 | 1 | 1 | 0 | 1 | | 384 |
| 1 | 1 | 1 | 1 | 0 | 0dB | 448 |
| 1 | 1 | 1 | 1 | 1 | | 512 |

*Table 6 Status Register*

**Interrupts**
An Interrupt Request ($\overline{IRQ}$), (if enabled by the Control Register) is produced by the FX802 to report the following actions:

Power Reading Ready
Store Command Complete
Play Command Complete.

When an Interrupt Request is produced the Status Register must be read to ascertain the source of the interrupt. This action will clear the $\overline{IRQ}$ output.

**Store Command Complete** bit
(and an interrupt) is set on completion of a Store command. This bit is cleared by loading the next Store command, or by a General Reset command ($01_H$).

**Play Command Complete** bit
(and an interrupt) is set on completion of a Play command. This bit is cleared by loading the next Play command, or by a General Reset command ($01_H$).

**Power Reading Ready** bit
(and an interrupt) is set for every 1024 (1 page) voice-data bits from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset command ($01_H$).

**Power Register**
The power assessment element shown in Figure 1 assesses the input signal power for each encoded 'page' (every 1024 encoder output bits) by counting the number of 'compand bits' (000 or 111 sequences in the output bit-stream) produced during that 'page,' shown in Table 6, with typical encoder input power levels (dB).
Power Reading measurements (Bits 0 – 4) are produced under the same conditions as in Figure 4.

At the end of each 'page' the "Power Reading Ready" bit of the Status Register is set, an Interrupt Request is generated (if enabled) and the resulting count converted to a 5-bit quasi-logarithmic form.

The Power Register reading is interpreted as below.

| | |
|---|---|
| 00000 represents | 0 compand bits |
| 00001 represents | 1 compand bit |
| 11111 represents | 512 compand bits – the maximum. |

This "Power" reading is placed in the Status Register where it can be read by the µC.

Figure 4 shows this output in graphical form, indicating the typical Input Power Level.

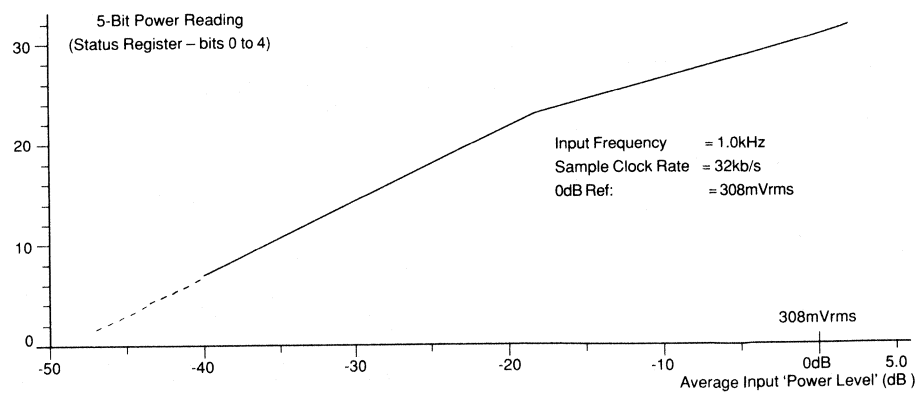



*Fig.4 Typical "Power" Readings vs Input Level*

## Timing Information

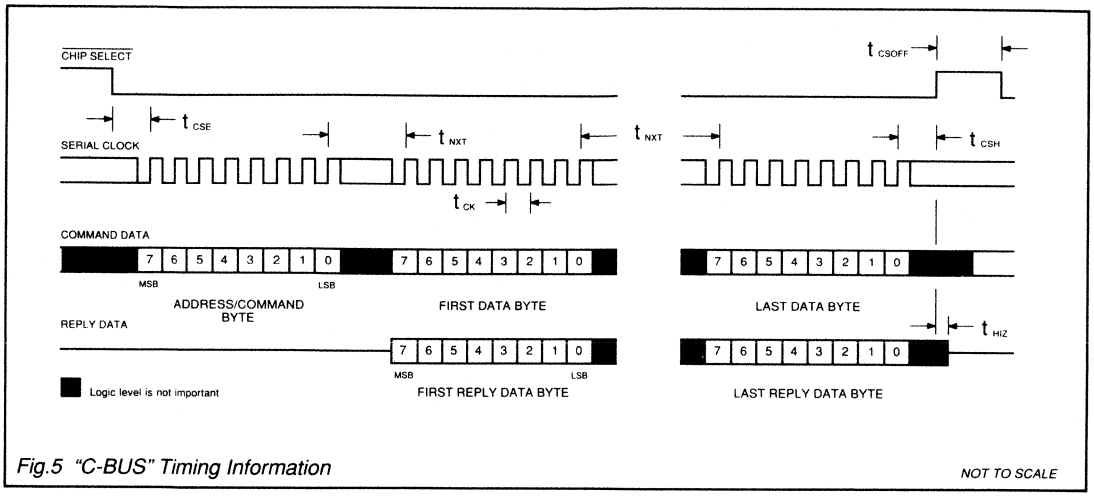



*Fig.5 "C-BUS" Timing Information*

NOT TO SCALE

**"C-BUS" Timing** – Figure 5

| Parameter | Min. | | | Max. | Unit |
|---|---|---|---|---|---|
| | a | b | c | | |
| $t_{CSE}$ | 2.0 | 4.0 | 8.0 | – | µs |
| $t_{CSH}$ | 4.0 | 4.0 | 8.0 | – | µs |
| $t_{HIZ}$ | – | – | – | 2.0 | µs |
| $t_{CSOFF}$ | 2.0 | 4.0 | 8.0 | – | µs |
| $t_{NXT}$ | 4.0 | 8.0 | 16.0 | – | µs |
| $t_{CK}$ | 2.0 | 4.0 | 8.0 | – | µs |

**Direct Access Timing** – Figure 6

| Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|
| $t_{CH}$ | 1.0 | – | – | µs |
| $t_{CL}$ | 1.0 | – | – | µs |
| $t_{SU}$ | 450 | – | – | ns |
| $t_H$ | 600 | – | – | ns |
| $t_{PCO}$ | – | – | 750 | ns |

$t_{SU} + t_H$ = Data True Time

**Notes**

(1) **Minimum Timing Values**
- (a) For all commands except "Read Data" and "Write Data" commands.
- (b) For "Read Data" and "Write Data" commands when no "Speech Store" or "Speech Play" commands are active.
- (c) For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.

(2) Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first, LSB (bit0) last. Reply Data is read from the peripheral MSB (bit7) first, LSB (bit0) last.

(3) To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity Serial Clock pulses.

(4) Data sent from the µController is clocked into the FX802 on the rising edge of the Serial Clock pulses. Reply Data sent from the FX802 to the µController is clocked into the µController when the Serial Clock is "high."

(5) Loaded commands are acted upon at the end of each command.

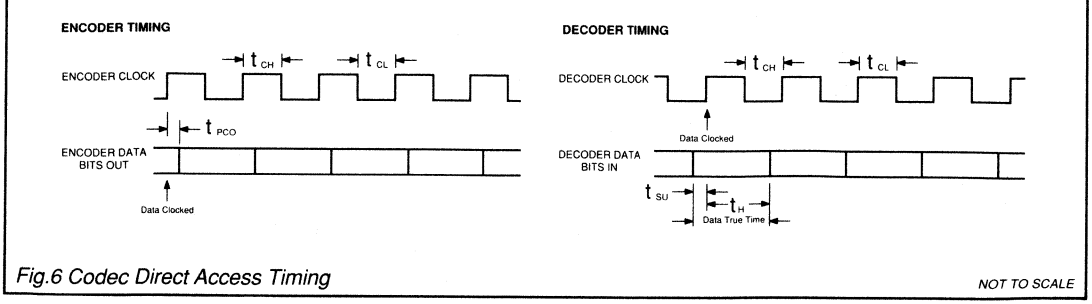



*Fig.6 Codec Direct Access Timing*

NOT TO SCALE

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX802J** | -40°C to +85°C (cerdip) |
| | **FX802LG/LH/LS** | -40°C to +85°C (plastic) |
| Storage temperature range: | **FX802J** | -55°C to +125°C (cerdip) |
| | **FX802LG/LH/LS** | -40°C to +85°C (plastic) |

**Operating Limits**

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.0MHz. Standard Test Signal $f_0$ = 1.0kHz. Sample Rate = 31.25kbits/s
Audio Level 0dB ref: = 308mVrms .

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage ($V_{DD}$) | | 4.5 | 5.0 | 5.5 | V |
| Supply Current (enabled) | 1 | – | 7.0 | – | mA |
| Supply Current (all powersaved) | 1 | – | 1.0 | – | mA |
| **Digital Interface** | | | | | |
| Input Logic "1" | 2, 4 | 3.5 | – | – | V |
| Input Logic "0" | 2, 4 | – | – | 1.5 | V |
| Output Logic "1" | | | | | |
| at IOH = -120µA | 8, 4 | 4.6 | – | – | V |
| at IOH = -50µA | 3, 4 | 4.6 | – | – | V |
| at IOH = 20µA | 4, 10 | 4.6 | – | – | V |
| Output Logic "0" | | | | | |
| at IOL = 20µA | 4, 10 | – | – | 0.4 | V |
| at IOL = 100µA | 3, 4 | – | – | 0.4 | V |
| at IOL = 360µA | 4, 8, 9 | – | – | 0.4 | V |
| Digital Input Current ($V_{IN}$ = Logic "1" or "0") | 2 | – | – | 1.0 | µA |
| Leakage Current into IRQ "OFF" Output | 5 | – | – | 4.0 | µA |
| Digital Input Capacitance | 2 | – | – | 7.5 | pF |
| **Analogue Impedance** | | | | | |
| Input Impedance | 13 | – | 500 | – | kΩ |
| Output Impedance | | – | 1.5 | – | kΩ |
| **Dynamic Values** | | | | | |
| **Encoder** | | | | | |
| Analogue Signal Input Levels | 6 | -24.0 | – | 4.0 | dB |
| Passband | 11, 12 | – | 3400 | – | Hz |
| **Decoder** | | | | | |
| Analogue Signal Output Levels | 6 | -24.0 | – | 4.0 | dB |
| Passband | 11, 12 | 300 | – | 3400 | Hz |
| **Encoder/Decoder (Full Codec)** | | | | | |
| Passband | 11, 12 | 300 | | 3400 | Hz |
| Passband Gain | 12 | – | 0 | – | dB |
| Passband Ripple | 12 | -3.0 | – | 3.0 | dB |
| Stopband | | 6.0 | – | 10 | kHz |
| Stopband Attenuation | | – | 50.0 | – | dB |
| SINAD Level (-6dB) | | – | 23.0 | – | dB |
| Output Noise (Input short circuit) | | – | -50 | – | dBp |
| Idle Channel Noise (Forced ) | | – | -55 | – | dBp |
| Xtal/clock Frequency | 7 | – | 4.0 | – | MHz |

**Notes**

1. Does not include current drawn by any attached DRAM.
2. Serial Clock, Command Data, CS, A1/DEI and A2/DCK inputs.
3. CAS, WE and A0 to A9 outputs.
4. All measurements are made at 5.0 volts $V_{DD}$, any variations may alter parameters accordingly.
5. When the IRQ Output is at $V_{DD}$.
6. The optimum range of levels for a good Signal-to-Noise Ratio.
7. Audio frequency responses will vary with respect to Xtal/clock frequency.
8. Reply Data output.
9. IRQ output.
10. RAS Outputs.
11. Passband is reduced to (typically) 2700Hz when a sample rate of 25kb/s or 50kb/s is employed.
12. Measured with a -20dB input level to avoid codec slope-overload.
13. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.

## Codec Performance

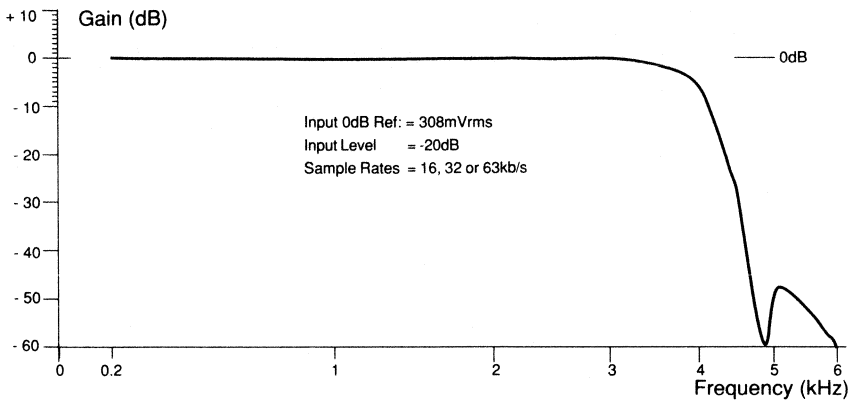



*Fig.7 Typical Overall (Encoder + Decoder) Frequency Response*

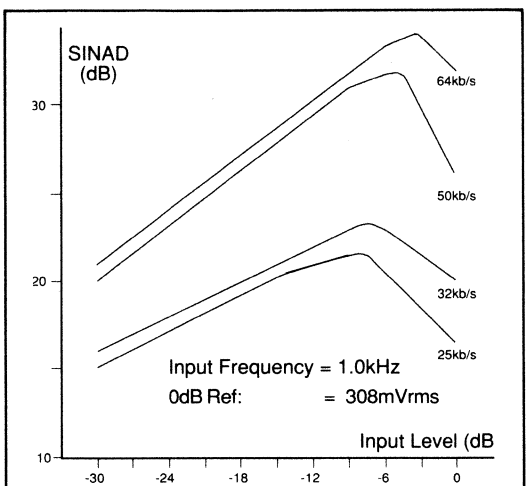



*Fig.8 SINAD vs Input Level at Differing Sample Rates*

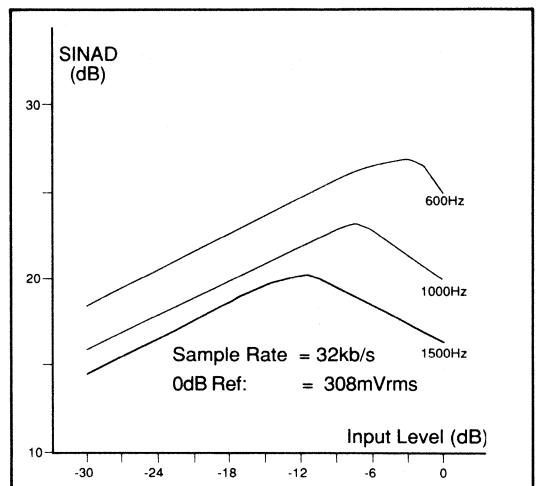



*Fig.9 SINAD vs Input Level at Differing Frequencies*

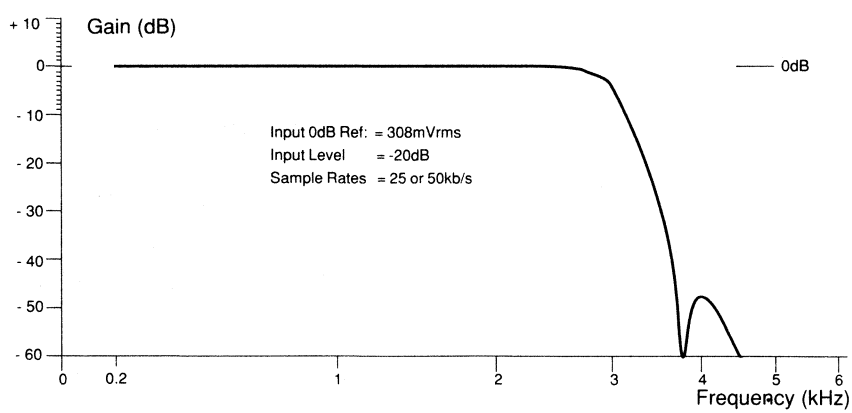
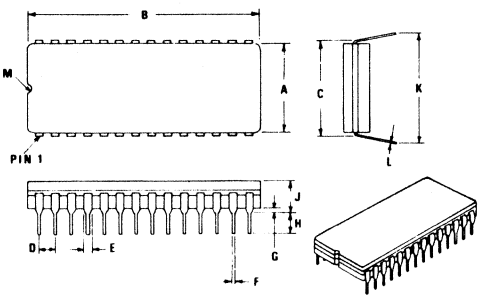



*Fig.10 Typical Overall (Encoder + Decoder) Frequency Response*

## Package Outline

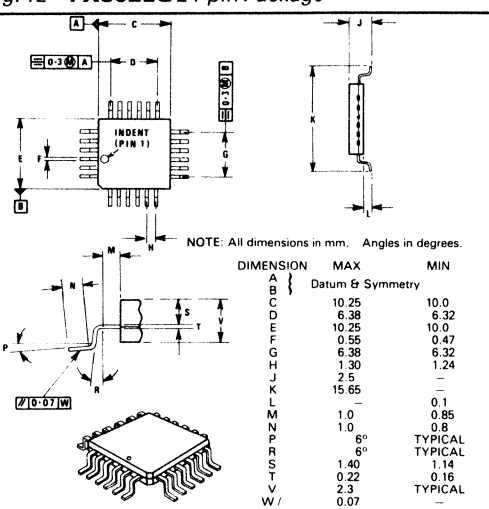
The FX802J, the dual-in-line package is shown in Figure 11. The 'LG' version is shown in Figure 12, the 'LS' version in Figure 13 and the 'LH' version in Figure 14. To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. The 'LH' package has an indent spot adjacent to pin 1 and a chamfered corner between pins 4 and 5. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 11* **FX802J** *28-pin DIL Package*




| DIMENSION | MAX | MIN | DIMENSION | MAX | MIN |
|---|---|---|---|---|---|
| A | 13.36 | 13.06 | G | 1.40 | TYPICAL |
| B | 37.05 | 36.58 | H | 4.30 | 4.10 |
| C | 15.70 | 15.50 | J | 5.57 | 4.49 |
| D | 2.54 | TYPICAL | K | 17.00 | TYPICAL |
| E | 1.39 | TYPICAL | L | 0.25 | TYPICAL |
| F | 0.45 | TYPICAL | M | 0.64R | TYPICAL |

*Fig. 12* **FX802LG** *24-pin Package*



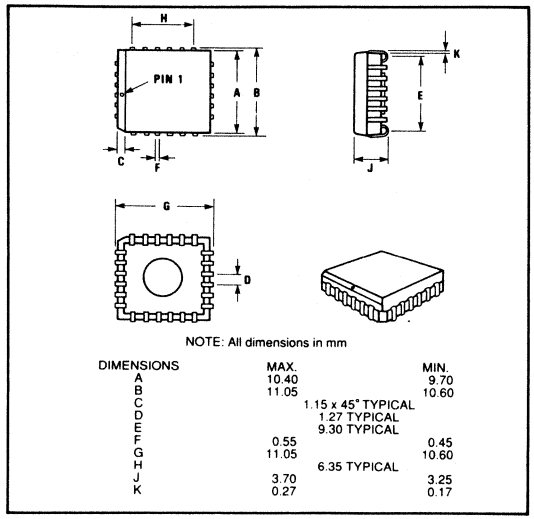

NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

## Handling Precautions

The FX802 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

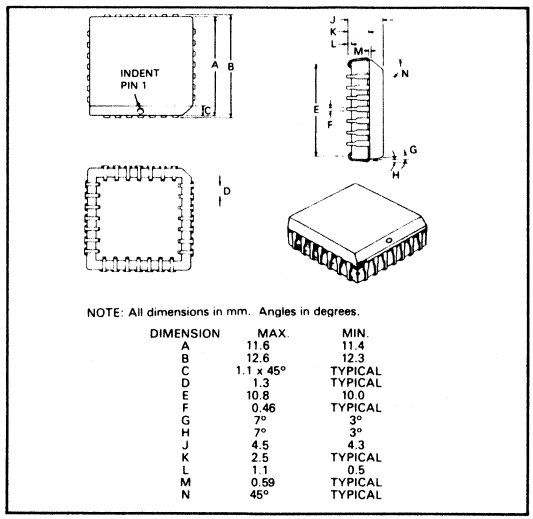
*Fig. 13* **FX802LS** *24-lead Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

*Fig. 14* **FX802LH** *28-lead Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 11.6 | 11.4 |
| B | 12.6 | 12.3 |
| C | 1.1 x 45° | TYPICAL |
| D | 1.3 | TYPICAL |
| E | 10.8 | 10.0 |
| F | 0.46 | TYPICAL |
| G | 7° | 3° |
| H | 7° | 3° |
| J | 4.5 | 4.3 |
| K | 2.5 | TYPICAL |
| L | 1.1 | 0.5 |
| M | 0.59 | TYPICAL |
| N | 45° | TYPICAL |

## Ordering Information

| | |
|---|---|
| **FX802J** | 28-pin cerdip DIL |
| **FX802LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX802LS** | 24-lead plastic leaded chip carrier |
| **FX802LH** | 28-lead plastic leaded chip carrier |

# FX803 Audio Signalling Processor

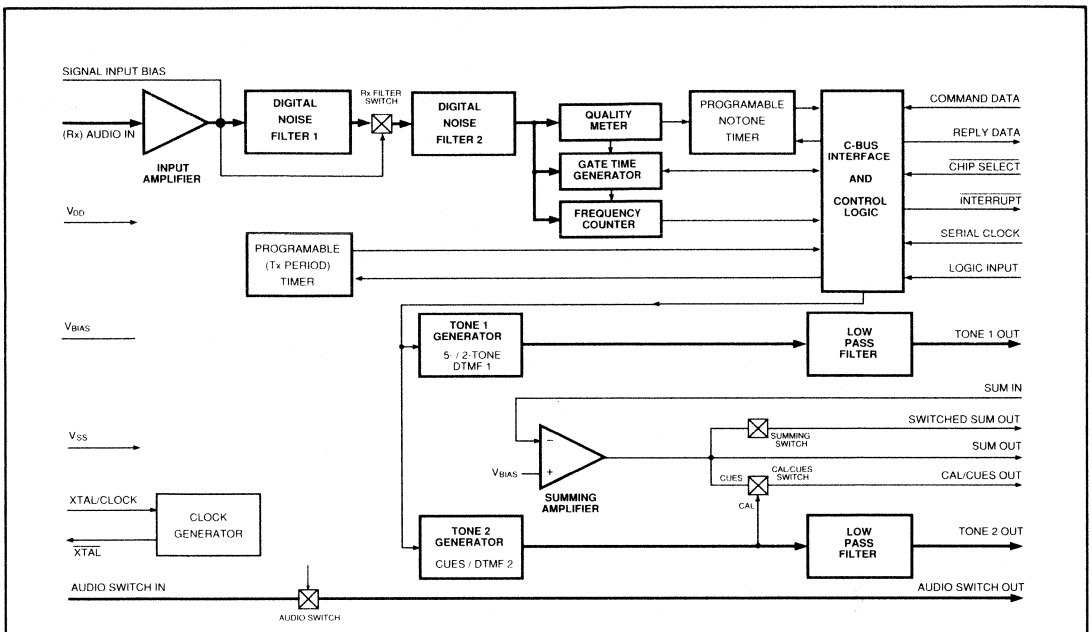



*Fig.1 FX803 Audio Signalling Processor*

## FX803 Audio Signalling Processor

As part of the DBS 800 System, this audio signalling processor will provide an inband tone signalling facility for PMR radio systems. Signalling systems supported include Selcall (CCIR, ZVEI I, II and III, EEA), 2-Tone Selcall and Dual Tone Multi-Frequency (DTMF) encode.

Using a non-predictive tone decoder and versatile encoders gives the FX803 the capability to work in any standard or non-standard tone system.

This is a full-duplex device consisting of:

- Two individual tone generators and a programmable (Tx) period timer.
- A tone decoder with programmable NOTONE Timer.
- An on-chip summing amplifier.

For use with Single Tone or Selective Call systems.

Under the control of the µController, via "C-BUS," the FX803 will encode and transmit a single or pair of audio tones, in the frequency range 208Hz to 3kHz, simultaneously, and detect, decode and indicate the frequency of non-predicted input tones in the frequency range 313Hz to 6kHz.

Both tone generators can be individually placed into a power economical "Powersave" mode.

A general purpose logic input, interfacing directly with the Status Register, is provided. This could be used as an auxiliary method of routeing digital information to the µController via the "C-BUS."

The output frequencies are produced from data loaded to the device, with a programmable, general purpose, on-chip timer available to indicate the tone transmit periods.

A Dual Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This Summing Amplifier output is also available for level adjustment.

Tones produced by the FX803 can also be used in the DBS 800 system as modulation calibration inputs and for "CUE" audio indications for the operator.

Received tones are measured and their frequency indicated to the µController in the form of a received data word. A poor-quality or incoherent tone will, after a programmed period, indicate NOTONE.

The FX803 is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.

Publication D/803/3 February 1993
Provisional Issue

## Pin Number Function

| FX803 J/LG/LS | |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2. |
| 2 | **Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock ($f_{XTAL}$) should be connected here. See Figure 2. |
| 3 | **Reply Data:** The "C-BUS" serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high-impedance when not sending data to the µController. See Timing Diagrams. |
| 4 | **Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagram. |
| 5 | **Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams. |
| 6 | **Logic Input:** This 'real-time' input is available as a general purpose logic input port which can be read from the Status Register. See Table 3. |
| 7 | **Interrupt Request ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low-impedance pulldown to logic "0" when active and a high-impedance when inactive. The System IRQ line requires one pullup resistor to $V_{DD}$.<br>The conditions that cause interrupts are indicated in the Status Register and are shown below:<br>G/Purpose Timer Period Expired — NOTONE Timer Period Expired<br>Rx Tone Measurement Complete<br>These interrupts are inactive during relevant Powersave conditions and can be disabled by Bits 5 and 6 in the Control Register. |
| 8 | No internal connection, connect to $V_{SS}$. |
| 9 | No internal connection, connect to $V_{SS}$. |
| 10 | **Audio Switch In:** The input to the stand-alone, on-chip Audio Switch. This switching function (Control Register Bit 7) may be used to break the system transmitter modulation path when it is required to provide a CUE (beep) from Tone Generator 2 to the loudspeaker via the FX806 PLMR Audio Processor. |
| 11 | **Audio Switch Out:** The output of the stand-alone, on-chip Audio Switch. |
| 12 | **$V_{SS}$:** Negative Supply (Signal Ground). |

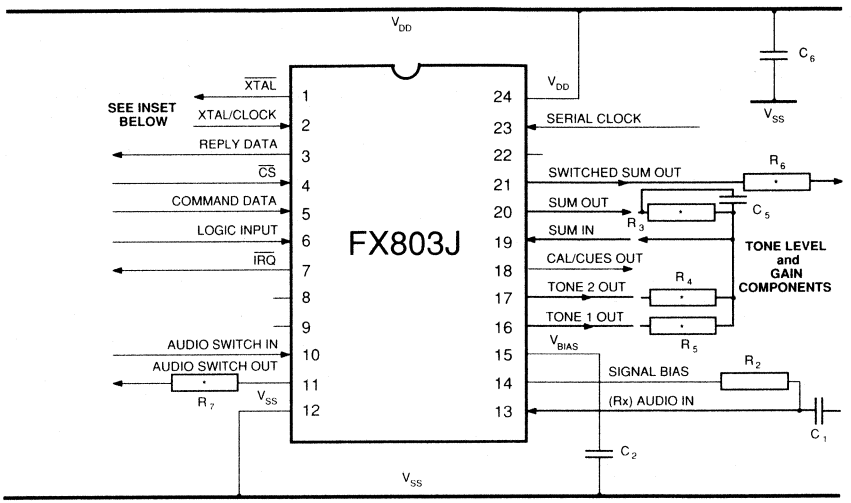
## Pin Number Function

| FX803 J/LG/LS | |
|---|---|
| 13 | **(Rx) Audio In:** The received audio tone signalling input to the Input Amplifier. This input requires to be a.c. coupled and connected, using external components, to the Signal Input Bias pin. See Figure 2. |
| 14 | **Signal Input Bias:** External components are required between this input and the (Rx) Audio In pin See Figure 2. |
| 15 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$ by capacitor $C_2$ See Figure 2. |
| 16 | **Tone 1 Out:** Tone 1 Generator (2-/5- tone Selcall or DTMF 1) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to Tx Tone Generator 1 Register (Table 4). See Figure 2. |
| 17 | **Tone 2 Out:** Tone 2 Generator (2-/5- tone Selcall, CUES or DTMF 2) output. External gain and coupling components will be required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to Tx Tone Generator 2 Register (Table 5). See Figure 2. |
| 18 | **CAL/CUES Out:** An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by Bit 14 in the Tx Tone Generator 2 Register (Table 5). In a DBS 800 audio installation, this output should be connected to the Calibration Input of the FX806 PLMR Audio Processor. When Tone Generator 2 is set to $V_{BIAS}$ (NOTONE), the CAL output is pulled to $V_{BIAS}$ and during a powersave of Tone Generator 2 it is held at $V_{SS}$. |
| 19 | **Sum In:** The input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figures 2 and 3. |
| 20 | **Sum Out:** The output of the on-chip Summing Amplifier. Combined tones (1 and 2) are available at this output. See Figures 2 and 3. |
| 21 | **Switched Sum Out:** The combined tone output available for transmitter modulation. The switch allows control of the FX803 final output to the FX806. Control of this switch is by Bit 4 of the Control Register. See Figures 2 and 3. |
| 22 | No internal connection, connect to $V_{SS}$. |
| 23 | **Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the Audio Signalling Processor. See Timing Diagrams. |
| 24 | **$V_{DD}$:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the Audio Signalling Processor are dependent upon this supply. |

**NOTE:** (i) Pins 8, 9 and 22 may be connected to $V_{SS}$ to improve screening.
(ii) Further information on external components and DBS 800 system integration of this microcircuit are contained in the System Support Document, Document 2.
(iii) A glossary of abbreviations used in this document can be found on Page 14.

***"C-BUS"** is CML's proprietary standard for the transmission of commands and data between a µController and DBS 800 microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController.*

## External Components




| Component | | Value | | | |
|---|---|---|---|---|---|
| $R_1$ | = | 1.0MΩ | $C_1$ | = | 0.1µF |
| $R_2$ | | 2.0MΩ | $C_2$ | | 1.0µF |
| *$R_3$ | | 100kΩ | $C_3$ | | 33.0pF |
| *$R_4$ | | 82.0kΩ | $C_4$ | | 33.0pF |
| *$R_5$ | | 122kΩ | $C_5$ | | 22.0pF |
| *$R_6$ | | 100kΩ | $C_6$ | | 1.0µF |
| *$R_7$ | | 100kΩ | $X_1$ | $f_{XTAL}$ | 4.032MHz |

Tolerance: R = ± 10% C = ± 20%

*Fig.2 Recommended External Components*

### Notes

1. Xtal/clock circuitry components shown INSET are recommended in accordance with CML Application Note D/XT/1 April 1986. The DBS 800 System Support Document contains additional notes on the use of Xtal/clock frequencies ($f_{XTAL}$).

2. It is recommended that, to improve screening and reduce noise levels around the FX803, Pins 8, 9 and 22 are connected to $V_{SS}$.

3. Resistors marked with an asterisk (*) are System Components, calculated to operate in a system with other DBS 800 microcircuits. Figure 3 shows in detail, these components used in the System signal paths.

   $R_3$, $R_4$, $R_5$, $C_5$ – Tone mixing components to provide a 3dB tone-differential (twist) when used in a DTMF configuration. Single tone output levels are set independently or by the FX806 Modulator Drivers.

   $R_7$ – Modulation level and matching for inputs to the FX806.

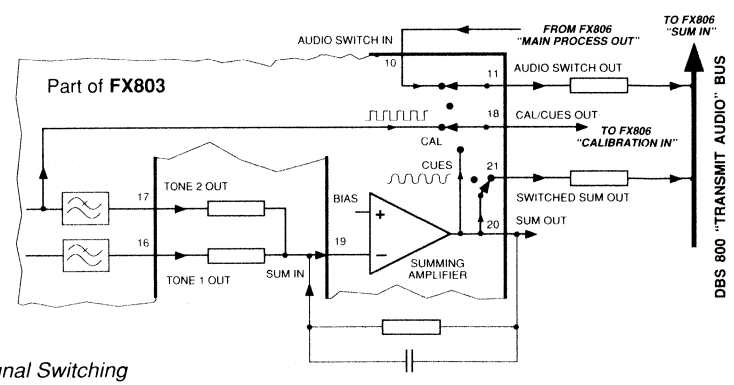



*Fig.3 Output Signal Switching*

## Controlling Protocol

Control of the FX803 Audio Signalling Processor's operation is by communication between the μController and the FX803 internal registers on the "C-BUS," using Address/Commands (A/Cs) and appended instructions or data (see Figure 7). The use and content of these instructions is detailed in the following paragraphs and tables.

## FX803 Internal Registers

FX803 internal registers are detailed below:

**Control** Register ($30_H$) – Write Only, control and configuration of the FX803.

**Status** Register ($31_H$) – Read Only, reporting of device functions.

**Rx Tone Frequency** Register ($32_H$) – Read Only, indicates frequency of the last received input.

**Rx NOTONE Timer** Register ($33_H$) – Write Only, setting of the Rx NOTONE period.

**Tx Tone Generator 1** Register ($34_H$) – Write Only, setting the required output frequency from Tx Tone Generator 1.

**Tx Tone Generator 2** Register ($35_H$) – Write Only, setting required output frequency from Tx Tone Generator 2.

**General Purpose Timer** Register ($36_H$) – Write Only, setting of a general purpose, sequential time period.

## Address/Commands

The first byte of a loaded data sequence is always recognized by the "C-BUS" as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data or,

(ii) a Status or data Reply.

Instructions and data are loaded and transferred, via "C-BUS," in accordance with the timing information given in Figures 7 and 8.

Table 1 shows the list of A/C bytes relevant to the FX803. A complete list of DBS 800 "C-BUS" Address allocations is published in the System Support Document, Document 2.

| Command Assignment | Address/Command (A/C) Byte Hex. | Binary MSB LSB | + | Data Byte/s |
|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | |
| Write to Control Register | 30 | 0 0 1 1 0 0 0 0 | + | 1 byte Instruction to Control Register |
| Read Status Register | 31 | 0 0 1 1 0 0 0 1 | + | 1 byte Reply from Status Register |
| Read Rx Tone Frequency | 32 | 0 0 1 1 0 0 1 0 | + | 2 byte Reply from Rx Tone Register |
| Write to NOTONE Timer | 33 | 0 0 1 1 0 0 1 1 | + | 1 byte Instruction to NOTONE Register |
| Write to Tx Tone Gen. 1 | 34 | 0 0 1 1 0 1 0 0 | + | 2 byte Instruction to Tx Tone Gen. 1 |
| Write to Tx Tone Gen. 2 | 35 | 0 0 1 1 0 1 0 1 | + | 2 byte Instruction to Tx Tone Gen. 2 |
| Write to G/Purpose Timer | 36 | 0 0 1 1 0 1 1 0 | + | 1 byte Instruction to G/Purpose Timer |

*Table 1 "C-BUS" Address/Commands*

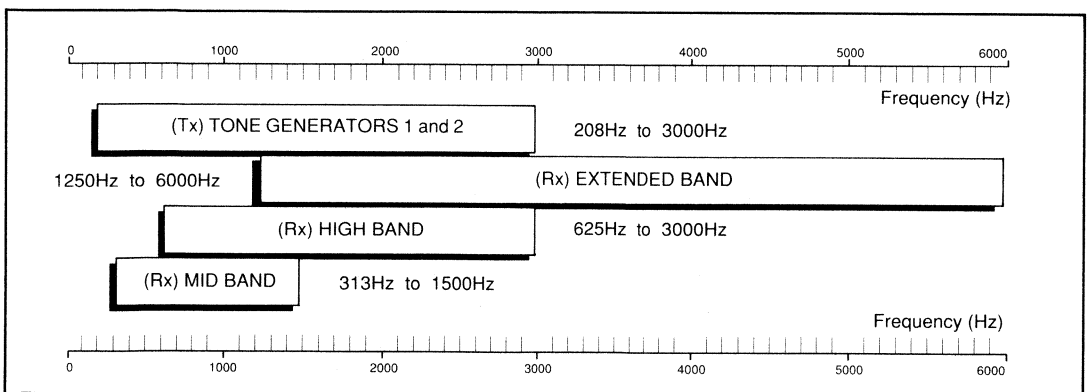



*Fig.4 FX803 Frequencies*

# Controlling Protocol...

## "Write to Control Register" – A/C $30_H$, followed by 1 byte of Command Data.

**Audio Switch**

See the Signal Switching diagram (Figure 3) and DBS 800 Document 2 for application examples.

**General Purpose Timer**

Should be set up before interrupts are enabled, as a General Reset command will set the timer period to $00_H$ – 0ms (permanent interrupt). See Page 14, Operational Recommendations.

**Interrupt Enable Instructions**

Status Bits 0, 1 and 2 are produced regardless of the state of these settings.

**Band Selection**

Bits 2 and 3 set the required frequency range (see Figure 4, FX803 Frequencies).

**Summing Switch**

To break the FX803 drive to the FX806 PLMR Audio Processor (see Figure 3, Signal Switching).

**Interrupt Designation**

Decoder Interrupts:
No Tone Timer and Rx Tone Measurement.

Transmitter Interrupt:
G/Purpose Timer Interrupt.

| *Setting* | *Control Bits* |
|---|---|
| ***MSB Bit 7*** | ***Transmitted First*** |
| 1 | **Audio Switch** Enable |
| 0 | Disable |
| ***6*** | **G/Purpose Timer Interrupt** |
| 1 | Enable |
| 0 | Disable |
| ***5*** | **Decoder Interrupts** |
| 1 | Enable |
| 0 | Disable |
| ***4*** | **Summing Switch** |
| 1 | Enable |
| 0 | Disable |
| ***3*** ***2*** | **Band Selection** |
| 0 0 | High Band |
| 0 1 | Mid Band |
| 1 0 | Extended Band |
| 1 1 | Do Not use this setting |
| ***1*** | Set to |
| 0 | "0" |
| ***0*** | Set to |
| 0 | "0" |

*Table 2 Control Register*

## "Read Status Register" – A/C $31_H$, followed by 1 byte of Reply Data.

| *Reading* | *Status Bits* |
|---|---|
| ***MSB Bit 7*** | ***Received First*** |
| 0 | Set to "0" |
| ***6*** | Set to |
| 0 | "0" |
| ***5*** | Set to |
| 0 | "0" |
| ***4*** | Set to |
| 0 | "0" |
| ***3*** | **Logic Input Status** |
| 1 | "1" |
| 0 | "0" |
| ***2*** | **G/Purpose Timer Period** |
| 1 | Expired (IRQ generated if enabled) *(Table 2)* |
| ***1*** | **NOTONE Timer Period** |
| 1 | Expired (IRQ generated if enabled) *(Table 2)* |
| ***0*** | **Rx Tone Measurement** |
| 1 | Complete (Interrupt Generated) |

*Table 3 Status Register*

**Interrupt Requests ($\overline{IRQ}$)**

Interrupts on this device are available to draw the attention of the µController to a change in the condition of the bit in the Status Register. However Bits are set in the Status Register irrespective of the setting of interrupt enable bits (Table 2) and these changes may be recognized by 'polling' the register.

**General Purpose Timer Period**

**Set** to a logic "1" when the timer period has expired.
**Cleared** to a logic "0,"

i By a read of the Status Register or,
ii New G/Purpose Timer information or,
iii General Reset Command

**NOTONE Timer Period**

**Set** to a logic "1" when the timer period has expired.
**Cleared** to a logic "0,"

i By a read of the Status Register or,
ii New NOTONE Timer information or,
iii General Reset Command

**Rx Tone Measurement**

**Set** to a logic "1" when the Rx Tone measurement is complete.
**Cleared** to a logic "0,"

i By a read of the Status Register or,
ii General Reset Command

## Tx Tone Generator Registers 1 and 2

Each Tx Tone Generator is controlled individually by writing a two-byte command to the relevant Tx Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency ($f_{TONE}$) generation described in the following text.

### "Write to Tx Tone Generator 1 Register" – A/C $34_H$ followed by 2 bytes of Command Data.

| MSB (loaded first) | | | Bit Numbers | | | | | | | | | | | | LSB (loaded last) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| "0" | "0" | $V_{BIAS}$/ Enable | These 13 bits (0 to 12) are used to produce a binary number, designated "**A**." "**A**" is used in the formulas below to set the Tx Tone 1 frequency ($f_{TONE}$ 1). | | | | | | | | | | | | |

The binary number produced by bits 0 to 12 (MSB) is designated "A."
If "A" = all logic "0" then Tx Tone Generator 1 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at $V_{BIAS}$ (NOTONE).
"0" = Tone 1 Output Enabled.
Bits 14 and 15 (MSB) must be logic "0."

*Table 4 Setting Tx Tone Generator 1*

### "Write to Tx Tone Generator 2 Register" – A/C $35_H$ followed by 2 bytes of Command Data.

| MSB (loaded first) | | | Bit Numbers | | | | | | | | | | | | LSB (loaded last) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| "0" | CAL/ CUES | $V_{BIAS}$/ Enable | These 13 bits (0 to 12) are used to produce a binary number, designated "**B**." "**B**" is used in the formulas below to set the Tx Tone 2 frequency ($f_{TONE}$ 2). | | | | | | | | | | | | |

The binary number produced by bits 0 to 12 (MSB) is designated "B."
If "B" = all logic "0" then Tx Tone Generator 2 is Powersaved.

Bit 13 at logic "1" = Tone 1 Output at $V_{BIAS}$ (NOTONE).
"0" = Tone 1 Output Enabled.
Bit 14 at logic "1" = Squarewave CAL Output.
"0" = Sinewave CUES Output.
Bit 15 (MSB) must be a logic "0."

*Table 5 Setting Tx Tone Generator 2*

**Notes**

(1) Programming Tone Generator 2 to $V_{BIAS}$ (NOTONE) (Bit 13) will place the CAL/CUES Output at $V_{BIAS}$ via a 40kΩ internal resistor.
(2) Programming Tone Generator 2 to Powersave will place the CAL/CUES Output at $V_{SS}$.
(3) If both Tone Generators (1 and 2) are Powersaved, the Summing Amplifier is also Powersaved.

## Calculations

As can be seen from Tables 4 and 5 (above), a binary number ("A" or "B" – Bits 0 to 12) is loaded to the respective Tx Tone Generator. The formulas shown below are used to calculate the required output frequency.

| | | |
|---|---|---|
| Required Tx Tone output frequency | = | $f_{TONE}$ 1 or 2 |
| XTAL/clock frequency | = | $f_{XTAL}$ |
| Input Data Word (Bits 0 to 12) | = | "A" or "B" |

**Formula**

$$f_{TONE\ (Hz)} = \frac{f_{XTAL\ (Hz)}}{4 \times \text{"A" (or "B")}} \quad \textit{or} \quad \textbf{Input "A" (or "B")} = \frac{f_{XTAL\ (Hz)}}{4 \times f_{TONE\ (Hz)}}$$

### Tx Tone Frequencies

With reference to Tables 4 and 5 (above), whilst Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters (see "Specification" page).

## "Read Rx Tone Frequency Register" – A/C $32_H$, followed by 2 bytes of Reply Data.

### Measurement of Rx Signal Frequency ($S_{INPUT}$)

The measurement details given are for a Xtal/clock frequency ($f_{XTAL}$) of 4.032MHz, a scaling formula for other values of $f_{XTAL}$ is given at the bottom of page 10.

The input audio signal ($S_{INPUT}$) is filtered and measured in the Frequency Counter over a specified "measurement period" (9.125 ms or 18.250 ms).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the Rx Tone Measurement bit in the Status Register, and the Interrupt bit (if enabled) are set.

The Rx Tone Frequency Register will now indicate the signal frequency ($S_{INPUT}$) in the form of 2 bytes (1 and 0) as illustrated in Figure 6 below.

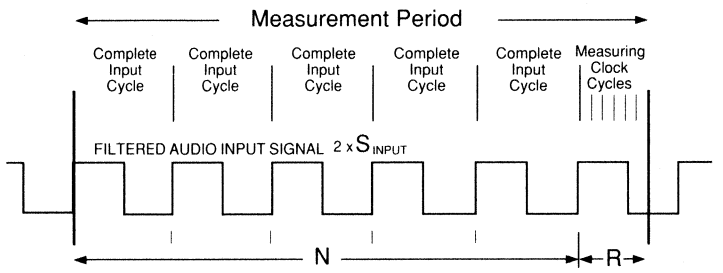



*Fig.5 Measurement of a Mid or High Band Rx Frequency*

### The Integer (N) – Byte 1

A binary number representing *'twice the number of complete input audio cycle periods'* counted during the specified measurement period, which is:

| | | | | |
|---|---|---|---|---|
| High Band Decode | = | 9.125 ms | = | "t" |
| Mid Band Decode | = | 18.250 ms | = | "t" |
| Extended Band Decode | = | 9.125 ms | = | "t" |

See the bottom of this page for "t" and "f" scaling factors

### The Remainder (R) – Byte 0

A binary number representing the remainder part, R, of 2 x Input Signal Frequency ($S_{INPUT}$). *'R = number of specified measuring-clock cycles'* required to complete the specified measurement period (See N).

The clock-cycle frequencies are:

| | | | | |
|---|---|---|---|---|
| High Band Decode | = | 56.00 kHz | = | "f" |
| Mid Band Decode | = | 28.00 kHz | = | "f" |
| Extended Band Decode | = | 56.00 kHz | = | "f" |

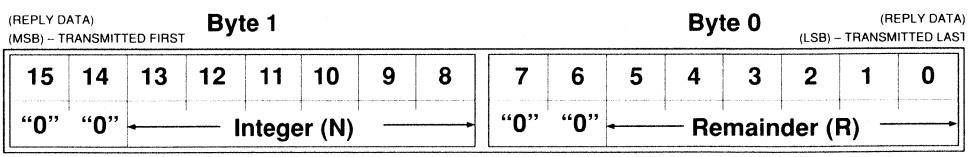



*Fig.6 Format of the Rx Tone Frequency Register*

### $f_{XTAL}$ Scaling Factors

The calculations above are for an $f_{XTAL}$ of 4.032MHz. The following formulas enable the calculation of these values using any Xtal value. Note: $f_{XTAL}$ values are stated in MHz.

$$\text{"t"}_{scaled} = \text{"t"} \times \left[\frac{4.032}{f_{XTAL}}\right]$$

$$\text{"f"}_{scaled} = \text{"f"} \times \left[\frac{f_{XTAL}}{4.032}\right]$$

## Frequency Measurement Formulæ

To assist in the production of 'look-up' tables and limit-values in the µController and provide guidance upon the determination of N and R from a measured frequency, the following formulæ show the derivation of the Rx frequency, $S_{INPUT}$, from the measured data bytes (N and R), Figure 6.

## High Band Measurement

**$S_{INPUT}$ – High Band**

In the measurement period of 9.125ms, there are Nh cycles at $2S_{INPUT}$ and Rh clock cycles at 56.000kHz.

$$\text{so} \quad \frac{Nh}{2 \times S_{INPUT}} + \frac{Rh}{56000} = 9.125\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{28000 \times Nh}{(511 - Rh)} \text{ Hz} \qquad [1]$$

**Nh and Rh – High Band**

The measurement period = 9.125ms
Clock Frequency = 56.000kHz
The measured frequency = $2 \times S_{INPUT}$ c/s
In the measurement period there are:
$2 \times S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

Nh is the lower integer value of this decimal number:

$$Nh = \text{INT}\,(9.125 \times 10^{-3} \times 2 \times S_{INPUT}) \qquad [4]$$

Rh is rounded to the nearest integer of this decimal number:

$$Rh = (9.125 \times 10^{-3} - \frac{Nh}{2 \times S_{INPUT}}) \times 56000 \qquad [5]$$

## Mid Band Measurements

**$S_{INPUT}$ – Mid Band**

In the measurement period of 18.250ms, there are Nm cycles at $2S_{INPUT}$ and Rm clock cycles at 28.000kHz.

$$\text{so} \quad \frac{Nm}{2 \times S_{INPUT}} + \frac{Rm}{28000} = 18.250\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{14000 \times Nm}{(511 - Rm)} \text{ Hz} \qquad [2]$$

**Nm and Rm – Mid Band**

The measurement period = 18.250ms
Clock Frequency = 28.000kHz
The measured frequency = $2 \times S_{INPUT}$ c/s
In the measurement period there are:
$2 \times S_{INPUT} \times 18.250 \times 10^{-3}$ cycles

Nm is the lower integer value of this decimal number:

$$Nm = \text{INT}\,(18.250 \times 10^{-3} \times 2 \times S_{INPUT}) \qquad [6]$$

Rm is rounded to the nearest integer of this decimal number:

$$Rm = (18.250 \times 10^{-3} - \frac{Nm}{2 \times S_{INPUT}}) \times 28000 \qquad [7]$$

## Extended Band Measurements

**$S_{INPUT}$ – Extended Band**

In the measurement period of 9.125ms, there are Ne cycles at $S_{INPUT}$ and Re clock cycles at 56.000kHz.

$$\text{so} \quad \frac{Ne}{S_{INPUT}} + \frac{Re}{56000} = 9.125\text{ms}$$

$$\text{From which } S_{INPUT} = \frac{56000 \times Ne}{(511 - Re)} \text{ Hz} \qquad [3]$$

**Ne and Re – Extended Band**

The measurement period = 9.125ms
Clock Frequency = 56.000kHz
The measured frequency = $S_{INPUT}$ c/s
In the measurement period there are:
$S_{INPUT} \times 9.125 \times 10^{-3}$ cycles

Ne is the lower integer value of this decimal number:

$$Ne = \text{INT}\,(9.125 \times 10^{-3} \times S_{INPUT}) \qquad [8]$$

Re is rounded to the nearest integer of this decimal number:

$$Re = (9.125 \times 10^{-3} - \frac{Ne}{S_{INPUT}}) \times 56000 \qquad [9]$$

## Controlling Protocol...

### "Write to the Rx NOTONE Timer Register" – A/C $33_H$ followed by 1 byte of Command Data.

| Setting | | | | Function/Period | | |
|---|---|---|---|---|---|---|
| MSB | | | | | | |
| 7 | 6 | 5 | 4 | *Transmitted Bit 7 First* | | |
| 0 | 0 | 0 | 0 | These 4 bits must be "0" | | |
| 3 | 2 | 1 | 0 | | High/Extended Band | Mid Band |
| 0 | 0 | 0 | 0 | period (ms) | 0 | 0 |
| 0 | 0 | 0 | 1 | " | 20 ±1% | 40 ±1% |
| 0 | 0 | 1 | 0 | | 40 " | 80 " |
| 0 | 0 | 1 | 1 | | 60 " | 120 " |
| 0 | 1 | 0 | 0 | | 80 " | 160 " |
| 0 | 1 | 0 | 1 | | 100 " | 200 " |
| 0 | 1 | 1 | 0 | | 120 " | 240 " |
| 0 | 1 | 1 | 1 | | 140 " | 280 " |
| 1 | 0 | 0 | 0 | | 160 " | 320 " |
| 1 | 0 | 0 | 1 | | 180 " | 360 " |
| 1 | 0 | 1 | 0 | | 200 " | 400 " |
| 1 | 0 | 1 | 1 | | 220 " | 440 " |
| 1 | 1 | 0 | 0 | | 240 " | 480 " |
| 1 | 1 | 0 | 1 | | 260 " | 520 " |
| 1 | 1 | 1 | 0 | | 280 " | 560 " |
| 1 | 1 | 1 | 1 | | 300 " | 600 " |

*Table 6 Rx NOTONE Timer Settings*

### Operation of the Rx NOTONE Timer

An Rx NOTONE period is that period when no signal or a consistently bad-quality signal is received.

The Rx NOTONE Timer can be employed to indicate to the µController that a NOTONE situation has existed for a predetermined period.

This timer register can be written-to and set in any mode of the FX803.

The NOTONE Timer period is 'primed' by writing to the NOTONE Timer Register ($33_H$) using the settings given in Table 6.

*"Priming" sets the timing period;* ***this period can only start directly after a frequency (tone) measurement has been successfully completed.***

The NOTONE Timer is a one-shot timer being reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down.

On completion of the preset period, the NOTONE Timer Period Expired bit in the Status Register and the Interrupt (when enabled, *Table 2*) are set.

Upon detection of the Interrupt, the Status Register should be read by the µController to ascertain the source of the Interrupt.

The NOTONE Timer Period Expired bit is cleared:

i By a read of the Status Register or,
ii New NOTONE Timer information or,
iii General Reset command

This timer is set to $00_H$ (0ms) by a General Reset command.

---

The following situations may be encountered by the NOTONE Timer circuitry:

### No Signal

The NOTONE Timer can only start its run down on completion of a valid frequency measurement.

### No Signal after a Valid Tone Measurement

The timer will start to run down when the last Rx Tone Measurement complete bit is set. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

### Signal Fades after a Valid Tone Measurement

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

### Signal Appears after the Timer has Started

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

## Controlling Protocol...

### "Write to General Purpose Timer Register" – A/C $36_H$ followed by 1 byte of Command Data.

| Setting | | | | Function/Period | | | | |
|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | | |
| 7 | 6 | 5 | 4 | Transmitted Bit 7 First | | | | |
| 0 | 0 | 0 | 0 | These 4 bits must be "0" | | | | |
| 3 | 2 | 1 | 0 | High/Extended Band | | Mid Band | | |
| | | | | Reset Timer and Start Timing | | | | |
| 0 | 0 | 0 | 0 | Period of | 0 | | 0 | |
| 0 | 0 | 0 | 1 | " | 10 ms | ±1% | 20 ms | ±1% |
| 0 | 0 | 1 | 0 | | 20 | " | 40 | " |
| 0 | 0 | 1 | 1 | | 30 | " | 60 | " |
| 0 | 1 | 0 | 0 | | 40 | " | 80 | " |
| 0 | 1 | 0 | 1 | | 50 | " | 100 | " |
| 0 | 1 | 1 | 0 | | 60 | " | 120 | " |
| 0 | 1 | 1 | 1 | | 70 | " | 140 | " |
| 1 | 0 | 0 | 0 | | 80 | " | 160 | " |
| 1 | 0 | 0 | 1 | | 90 | " | 180 | " |
| 1 | 0 | 1 | 0 | | 100 | " | 200 | " |
| 1 | 0 | 1 | 1 | | 110 | " | 220 | " |
| 1 | 1 | 0 | 0 | | 120 | " | 240 | " |
| 1 | 1 | 0 | 1 | | 130 | " | 260 | " |
| 1 | 1 | 1 | 0 | | 140 | " | 280 | " |
| 1 | 1 | 1 | 1 | | 150 | " | 300 | " |

*Table 7 General Purpose Timer Settings*

#### Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the FX803, can be employed within the DBS 800 system to indicate time-elapsed periods of between 10ms and 150ms in the High/Extended Band, 20ms and 300ms in the Mid Band, to the µController.

Setting of the timer is by loading a single-byte data word via the "C-BUS," as indicated in Table 7 (left), to the FX803 via the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (Bit 2) in the Status Register and the Interrupt (if enabled) are set.

The General Purpose Timer Expired bit is cleared:

i By a read of the Status Register, or
ii New G/P Timer information, or
iii General Reset command.

When the programmed time period has expired, this timer will reset, restart and continue sequencing until;

i New G/P Timer information is written, or
ii A General Reset command.

The General Purpose Timer Expired bit and the Interrupt will remain set until cleared.

This timer is set to $00_H$ (0ms) by a General Reset command.

---

## Powersave

Various sections of the FX803 can be placed independently into a power economical condition. Table 8 (below) gives a brief summary of the inactive, power-economical states available to the FX803.

| Powersaved Section | Instruction Source | | Table |
|---|---|---|---|
| Tone Encoder 1 | Tx Tone Gen.1 Reg. ($34_H$) | All bits = "0" | 4 |
| Tone Encoder 2 | Tx Tone Gen.2 Reg. ($35_H$) | All bits = "0" | 5 |
| Summing Amplifier | This action is automatic when both Tone Encoders are in the powersave condition. | | |

*Table 8 FX803 Powersave Functions*

#### Powersave Conditions

**Xtal/Clock and "C-BUS"**: This circuitry is always active, on all DBS 800 microcircuits, under any powered/powersaved conditions.

# Controlling Protocol...

## Interrupt Requests

An Interrupt (IRQ), when enabled, is provided by the FX803 to indicate the following conditions to the µController.

**NOTONE Timer Period Expired**

**Enabled:** By Control Register Bit 5.

**Set:** When the preset Notone Flag is set.

**Identified:** By Status Register Bit 1.

**Cleared:** By reading the Status Register.

**G/Purpose Timer Period Expired**

**Enabled:** By Control Register Bit 6.

**Set:** When the General Purpose Timer has timed out.

**Identified:** By Status Register Bit 2.

**Cleared:** By reading the Status Register.

**Rx Tone Measurement Complete**

**Enabled:** By Control Register Bit 5.

**Set:** When an Rx Frequency Measurement has been successfully completed.

**Identified:** By Status Register Bit 0.

**Cleared:** By reading the Status Register.

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status Bits are transferred to the µController via the "C-BUS" Reply Data line and the internal Status Bits are cleared.

## Operational Recommendations

It is recommended that, following initial System power-up a General Reset command is sent to the FX803.

### Receive Sequence

1. Send Control Command for Rx:
   Select Midband/Highband and Digital Filter length.
2. Disable transmitters, if desired by writing to Tone Frequency registers.
3. Prime the NOTONE Timer by sending the required period byte.
4. Enable Decoder interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt sent to the µC.
6. The µC examines the Status Register, if tone measurement is complete, reads in the Rx Tone Frequency in the form N + R (Figure 6).
7. Rx Tone Measurement Complete interrupts are periodically sent to the µC unless NOTONE is detected, in which case a NOTONE Interrupt is sent.

### Transmit Control Sequence

1. Set Tone Frequency Generators to $V_{BIAS}$ (setting both tone generators (Bit 13 = "1")) during the transmitter initialization period.
2. Send Control Command for Tx:
   Select Sum/Switched Sum o/p and Audio Switch states.
3. Send General Purpose (GP) Timer information for the $V_{BIAS}$ (NOTONE) transmitter initialization period (Step 1). This will initiate the timer.
4. Enable the General Purpose Timer interrupt.
5. µC waits for "GP Timer Expired;" Reads the Status Register to check interrupt due to timer; Resets the Status Bit.
   If required, the µC sends the next timer period followed by the next tone(s) frequency information.
   A new timer period sent will reset the timer, otherwise the timer is self-sequencing.
6. The µC monitors the interrupts and repeats 5 & 6 as required.
7. After last loaded tone the µC turns off the Tone Generator(s) by setting tone outputs to $V_{BIAS}$ (NOTONE) (Tables 4 and 5).

## General Reset

Upon Power-Up the "bits" in the FX803 registers will be random (either "0" or "1"). A General Reset Command ($01_H$) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX803.

| | |
|---|---|
| Control Reg. | Set as $00_H$ |
| Status Reg. Bits 0, 1, 2.) | Set as $00_H$ |
| NOTONE Timer Reg. | Set as $00_H$ |
| Tone Gen. 1 Reg. (2 bytes) | Set as $0000_H$ |
| Tone Gen. 2 Reg. (2 bytes) | Set as $0000_H$ |
| Gen/Purpose Reg. | Set as $00_H$ |

Sets the FX803 to:
Encoder High Band (625Hz to 3000Hz) – with interrupts disabled, both timers set to $00_H$.

It is recommended that both timers are set-up before interrupts are enabled, to prevent initial, undesired interrupts.

## Glossary of Abbreviations

Below is a list of abbreviations used within this Data Sheet.

| | |
|---|---|
| $f_{XTAL}$ | Xtal/clock frequency |
| $S_{INPUT}$ | Audio input signal |
| $f_{TONE}$ | Tone frequency |

# Timing Information

## Timing Diagrams

Figure 7 shows the timing parameters for two-way communication between the µController and the FX803 on the "C-BUS." Figure 8 shows, in detail, the timing relationships for "C-BUS" information transfer.

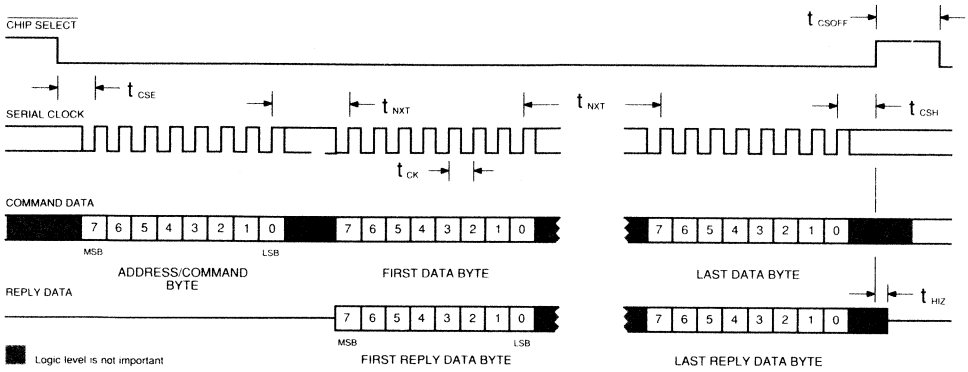



*Fig.7 "C-BUS" Timing Information*

*NOT TO SCALE*

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $t_{CSE}$ | 2.0 | – | – | µs |
| $t_{CSH}$ | 4.0 | – | – | µs |
| $t_{CSOFF}$ | 2.0 | – | – | µs |
| $t_{NXT}$ | 4.0 | – | – | µs |
| $t_{CK}$ | 2.0 | – | – | µs |
| $t_{CH}$ | 500 | – | – | ns |
| $t_{CL}$ | 500 | – | – | ns |
| $t_{CDS}$ | 250 | – | – | ns |
| $t_{CDH}$ | 0 | – | – | ns |
| $t_{RDS}$ | 250 | – | – | ns |
| $t_{RDH}$ | 50.0 | – | – | ns |
| $t_{HIZ}$ | – | – | 2.0 | µs |

**Notes**

(1) Command Data is transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. Reply Data is read from the FX803 MSB (Bit 7) first, LSB (Bit 0) last.
(2) Data is clocked into the FX803 and into the µController on the rising Serial Clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX803 will work with either polarity Serial Clock pulses.

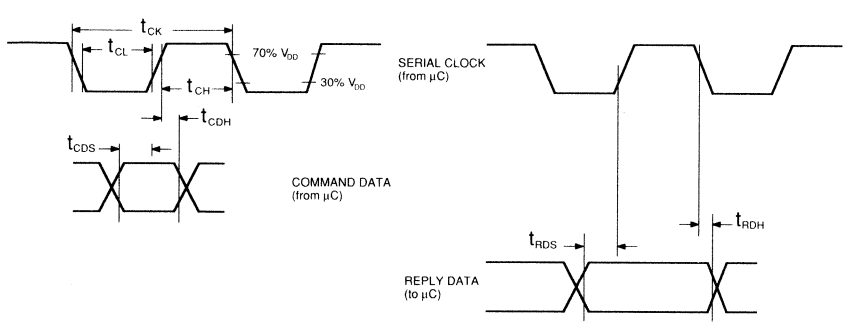



*Fig.8 "C-BUS" Timing Relationships*

*NOT TO SCALE*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX803J** | -40°C to +85°C (cerdip) |
| | **FX803LG/LS** | -40°C to +85°C (plastic) |
| Storage temperature range: | **FX803J** | -55°C to +125°C (cerdip) |
| | **FX803LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock ($f_{XTAL}$) = 4.032MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz *(60% deviation, FM).*

Noise Bandwidth = 5.0kHz Band-Limited Gaussian.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | | | | |
| (Decoder + Both Timers) | | – | 2.0 | – | mA |
| (Decoder + Both Timers + One Tx only) | | – | 4.0 | – | mA |
| (All Functions Enabled) | | – | 5.0 | – | mA |
| **Analogue Impedances** | | | | | |
| (Rx) Audio Input | | – | 20.0 | – | MΩ |
| Summing Amp Input | | – | 20.0 | – | MΩ |
| Switch | | – | 1.0 | – | kΩ |
| Tones 1 and 2 Outputs | | – | 10.0 | – | kΩ |
| CAL/CUES Output | | – | 5.0 | – | kΩ |
| Summing Outputs | | – | 10.0 | – | kΩ |
| **Dynamic Values** | | | | | |
| **Digital Interface** | | | | | |
| Input Logic "1" | 1 | 3.5 | – | – | V |
| Input Logic "0" | 1 | – | – | 1.5 | V |
| Output Logic "1" (IOH = -120µA) | 2 | 4.6 | – | – | V |
| Output Logic "0" (IOL = 360µA) | 3 | – | – | 0.4 | V |
| $I_{OUT}$ Tristate (Logic "1" or "0") | 3 | – | – | 4.0 | µA |
| Input Capacitance | 1 | – | – | 7.5 | pF |
| IOX ($V_{OUT}$ = 5.0V) | 4 | – | – | 4.0 | µA |
| **Overall Performance** | | | | | |
| **Rx – Decoding** | | | | | |
| **High-Band** | | | | | |
| Sensitivity | | – | -20.0 | – | dB |
| Tone Response Time | | | | | |
| Good Signal | 5 | – | – | 30.0 | ms |
| Tone-to-Noise Ratio = 0dB | 5, 6 | – | – | 40.0 | ms |
| Frequency | | | | | |
| Band | | 625 | | 3000 | Hz |
| Measurement Resolution | | – | 0.2 | – | % |
| Measurement Accuracy | 9 | – | 0.5 | – | % |

## Specification...

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Rx – Decoding .....** | | | | | |
| **Mid-Band** | | | | | |
| Sensitivity | | – | -20.0 | – | dB |
| Tone Response Time | | | | | |
| Good Signal | 7 | – | – | 60.0 | ms |
| Tone-to-Noise Ratio = 0dB | 6, 7 | – | – | 80.0 | ms |
| Frequency | | | | | |
| Band | | 313 | | 1500 | Hz |
| Measurement Resolution | | – | 0.2 | – | % |
| Measurement Accuracy | 9 | – | 0.5 | – | % |
| **Extended-Band** | | | | | |
| Sensitivity | | – | -20.0 | – | dB |
| Tone Response Time | | | | | |
| Good Signal | 5 | – | – | 20.0 | ms |
| Frequency | | | | | |
| Band | | 1250 | | 6000 | Hz |
| Measurement Resolution | | – | 0.2 | – | % |
| Measurement Accuracy | 9 | – | 0.5 | – | % |
| **Tx – Encoders 1 and 2** | | | | | |
| Tone Frequency | | 208 | | 3000 | Hz |
| Period ($1/f_{TONE}$) Error | | – | – | 1.0 | µs |
| Tone Amplitude | | -1.5 | – | +1.5 | dB |
| Total Harmonic Distortion | | – | – | 5.0 | % |
| Rise Time to 90% | | – | $3/f_{TONE}$ | – | secs |
| Fall Time to 10% | 8 | – | – | 5.0 | ms |
| Frequency Change Time | | – | $3/f_{TONE}$ | – | secs |
| **Timers** | | | | | |
| **General Purpose** | | | | | |
| Timing Period Range | | | | | |
| High-Band | | 10.0 | | 150 | ms |
| Mid-Band | | 20.0 | | 300 | ms |
| **Rx NOTONE** | | | | | |
| Timing Period Range | | | | | |
| High-Band | | 20.0 | | 300 | ms |
| Mid-Band | | 40.0 | | 600 | ms |
| **Xtal/Clock Frequency** ($f_{XTAL}$) | | 3.9 | – | 4.1 | MHz |

**Notes**

1. Device control pins; Serial Clock, Command Data, and CS.
2. Reply Data output.
3. Reply Data and IRQ outputs.
4. Leakage current into the "Off" IRQ output.
5. Measurement Period = 9.125ms.
6. Decode Probability = 0.993.
7. Measurement Period = 18.250ms.
8. When set to Powersave.
9. For a good input signal.

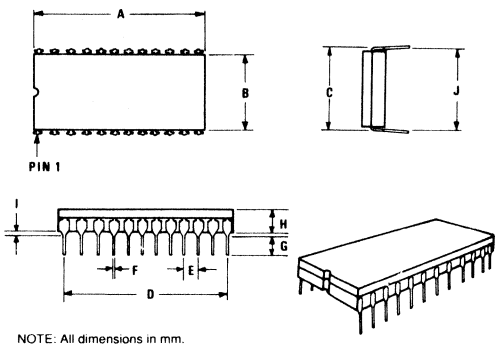
## Package Outline

The FX803J, the dual-in-line package, is shown in Figure 9. The 'LG' version is shown in Figure 10 and the 'LS' version in Figure 11.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX803 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

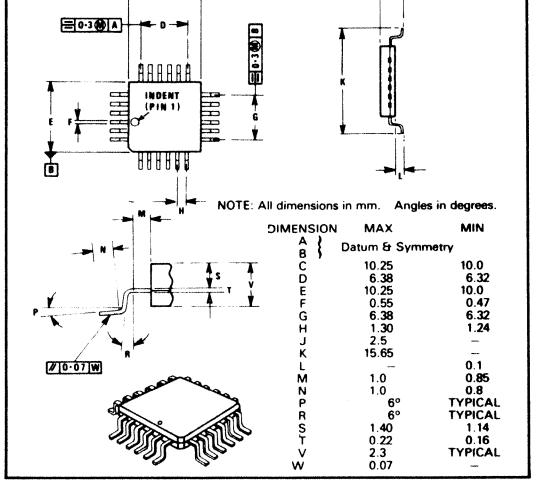
*Fig. 9* **FX803J** *24-pin DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. | DIMENSION | MAX. | MIN. |
|---|---|---|---|---|---|
| A | 32.03 | 31.50 | F | 0.46 | TYPICAL |
| B | 14.81 | 13.06 | G | 4.30 | 4.10 |
| C | 15.61 | 15.14 | H | 4.35 | 3.99 |
| D | 28.04 | 27.84 | I | 1.40 | TYPICAL |
| E | 2.54 | TYPICAL | J | 18.20 | 16.54 |

*Fig. 10* **FX803LG** *24-pin Package*



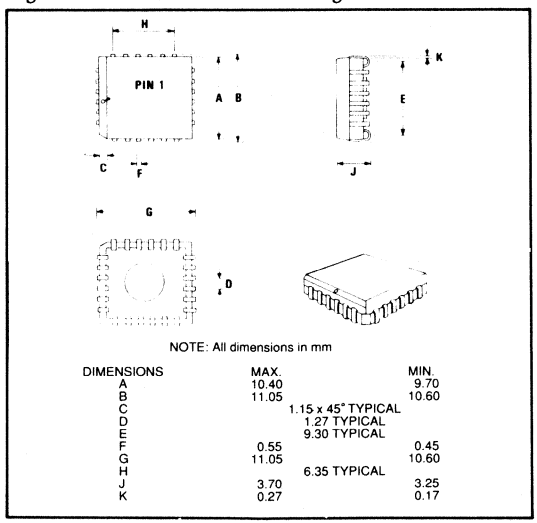

NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

## Ordering Information

| | |
|---|---|
| **FX803J** | 24-pin cerdip DIL |
| **FX803LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX803LS** | 24-lead plastic leaded chip carrier |

*Fig. 11* **FX803LS** *24-lead Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

# FX805 Sub-Audio Signalling Processor

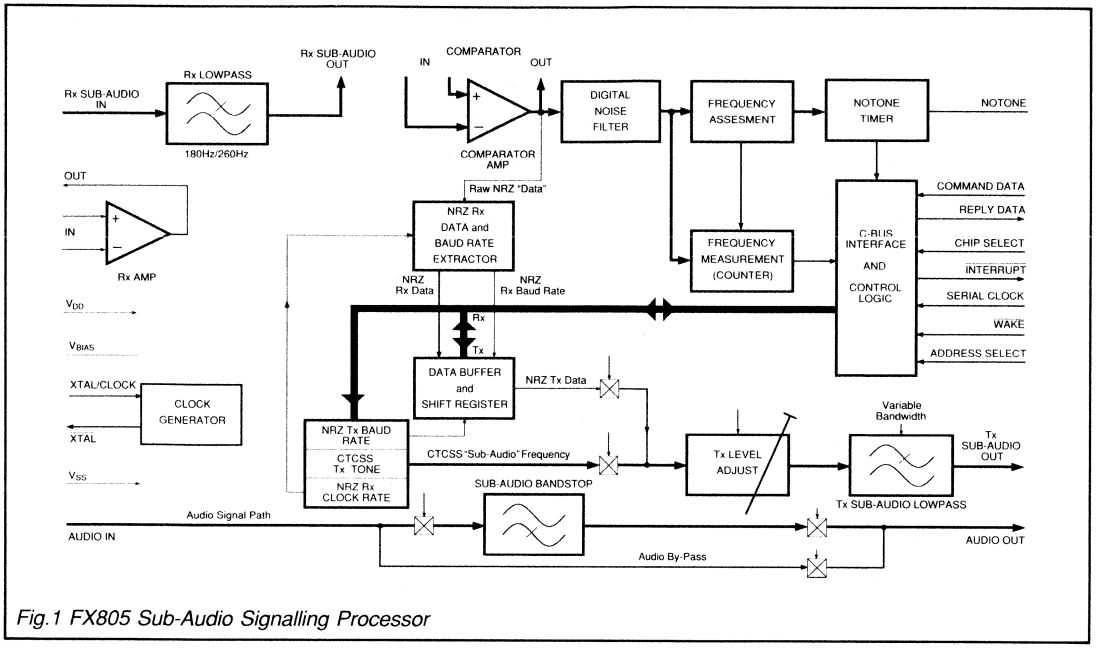



*Fig.1 FX805 Sub-Audio Signalling Processor*

## FX805 Sub-Audio Signalling Processor

A µProcessor controlled, sub-audio frequency signalling processor to provide an outband audio and digital signalling facility for PMR radio systems.

This device caters for the transmission and non-predictive reception of:

- *Continuous Tone Controlled Squelch (CTCSS) tones and other non-standard sub-audio frequencies.*
- *Non-Return-to-Zero (NRZ) data to facilitate Continuous Digitally Coded Squelch (CDCS/DPL™ ) system operations.*

To achieve these functions, the FX805 has on-chip:

- *A non-predictive CTCSS Tone Decoder and CDCS sub-audio signal demodulator.*
- *A CTCSS/NRZ Encoder with Tx level adjustment and lowpass filter output stage with optional NRZ pre-emphasis.*
- *A selectable sub-audio bandstop filter.*
- *A Notone (CTCSS Rx) period timer.*

Setting of the FX805 functions and modes is by data loaded from the µController to the controlling registers within the device. Reply Data and Interrupt protocol keep the µController up to date on the operational status of the circuitry — all via the "C-BUS" interface.

**CTCSS** tone data for transmission is generated within the µController, loaded to CTCSS Tx Frequency Register, encoded and output as a tone via the Tx Sub-Audio Lowpass Filter.

Received non-predicted CTCSS tone frequencies are measured and the resulting data, in the form of a 2-byte data-word, is presented via the CTCSS Rx Frequency Register to the µController for matching against a 'look-up' table. Noise filtering is provided to improve the signal quality prior to measurement.

**NRZ** coded data streams for transmission, when generated within a µController, are loaded to the NRZ Tx Data Buffer and output, in 8-bit bytes, through the Lowpass Filter circuitry as sub-audio signals. CDCS turn-off tones can be added to the data signals by switching the FX805 to the CTCSS transmit mode at the appropriate time.

NRZ coding is produced by the µController and translated into sub-audio signals by the FX805.

Received NRZ data is filtered, detected and placed into the NRZ Rx Data Register which is then available for transfer one byte at a time, to the µController, for decoding by software. Clock extraction circuitry is provided on chip and Rx and Tx baud rates are selectable.

Provision is made in both hardware and system software allocations to address two FX805 Sub-Audio Signalling Processors consecutively to achieve multi-mode, duplex operation.

The FX805 has a powersaving function which may be controlled by software or a dedicated (Wake) input.

The FX805 is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.



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## Pin Number Function

| FX805 J/LG/LS | |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal ($f_{XTAL}$) input is used. See Figure 2. |
| 2 | **Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock ($f_{XTAL}$) should be connected here. See Figure 2. |
| 3 | **Address Select:** This pin enables two FX805 devices to be used on the same "C-BUS," providing full-duplex operation. See Tables 1 and 2. |
| 4 | **Interrupt Request ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The System IRQ line requires 1 pullup resistor to $V_{DD}$. The conditions that cause interrupts are indicated in the Status Register (Table 4) and are shown below:<br>*Rx CTCSS Tone Measurement Complete*<br>*1 NRZ Rx Data Byte Received*<br>*NRZ Tx Buffer Ready*<br>*CTCSS NOTONE Timer Expired*<br>*New NRZ Rx Data Received Before Last Byte Read*<br>*NRZ Data Transmission Complete* |
| 5 | **Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the Sub-Audio Signalling Processor. See Timing Diagrams. |
| 6 | **Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams. |
| 7 | **Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CS signal. See Timing Diagrams. |
| 8 | **Reply Data:** The "C-BUS" serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams. |
| 9 | **Tx Sub-Audio Out:** The sub-audio output (pure or NRZ derived). Signals are band-limited, the Tx Output Filter has a variable bandwidth, see Table 6. This output is at $V_{BIAS}$ (a) when the NRZ Encoder is enabled but no data is being transmitted, (b) when the FX805 is placed in the Powersave All condition. |
| 10 | **Audio In:** The input to the switched sub-audio bandstop (highpass) filter. This input is internally biased and requires to be a.c. coupled by capacitor $C_7$. |
| 11 | **Audio Out:** The output of the 'audio signal path' (filter or by-pass). This output is controlled by the Control Register and when disabled is held at $V_{DD}/2$. |
| 12 | **$V_{SS}$:** Negative Supply (Signal Ground). |

## Pin Number Function

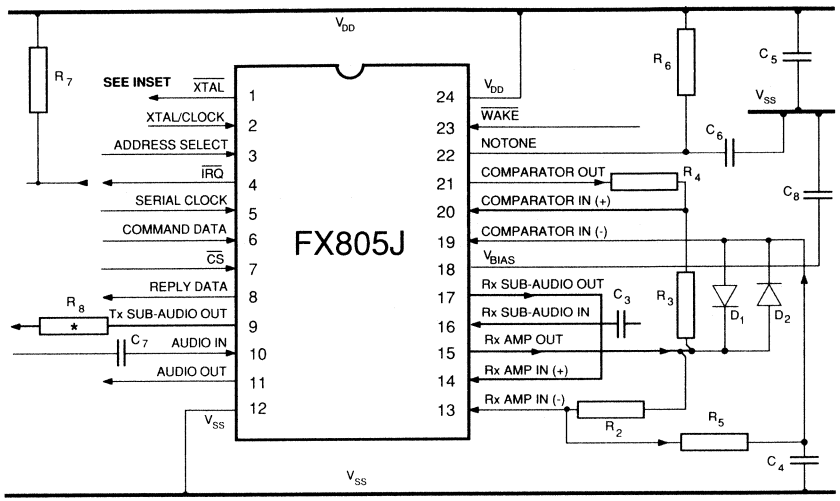
| FX805 J/LG/LS | |
|---|---|
| 13 | **Rx Amp (-) In:** The inverting input to the on-chip Rx Input Amp. See Figures 2, 3 and 4. |
| 14 | **Rx Amp (+) In:** The non-inverting input to the on-chip Rx Input Amp. |
| 15 | **Rx Amp Out:** The output of the on-chip Rx Input Op-Amp. This circuit may be used, with external components, as a signal amplifier and an anti-aliasing filter prior to the Rx Lowpass Filter, or for other purposes. See Figure 2 for component details. |
| 16 | **Rx Sub-Audio In:** The received sub-audio (CTCSS/NRZ) input. This input is internally biased to $V_{DD}/2$ and requires to be a.c. coupled or biased. See Figure 2 for component details. |
| 17 | **Rx Sub-Audio Out:** The output of the Rx Lowpass Filter. This output may be coupled into the on-chip amplifier or comparator as required. |
| 18 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$ by capacitor $C_8$ (see Figure 2). |
| 19 | **Comparator In (-):** The inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4. |
| 20 | **Comparator (+):** The non-inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4. |
| 21 | **Comparator Out:** The output of the "comparator" amplifier. This node is also internally connected to the input of the Digital Noise Filter (see Figure 1). When both decoders are Powersaved, this output is at a logic "0." |
| 22 | **NOTONE Timing:** External RC components connected to this pin form the timing mechanism of a NOTONE period timer. The external network determines the 'charge-rate' of the timer to $V_{DD}/2$. Expiry of the timer will cause an interrupt. This facility is only used in the CTCSS Rx mode. See Page 11. |
| 23 | **$\overline{\text{Wake}}$:** This 'real-time ' input can be used to reactivate the FX805 from the 'Powersave All' condition using an externally derived signal. The FX805 will be in a 'Powersave All' condition when both this pin and Bit 0 of the Control Register are set to a logic "1." Recovery from "Powersave All" is achieved by putting either the Wake pin or the 'Powersave All' bit to logic "0," thus allowing FX805 activation by the µController or an external signal, such as R.S.S.I. or Carrier Detect. |
| 24 | **$V_{DD}$:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the Sub-Audio Signalling Processor are dependant upon this supply. |

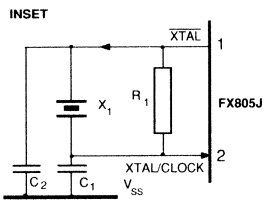
**NOTE:** (i) Further information on external components and DBS 800 system integration of this microcircuit are contained in the System Support Document, Document 2.
(ii) A glossary of abbreviations used in this document can be found on Page 9.
(iii) Guidance upon the generation and manipulation of NRZ Rx and Tx data is given in DBS 800 Application Support Document, Document 4.

***"C-BUS"** is CML's proprietry standard for the transmission of commands and data between a µController and DBS 800 microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined soley by the µController.*

# Application Information

## External Components




| Component | Value | Component | Value | Component | Value |
|---|---|---|---|---|---|
| $R_1$ = | 1.0MΩ | $R_9$ = | Fig.4 | $C_6$ = | 1.0µF |
| $R_2$ | 360kΩ | $R_{10}$ | Fig.4 | $C_7$ | 0.1µF |
| $R_3$ | 10.0kΩ | $R_{11}$ | Fig.4 | $C_8$ | 1.0µF |
| $R_4$ | 150kΩ | $C_1$ | 33.0pF | $C_9$ | Fig.4 |
| $R_5$ | 100kΩ | $C_2$ | 33.0pF | $D_1$ | silicon small sig |
| $R_6$ | 150kΩ | $C_3$ | 1.5µF | $D_2$ | silicon small sig |
| $R_7$ | 22.0kΩ | $C_4$ | 15.0µF | $X_1$ | $f_{XTAL}$ 4.00MHz |
| $R_8$ | 360kΩ | $C_5$ | 1.0µF | | |

*Fig.2 Recommended External Components*

### Notes *on external components and connections*

1. Xtal/clock circuitry components shown INSET are recommended in accordance with CML Application Note D/XT/1 April 1986. The DBS 800 System Information Document contains additional notes on Xtal/clock distribution and frequencies.
2. $R_8$ is a System Component. Its value is chosen, for example, with the FX806 Modulation Summing Amplifier, to provide a sub-audio signal level of -11.0dB to the system modulator.
3. Components $R_6$ and $C_6$ are NOTONE timing components.
4. $R_2$ and $R_5$ are dependant upon the input signal level. Values given are for the specified composite signal (Page 16).
5. $R_7$ is used as the DBS 800 system common-pullup for the "C-BUS" Interrupt Request (IRQ) line, the optimum value of this component will depend upon the circuitry connected to the IRQ line.

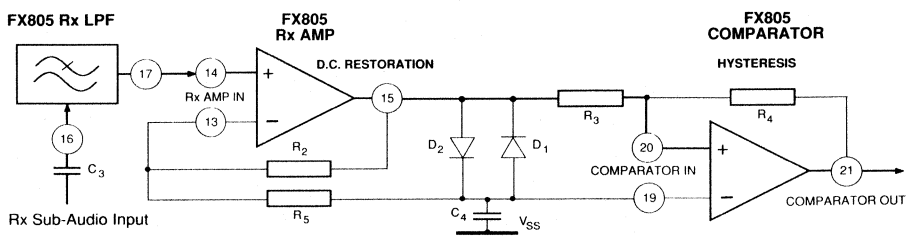



*Fig.3 Employment of FX805 Input Components*

With reference to Figure 2, Figures 3 and 4 show in detail recommended alternative component configurations for the FX805.

# Application Information...

## External Components .....

Figure 3 shows an input component configuration for use generally for CTCSS signal and NRZ data reception.

Input coupling capacitor $C_3$ is required because the Rx Sub-Audio Input is held at $V_{BIAS}$ during all powered conditions of the FX805. Diodes $D_1$ and $D_2$ can be any silicon small-signal diode.

The output resistance (open loop) of the on-chip Rx Amp is ≈ 6kΩ. In the configuration shown in Figure 3, the (Rx Amp) RC time-constant is therefore 90ms. If this period is too long for some systems, ie. those employing half-duplex, short data bursts, an external amplifier should be considered in place of the FX805 on-chip Rx Amp.

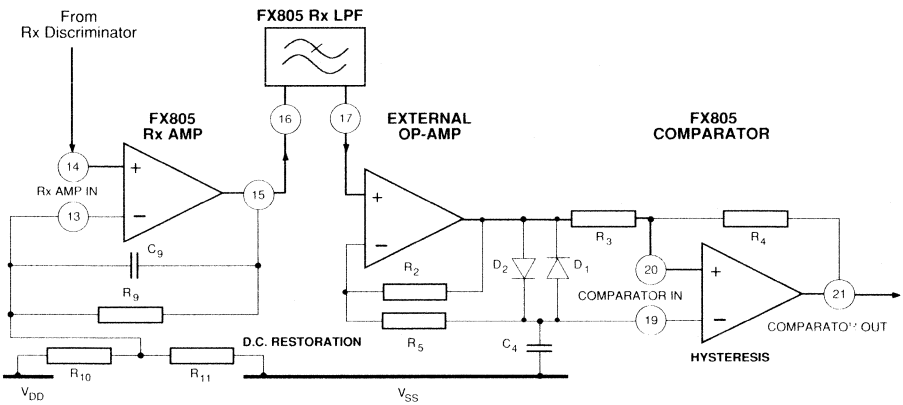



*Fig.4 FX805 Input Components Using an External Op-Amp*

### Using an External Op-Amp

For d.c. coupling the FX805 to the receiver's discriminator output when using NRZ communication, it is recommended that an additional, external Op-Amp is employed as configured in Figure 4. This configuration will allow long sequences of logic "1s" or "0s" to be successfully decoded (eg. LTR™ trunking systems).

Components $R_9$, $R_{10}$ and $R_{11}$ should be calculated to provide an accurate potential of 2.5V d.c. (equal to $V_{BIAS}$) at pin-junction 15/16 when using a discriminator input. $C_9$ is an optional component which, if additional filtering is required, should be calculated, with $R_9$ to provide a lowpass cut-off frequency ($f_{CO}$) of 500Hz.

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# FX805 Operational Modes

### NRZ Tx (Encoding)

The NRZ Encoder is formed by a shift register and the Tx Sub-Audio Lowpass Filter. Data loaded from the Command Data line is output one 8-bit byte at a time from the NRZ Tx Data Register. The output data-signal level may be adjusted and filtered. Data may be pre-emphasized via a "C-BUS" command. The Tx baud rate is programmed as the NRZ Tx Baud Rate ($R_{NRZ\,Tx}$) (Table 5/Page 13).

### CTCSS Tx (Encoding)

The CTCSS Tone Encoder comprises a clock-divider programmed by an 11-bit binary number (Q) loaded to the CTCSS Tx Frequency Register (Table 5) via the "C-BUS" Command Data line.

The square-wave output of the encoder is fed through the Tx Level Adjust variable gain block to the Tx Sub-Audio Lowpass Filter, a variable bandwidth circuit controlled by 4-bits (P) of the CTCSS Tx Frequency Register. The Tx Sub-Audio output is a sine-wave. Standard and non-standard sub-audio tones are available, a 'CDCS' turn-off tone may be generated.

### NRZ Rx (Decoding)

Input (NRZ type) sub-audio signals are filtered and the data clock extracted. Decoded data is serially loaded into a shift register buffer. This data is output one 8-bit byte at a time as Reply Data from the NRZ Rx Data Register (Page 14) to the μController. The expected Rx baud rate is programmed as the NRZ Rx Baud Rate ($R_{NRZ\,Rx}$) (Table 5). Any codeword recognition can be carried out by software.

### CTCSS Rx ( Decoding)

Received CTCSS signals are filtered, coherence is increased by the digital noise filter. The quality of the signal is assessed by measurement of the cycle-to-cycle period variance and, provided it is sufficiently good, the frequency is measured over a period of 122.64 milliseconds.

If the average signal quality is consistently too low, NOTONE is indicated, if not, the input frequency is precisely indicated in the CTCSS Rx Frequency Register in a binary form as shown in Figure 6.

As any single sub-audio tone within the specified range may be selected, this would enable a 'CDCS' turn-off tone (of 134Hz) to be decoded whilst operating in the NRZ Rx mode.

## Controlling Protocol

Control of the FX805 Sub-Audio Signalling Processor's operation is by communication between the µController and the FX805 internal registers on the "C-BUS," using Address/Commands (A/Cs) and appended instructions or data (see Figure 9). The use and content of these instructions is detailed in the following paragraphs and tables. The Address Select input enables the addressing of 2 separate FX805s on the "C-BUS" to provide full-duplex multi-mode signalling.

## FX805 Internal Registers

FX805 internal registers are detailed below:

**Control** Register ($70_H/78_H$) – Write only, control and configuration of the FX805. Page 9.

**Status** Register ($71_H/79_H$) – Read Only, reporting of device functions. Page 10.

**CTCSS Rx Frequency** Register ($72_H/7A_H$) – Read Only, a 2-byte binary word indicating the frequency of the received sub-audio input. Page 11.

**CTCSS Tx Frequency / NRZ Tx or Rx Baud Rate** Register ($73H/7B_H$) – Write Only, a 2-byte command to set the relevant parameters. Page 12.

**NRZ Rx Data** Register ($74_H/7C_H$) – Read Only, a single-byte of received NRZ data. Page 14.

**NRZ Tx Data** Register ($75_H/7D_H$) – Write Only, to load a single-byte of NRZ data for transmission one byte at a time. Page 14.

**Gain-Set** Register ($76_H/7E_H$) – Write Only, a single byte to set the gain of the Tx Lowpass Filter. Page14.

## Address/Commands

The first byte of a loaded data sequence is always recognized by the "C-BUS" as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data or,

(ii) a Status or data Reply.

Instructions and data are loaded and transferred, via "C-BUS," in accordance with the timing information given in Figures 9 and 10.

Placing the Address Select input at a logic "0" will address FX805 No.1, a logic "1" will address FX805 No.2.

Tables 1 and 2 show the list of A/C bytes relevant to the FX805. A complete list of DBS 800 "C-BUS" Address allocations is published in the System Support Document, Document 2.

| Command Assignment | Address/Command (A/C) Byte Hex. | Binary MSB LSB | + | Data Byte/s |
|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | |
| Write to Control Reg. | 70 | 0 1 1 1 0 0 0 0 | + | 1 byte Instruction to Control Reg. |
| Read Status Reg. | 71 | 0 1 1 1 0 0 0 1 | + | 1 byte Reply from Status Reg. |
| Read CTCSS Rx Freq. Reg. | 72 | 0 1 1 1 0 0 1 0 | + | 2 byte Reply of CTCSS Rx data |
| Write to CTCSS Tx Frequency/ NRZ Baud Rate Reg. | 73 | 0 1 1 1 0 0 1 1 | + | 2 byte Instruction for Tx Frequency and NRZ Tx/Rx baud rates |
| Read NRZ Rx Data Reg. | 74 | 0 1 1 1 0 1 0 0 | + | 1 byte binary data Reply |
| Write to NRZ Tx Data Reg. | 75 | 0 1 1 1 0 1 0 1 | + | 1 byte binary data Command |
| Write to Gain-Set Reg. | 76 | 0 1 1 1 0 1 1 0 | + | 1 byte Instruction for Tx Output |

*Table 1 – FX805 No.1 "C-BUS" Address/Commands* Address Select input at a logic "0"

| Command Assignment | Address/Command (A/C) Byte Hex. | Binary MSB LSB | + | Data Byte/s |
|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | |
| Write to Control Reg. | 78 | 0 1 1 1 1 0 0 0 | + | 1 byte Instruction to Control Reg. |
| Read Status Reg. | 79 | 0 1 1 1 1 0 0 1 | + | 1 byte Reply from Status Reg. |
| Read CTCSS Rx Frequency Reg. | 7A | 0 1 1 1 1 0 1 0 | + | 2 byte Reply of CTCSS Rx data |
| Write to CTCSS Tx Frequency/ NRZ Baud Rate Reg. | 7B | 0 1 1 1 1 0 1 1 | + | 2 byte Instruction for Tx Frequency and NRZ Tx/Rx baud rates |
| Read NRZ Rx Data Reg. | 7C | 0 1 1 1 1 1 0 0 | + | 1 byte binary data Reply |
| Write to NRZ Tx Data Reg. | 7D | 0 1 1 1 1 1 0 1 | + | 1 byte binary data Command |
| Write to Gain-Set Reg. | 7E | 0 1 1 1 1 1 1 0 | + | 1 byte Instruction for Tx Output |

*Table 2 – FX805 No.2 "C-BUS" Address/Commands* Address Select input at a logic "1"

## "Write to Control Register" – A/C $70_H$ ($78_H$), followed by 1 byte of Command Data.

Table 3 (below) shows the configurations available to the FX805. Bits 5, 6 and 7 are used together to Enable and Powersave circuit sections as required.

| *Setting* | | | *Control Bits* | |
|---|---|---|---|---|
| *MSB* | | | *Transmitted First* | |
| *7* | *6* | *5* | **Functions Enabled** | **Functions Powersaved** |
| 0 | 0 | 0 | CTCSS Decoder | NRZ Decoder and Both Encoders |
| 0 | 0 | 1 | NRZ Decoder | CTCSS Decoder and Both Encoders |
| 0 | 1 | 0 | CTCSS Encoder | All Decoders |
| 0 | 1 | 1 | NRZ Encoder | All Decoders |
| 1 | 0 | 0 | CTCSS Encoder and Decoder | NRZ Encoder and Decoder |
| 1 | 0 | 1 | NRZ Encoder and CTCSS Decoder | None |
| 1 | 1 | 0 | NRZ Decoder and CTCSS Decoder | All Encoders |
| 1 | 1 | 1 | NRZ Decoder | All Encoders (except Tx Sub-Audio LPF) and CTCSS Decoder |

| | |
|---|---|
| ***4*** | |
| 1 | Enable Audio Output – Used with Bit 3 |
| 0 | Disable Audio Output – Output to $V_{BIAS}$ |
| ***3*** | |
| 1 | Enable Sub-Audio Bandstop Filter (Audio Signal Path) |
| 0 | By-pass Sub-Audio Bandstop Filter |
| ***2*** | |
| 1 | Enable All FX805 Interrupts |
| 0 | Disable All FX805 Interrupts |
| ***1*** | |
| 1 | Set Rx Lowpass Filter bandwidth to 180Hz – For low CTCSS Tones or NRZ Data |
| 0 | Set Rx Lowpass Filter bandwidth to 260Hz |
| ***0*** | |
| 1 | All Encoders and Decoders Powersaved (Powersave All) |
| 0 | All Encoders and Decoders Enabled unless individually Powersaved |

*Table 3 Control Register*

## General Reset

Upon Power-Up the "bits" in the FX805 registers will be random (either "0" or "1"). A General Reset Command ($01_H$) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX805.

| | |
|---|---|
| *Control Register* | *Set as $00_H$* |
| *Status Register* | *Set as $00_H$* |
| *NOTONE Timer* | *Discharged* |

**Warning** – The following FX805 register configurations are not affected by a General Reset command:

*CTCSS Rx Frequency*
*CTCSS Tx Frequency/NRZ Baud Rate Register*
*NRZ Rx Data Register*
*NRZ Tx Data Register*
*Gain-Set Register*

Note that setting the Control Register in this way (General Reset) will set the FX805 to the CTCSS Decode mode and overwrite a "Powersave All" instruction.

It should also be considered that a General Reset command will reset ALL DBS 800 microcircuits operating on the "C-BUS."

## Glossary of Abbreviations

Below is a list of abbreviations used within this Data Sheet.

| | |
|---|---|
| CDCS | Continuous Digitally Coded Squelch |
| CTCSS | Continuous Tone Controlled Squelch |
| DPL™ | Digital Private Line |
| LTR™ | Logic Trunked Radio |
| NRZ | Non-Return-to-Zero data levels |
| $f_{CO}$ | Filter cut-off frequency |
| $f_{CTCSS\ IN}$ | Sub-Audio Rx frequency |
| $f_{CTCSS\ OUT}$ | Sub-Audio Tx frequency |
| $f_{TONE}$ | Tone frequency |
| $f_{XTAL}$ | Xtal/clock frequency |
| $R_{NRZ\ Rx}$ | NRZ Rx baud rate |
| $R_{NRZ\ Tx}$ | NRZ Tx baud rate |
| $S_{INPUT}$ | Audio input signal |

## "Read Status Register" – A/C $71_H$ ($79_H$), followed by 1 byte of Reply Data.

The Status Register indicates the operational condition of the FX805. Bits 0 to 5 are set individually to indicate specific actions within the device. When a Status Bit is set to a logic "1," an Interrupt Request (IRQ) output is generated. A read of the Status Register will reset the interrupt condition and ascertain the state of this register.

Table 4 (below) shows the conditions indicated by the Status Bits.

| Status Bit | Set By | Logic | Cleared By | Logic |
|---|---|---|---|---|
| *MSB 7, 6* | *Received First* Not used | "0" | Not used | "0" |
| *5* | NRZ data transmission complete. No new data loaded. | "1" | 1. Write to NRZ Tx Data Reg. or, 2. General Reset or, 3. NRZ Encoder Powersave. | "0" |
| *4* | NRZ Tx Data Buffer ready for next data byte. | "1" | 1. Write to NRZ Tx Data Reg. or, 2. General Reset or, 3. NRZ Tx Powersave. | "0" |
| *3* | New NRZ Rx data received **before** last byte was read. | "1" | 1. Read NRZ Rx Data Reg. or, 2. General Reset or, 3. NRZ Decoder Powersave. | "0" |
| *2* | 1 byte of NRZ Rx data received. | "1" | 1. Read NRZ Rx Data Reg. or, 2. General Reset or, 3. NRZ Decoder Powersave. | "0" |
| *1* | NOTONE Timer period expired. | "1" | 1. Read Status Register or, 2. General Reset or, 3. CTCSS Decoder Powersave. | "0" |
| *0* | Rx Tone Measurement complete. | "1" | 1. Read Status Register or, 2. General Reset or, 3. CTCSS Decoder Powersave. | "0" |

*Table 4 Status Register*

## "Read CTCSS Rx Frequency Register" – A/C $72_H$($7A_H$), followed by 2 bytes of Reply Data.

### Measurement of CTCSS Rx Frequency ($f_{CTCSS\ IN}$)

The input sub-audio signal ($f_{CTCSS\ IN}$), is filtered and measured in the Frequency Counter over the "measurement period" (122.64ms).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the measurement period of a successful decode is complete, the Rx Tone Measurement bit in the Status Register, and the Interrupt bit are set.

The CTCSS Rx Frequency Register will now indicate the sub-audio signal frequency ($f_{CTCSS\ IN}$) in the form of 2 data bytes (1 and 0) as illustrated in Figure 6.

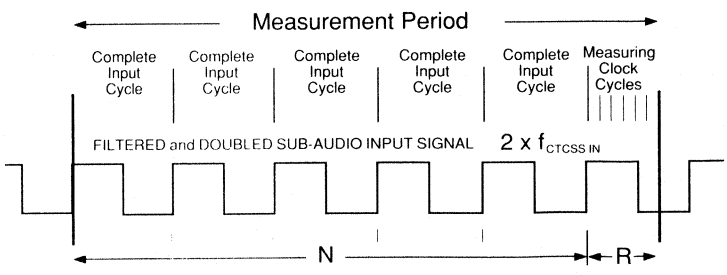



*Fig.5 Measurement of a CTCSS Rx Frequency*

### "Read CTCSS Rx Frequency Register" .....

**The Integer (N)** – Byte 1

A binary number representing 'twice the number of complete input sub-audio cycle periods' counted during the measurement period of 122.64ms

**The Remainder (R)** – Byte 0

A binary number representing the remainder part, R, of 2 x Sub-Audio Input Frequency. 'R = number of specified measuring-clock cycles' required to complete the specified measurement period (See N). The clock-cycle frequency is 4166.6Hz

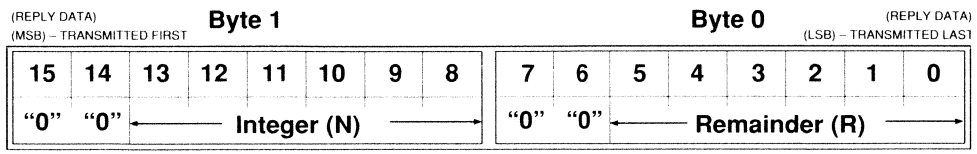



*Fig. 6 Format of the CTCSS Rx Frequency Register*

### CTCSS Rx Frequency Register

Figure 6 (above) shows the format of the CTCSS Rx Frequency Register.

Bits 8 (LSB) to 13 (MSB) are used to represent the Integer (N). From Byte 1, valid values of $N = 16 \leq N \leq 61$.

ie. values of N less than 16 and greater than 61 are not within the specified frequency band.

Bits 0 (LSB) to 5 (MSB) (Byte 0) are used to represent the Remainder (R). From Byte 0, valid values of $R = \leq 31$.

This register is not affected by the General Reset command ($01_H$) and may adopt any random configuration at Power-Up.

---

### CTCSS Rx Frequency Measurement Formulæ

To assist in the production of 'look-up' tables and limit-values in the µController and provide guidance upon the determination of N and R from a measured CTCSS frequency, the following formulæ show the derivation of the CTCSS Rx Frequency ($f_{CTCSS\ IN}$) from the measured data bytes (N and R).

**$f_{CTCSS\ IN}$**

In the measurement period of 122.64ms there are N cycles at 2 x $f_{CTCSS\ IN}$ and R clock-cycles at 4166.6Hz, for any input frequency.

So

$$f_{CTCSS\ IN} = \frac{N \times f_{XTAL}}{1920 \times (511 - R)} \text{ Hz} \quad [1]$$

$$N = \text{INT}\left[\frac{(1920 \times 511 \times f_{CTCSS\ IN})}{f_{XTAL}}\right] \quad [2]$$

$$R = \text{INT}\left[511 - \left[\frac{N \times f_{XTAL}}{1920 \times f_{CT\ CSS\ IN}}\right] + 0.5\right] \quad [3]$$

**Calculate N first**

**Examples** ($f_{XTAL}$ = 4.00MHz): $f_{CTCSS\ IN}$ = 100Hz N = 24 R = 11; $f_{CTCSS\ IN}$ = 250Hz N = 61 R = 3

---

## NOTONE Timing

The input sub-audio signal is monitored by the Frequency Assessment circuitry. Before any NOTONE action is enabled, the FX805 must have achieved at least one successful "Tone Measurement Complete" action.

If there is no signal or the signal is of a consistently poor quality, the NOTONE Timer will start to charge via the timing components. When the timing period has expired (at $V_{DD}/2$), an Interrupt and a Status bit (NOTONE Timer Expired) are generated. This is a one-shot function and is reset by a "Tone Measurement Complete" interrupt.

## "Write to CTCSS Tx Frequency/NRZ Baud Rate Register" – A/C $73_H$ ($7B_H$), followed by 2 bytes of Command Data.

The information loaded to this register will set either the:

(a) CTCSS Tx Tone Frequency $f_{CTCSS\ OUT}$
(b) NRZ Tx Baud Rate $R_{NRZ\ Tx}$
(c) NRZ Rx Baud Rate $R_{NRZ\ Rx}$

The chosen mode for this register (a, b or c) is determined by the FX805 operational mode enabled by the Control Register (Table 3), as shown in the table below.

| Control Register Bits 7 | 6 | 5 | FX805 Mode Enabled | CTCSS Tx/NRZ Baud Rate Register Function |
|---|---|---|---|---|
| 0 | 0 | 0 | CTCSS Decode | |
| 0 | 0 | 1 | NRZ Decode | NRZ Rx Baud Rate |
| 0 | 1 | 0 | CTCSS Encode | CTCSS Tx Frequency |
| 0 | 1 | 1 | NRZ Encode | NRZ Tx Baud Rate |
| 1 | 0 | 0 | CTCSS Encode and Decode | CTCSS Tx Frequency |
| 1 | 0 | 1 | NRZ Encode and CTCSS Decode | NRZ Tx Baud Rate |
| 1 | 1 | 0 | NRZ and CTCSS Decode | NRZ Rx Baud Rate |
| 1 | 1 | 1 | NRZ Decode | NRZ Rx Baud Rate |

*Table 5 CTCSS Frequency/NRZ Baud Rate Register Configurations*

### Data Format

Data is transmitted, via "C-BUS," to this register as 2 bytes of Command Data (1 and 2) distributed as command words P and Q, in the form illustrated in Figure 7. This register is not affected by the General Reset command ($01_H$) and may adopt any random configuration at Power-Up.

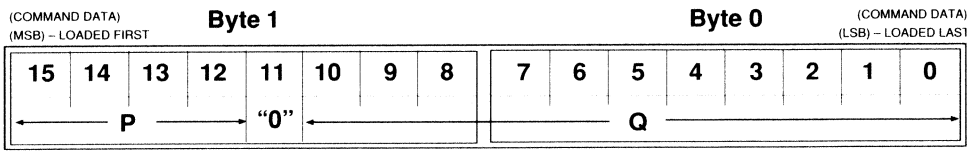



*Fig.7 Format of the CTCSS Tx Frequency/NRZ Baud Rate Register*

### Command Words P and Q

With reference to Figure 7, the two data words, P and Q, loaded to this register are interpreted as:

**P** = a binary number to set the Tx Sub-Audio Lowpass Filter bandwidth (applicable to NRZ Encode and CTCSS Encode modes).

**Q** = a binary number to set the frequency or baud rate of the selected function (see Table 5).

### Command Word 'P'

| Bits 15 | 14 | 13 | LSB 12 | 'P' | LPF Bandwidth |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 2 | 300Hz |
| 0 | 0 | 1 | 1 | 3 | 200Hz |
| 0 | 1 | 0 | 0 | 4 | 150Hz |
| 0 | 1 | 0 | 1 | 5 | 120Hz |
| 0 | 1 | 1 | 0 | 6 | 100Hz |
| 0 | 1 | 1 | 1 | 7 | 85.7Hz |
| 1 | 0 | 0 | 0 | 8 | 75Hz |

*Table 6 Valid Values of 'P'*

Bits 12 to 15 are used to produce the data word '**P**' as shown in Table 6 (left). The cut-off frequency $f_{CO}$ (0.5dB point) of the Tx Sub-Audio Lowpass Filter is calculated as:

$$f_{CO} = \frac{f_{XTAL}}{32 \times 208.33 \times \text{'P'}}$$

$$\text{so 'P'} = \frac{f_{XTAL}}{32 \times 208.33 \times f_{CO}}$$

Table 6 is given as an example and calculated using a Xtal/clock ($f_{XTAL}$) frequency of 4.00MHz. As illustrated, only values of '**P**' of *2 to 8* are usable.

**"Write to CTCSS Tx Frequency/NRZ Baud Rate Register" .....**

### Command Word 'Q'

With reference to Figure 7, Bits 0 to 10 are used to produce the data word '**Q**' which sets one of the parameters described below. As can be seen, command word '**Q**' could be used to produce a word whose value would produce a parameter outside that specified (Pages 16 and 17), care should be taken not to do this. Examples for limits of '**Q**' in each operational configuration are included. '**Q**' = 0 is not valid in the following calculations. Bit 11 is not used and must be set to logic "0"

**(a) CTCSS Tx Tone Frequency ($f_{CTCSS\ OUT}$)**

$$f_{CTCSS\ OUT} = \frac{f_{XTAL}}{32 \times \text{'Q'}} \text{ Hz}$$

$$\text{so 'Q'} = \frac{f_{XTAL}}{32 \times f_{CTCSS\ OUT}} \text{ Hz}$$

**Example Limits**

| | | | |
|---|---|---|---|
| $f_{CTCSS\ OUT}$ | = | 67Hz | |
| so '**Q**' | = | 1866 | "11101001010" |
| $f_{CTCSS\ OUT}$ | = | 250Hz | |
| so '**Q**' | = | 500 | "00111110100" |

**(b) NRZ Tx Baud Rate ($R_{NRZ\ Tx}$)**

$$R_{NRZ\ Tx} = \frac{f_{XTAL}}{32 \times \text{'Q'}} \text{ bits/sec}$$

$$\text{so 'Q'} = \frac{f_{XTAL}}{32 \times R_{NRZ\ Tx}}$$

| | | | |
|---|---|---|---|
| $R_{NRZ\ Tx}$ | = | 67 bits/sec | |
| so '**Q**' | = | 1866 | "11101001010" |
| $R_{NRZ\ Tx}$ | = | 300 bits/sec | |
| so '**Q**' | = | 417 | "00110100001" |

**(c) NRZ Rx Baud Rate ($R_{NRZ\ Rx}$)**

$$R_{NRZ\ Rx} = \frac{f_{XTAL}}{32 \times 11 \times \text{'Q'}} \text{ bits/sec}$$

$$\text{so 'Q'} = \frac{f_{XTAL}}{352 \times R_{NRZ\ Rx}}$$

| | | | |
|---|---|---|---|
| $R_{NRZ\ Rx}$ | = | 100 bits/sec | |
| so '**Q**' | = | 114 | "00001110010" |
| $R_{NRZ\ Rx}$ | = | 300 bits/sec | |
| so '**Q**' | = | 38 | "00000100110" |

## "Read NRZ Rx Data Register" – A/C $74_H$ ($7C_H$), followed by 1 byte of Reply Data.

Received NRZ data bits are organized into bytes and made available to the µController via the Reply Data line. As 8 bits are received into this register an interrupt is generated to indicate that a complete byte has been received, this byte must be read before the arrival of the last (8th) bit of the next incoming byte, if this is not done, an interrupt to indicate this condition will be generated and the previous Rx data is discarded (See Table 4, Status Register, Bits 2 and 3).

Word synchronization is not provided. Byte synchronization and any codeword recognition will be performed by the host µController. The Rx baud rate is set by writing to the CTCSS Tx Frequency/NRZ Baud Rate Register ($73_H$/$7B_H$). The first bit received is the first bit sent to the µController.

This register is not affected by the General Reset command ($01_H$) and may adopt any random configuration at Power-Up.

## "Write to NRZ Tx Data Register" – A/C $75_H$ ($7D_H$), followed by 1 byte of Command Data.

A byte for transmission is loaded from the "C-BUS" Command Data line with this A/C. The first data-bit received via the "C-BUS" is transmitted first. This transmitter operation is **non-inverting**.

The first data-byte loaded after the NRZ Encoder is enabled (Control Register) initiates the transmission sequence and an interrupt will be generated when the NRZ Tx Data Buffer is ready for the next data-byte. Subsequently, interrupts occur for every 8 bits transmitted.

Transmission is terminated, the Tx Sub-Audio Output placed at $V_{BIAS}$, and an interrupt generated if the next byte is not loaded within 7 bit periods. (See Table 4, Status Register, Bits 4 and 5).

This register is not affected by the General Reset command ($01_H$) and may adopt any random configuration at Power-Up.

## "Write to Gain-Set Register" – A/C $76_H$ ($7E_H$), followed by 1 byte of Command Data.

| Setting | | | | Gain Setting | |
|---|---|---|---|---|---|
| ***MSB*** | | | | | |
| ***7*** | ***6*** | ***5*** | ***4*** | ***Transmitted Bit 7 First*** | |
| 0 | 0 | 0 | 0 | These 4 Bits Must be "0" | |
| | | ***3*** | | **Pre-Emphasis Setting** | |
| | | 1 | | 1.72dB Gain Enabled | |
| | | 0 | | 1.72dB Gain Disabled | |
| ***2*** | | ***1*** | ***0*** | **Tx Level Adjust Gain Setting** | |
| 0 | | 0 | 0 | -2.58 | dB |
| 0 | | 0 | 1 | -1.72 | dB |
| 0 | | 1 | 0 | -0.86 | dB |
| 0 | | 1 | 1 | 0 | dB |
| 1 | | 0 | 0 | +0.86 | dB |
| 1 | | 0 | 1 | +1.72 | dB |
| 1 | | 1 | 0 | +2.58 | dB |
| 1 | | 1 | 1 | Not Used | |

*Table 7 Gain-Set Register Settings*

### The Gain-Set Register Settings

The settings of this register control the CTCSS and NRZ signal level that is presented at the Tx Sub-Audio Output.

Bit 3, when enabled, is used to produce a pre-emphasis effect on the NRZ Tx Data by increasing the gain of the data bit **before** a level change (Figure 8 below), by 1.72dB to make that data pulse level slightly more positive (or negative). The signal level will be 1.72dB greater than that set by Bits 0 to 2. If the Tx Sub-Audio Output level is set to +2.58dB, the pre-emphasized level will be +4.3dB.

The pre-emphasis function, will remain enabled until disabled by setting Bit 3 to a logic "0." If this function remains enabled when using the CTCSS Encoder the output signal level may be adversely affected, therefore this function should only be enabled when in the NRZ Encode mode.

This register is not affected by the General Reset command ($01_H$) and may adopt any random configuration at Power-Up.

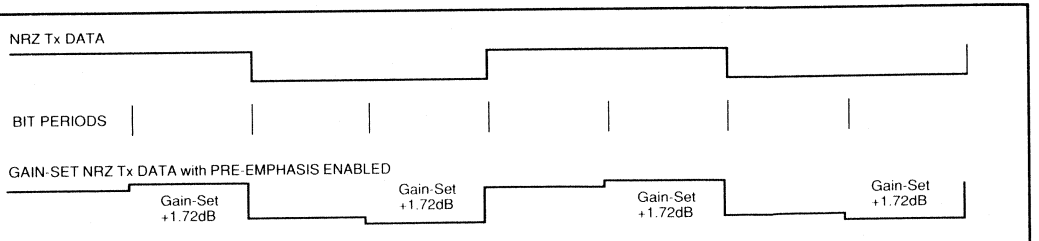



*Fig.8 Gain-Set with Pre-Emphasis*

# Timing Information

## Timing Diagrams

Figure 9 shows the timing parameters for two-way communication between the µController and the FX805 on the "C-BUS." Figure 10 shows, in detail, the timing relationships for "C-BUS" information transfer.

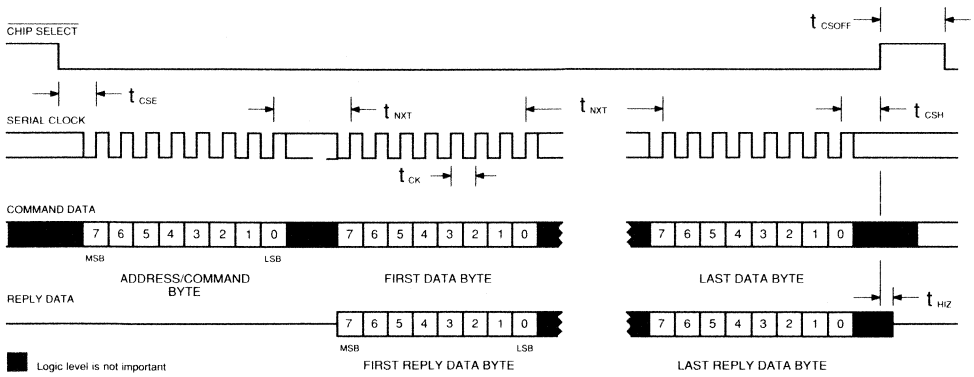



*Fig.9 "C-BUS" Timing Information* NOT TO SCALE

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $t_{CSE}$ | 2.0 | – | – | µs |
| $t_{CSH}$ | 4.0 | – | – | µs |
| $t_{CSOFF}$ | 2.0 | – | – | µs |
| $t_{NXT}$ | 4.0 | – | – | µs |
| $t_{CK}$ | 2.0 | – | – | µs |
| $t_{CH}$ | 500 | – | – | ns |
| $t_{CL}$ | 500 | – | – | ns |
| $t_{CDS}$ | 250 | – | – | ns |
| $t_{CDH}$ | 0 | – | – | ns |
| $t_{RDS}$ | 250 | – | – | ns |
| $t_{RDH}$ | 50.0 | – | – | ns |
| $t_{HIZ}$ | – | – | 2.0 | µs |

### Notes

(1) Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last.
Reply Data is read from the FX805 MSB (bit 7) first, LSB (bit 0) last.
(2) Data is clocked into the FX805 and into the µController on the rising Serial Clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX805 will work with either polarity Serial Clock pulses.

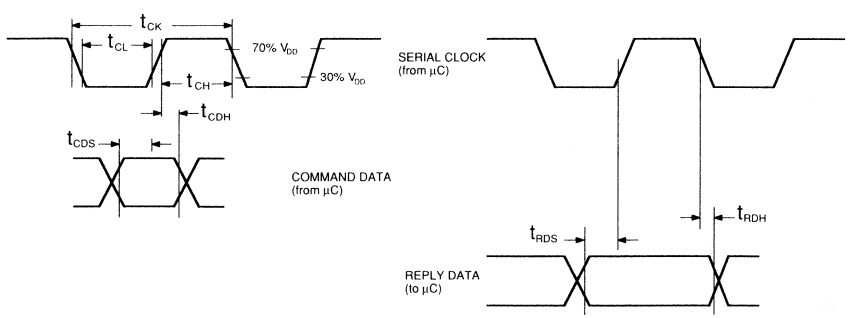



*Fig.10 "C-BUS" Timing Relationships* NOT TO SCALE

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX805J** | -40°C to +85°C (cerdip) |
| | **FX805LG/LS** | -40°C to +85°C (plastic) |
| Storage temperature range: | **FX805J** | -55°C to +125°C (cerdip) |
| | **FX805LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_{XTAL}$ = 4.0MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz.
Composite Signal = 308mVrms @ 1kHz + 75mVrms Noise + 31mVrms Sub-Audio Signal.
Noise Bandwidth = 5kHz Band Limited Gaussian.

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Values** | | | | | | |
| Supply Voltage | | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | (All Functions Enabled) | | – | 5.0 | – | mA |
| | (Decoders Only Enabled) | | – | 1.9 | – | mA |
| | (Powersave All) | | – | 0.9 | – | mA |
| **Analogue Impedances** | | | | | | |
| Rx Sub-Audio Input | | | 350 | – | – | kΩ |
| Audio Input | | | 350 | – | – | kΩ |
| Audio By-Pass Switch 'On' | | 5 | – | 2.0 | – | kΩ |
| Audio By-Pass Switch 'Off' | | 5 | 1.0 | 10.0 | – | MΩ |
| Rx Amp Input (+ and -) | | | 1.0 | 10.0 | – | MΩ |
| Comparator Input (+ and -) | | | 1. 0 | 10.0 | – | MΩ |
| Rx Sub-Audio Output | | | – | 2.0 | – | kΩ |
| Tx Sub-Audio Output | (Encoder Enabled) | 5 | – | 2.0 | – | kΩ |
| | (Encoder Disabled) | 5 | – | 500 | – | kΩ |
| Audio Output | (Enabled) | 5 | – | 2.0 | – | kΩ |
| | (Disabled) | 5 | – | 500 | – | kΩ |
| Rx Amp and Comparator Outputs | | | | | | |
| Large Signal | | | – | 6.0 | – | kΩ |
| Small Signal | | | – | 600 | – | Ω |
| **Dynamic Values** | | | | | | |
| **Digital Interface** | | | | | | |
| Input Logic "1" | | 1 | 3.5 | – | – | V |
| Input Logic "0" | | 1 | – | – | 1.5 | V |
| Output Logic "1" | (IOH = -120µA) | 2 | 4.6 | – | – | V |
| Output Logic "0" | (IOL = 360µA) | 3 | – | – | 0.4 | V |
| $I_{OUT}$ Tristate (Logic "1" or "0") | | 3 | – | – | 4.0 | µA |
| Input Capacitance | | 1 | – | – | 7.5 | pF |
| Logic Input Current | ($V_{IN}$ = 0 to 5.0V) | 1 | – | – | 1.0 | µA |
| IOX | ($V_{OUT}$ = 5.0V) | 4 | – | – | 4.0 | µA |
| **Overall Performance** | | | | | | |
| **CTCSS – Decode** | | | | | | |
| Sensitivity | (Pure CTCSS Tone) | 6 | – | -26.0 | – | dB |
| Response Time | (Composite Signal) | | | | | |
| 100Hz to 257Hz Tone | | | – | – | 250 | ms |
| 65Hz Tone | | 9 | – | – | 375 | ms |
| Tone Measurement Resolution | | | – | 0.2 | – | % |
| Tone Measurement Accuracy | | | – | 0.5 | – | % |
| NOTONE Response Time | (Composite Signal) | 7 | – | – | 250 | ms |
| False Tone Interrupts | (Noise input only) | 10 | – | 20.0 | – | /Hr |

## Specification...

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **CTCSS – Encode** | | | | | |
| Frequency Range | | 65.0 | | 257 | Hz |
| Tone Frequency Resolution | | – | – | 0.2 | % |
| Tone Amplitude Tolerance | | -1.0 | – | +1.0 | dB |
| Rise Time (to 90%) | | – | – | 30.0 | ms |
| Fall Time (to 10%) | | – | – | 50.0 | ms |
| Total Harmonic Distortion | | – | – | 5.0 | % |
| **NRZ – Decode** | | | | | |
| Rx Bit-Rate Sync Time | | – | 2 | – | edges |
| Rx Bit Error Rate | 11 | – | $1 \times 10^{-3}$ | – | $P_{(error)}$ |
| **NRZ – Tx** | | | | | |
| Tx Bit Rate | | 67.0 | – | 300 | bits/s |
| Tx LPF (3dB) Bandwidth | | 75 | – | 300 | Hz |
| Sub-Audio Tx Output Level | | | | | |
| CTCSS | | – | 0 | – | dB |
| NRZ | | – | 0.871 | – | V p-p |
| Amplitude Adjustment Range | | -2.58 | | 2.58 | dB |
| Adjustment Step Size (7 steps) | 8 | – | 0.86 | – | dB |
| **Sub-Audio Bandstop Filter** | | | | | |
| Passband | | 297 | | 3000 | Hz |
| Passband Gain | | – | 0 | – | dB |
| Passband Gain (w.r.t. gain at 1.0kHz) | | -1.5 | – | +0.5 | dB |
| Stopband Attenuation | | | | | |
| at 250 Hz | | – | 36.0 | – | dB |
| at 150 Hz | | – | 24.0 | – | dB |
| at 100 Hz | | – | 18.0 | – | dB |
| Residual Hum and Noise | | – | -50.0 | -46.0 | dBp |
| Alias Frequency | | – | – | 62.5 | kHz |
| **Xtal/Clock Frequency** ($f_{XTAL}$) | | 3.9 | – | 4.1 | MHz |

**Notes**

1. Device control pins; Serial Clock, Command Data, Wake and CS.
2. Reply Data output.
3. Reply Data and IRQ outputs.
4. Leakage current into the "Off" IRQ output.
5. See Control Register.
6. With Input gain components set as recommended in Figure 2.
7. Probability 0.97
8. See Gain-Set Register, Table 7 - Bits 0, 1, 2 and 3.
9. For $f_{CTCSS\ IN}$ of 65Hz to 100Hz, Response Time $t_R = (100/f_{TONE}) \times 250$ ms.
10. Distributed across the Rx frequency band.
11. With 10dB signal-to-noise ratio in a bit-rate bandwidth.

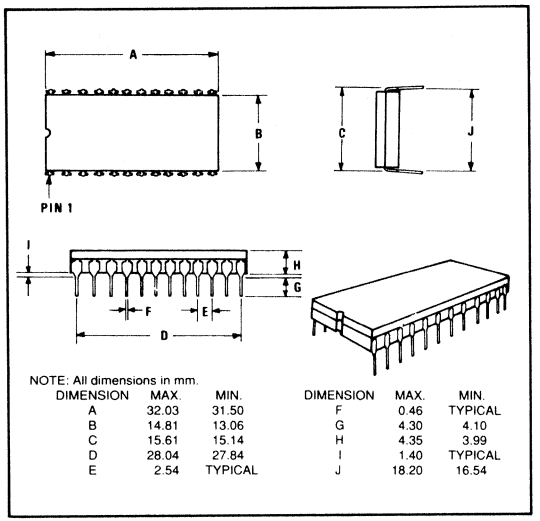
## Package Outline

The FX805J, the dual-in-line package, is shown in Figure 11. The 'LG' version is shown in Figure 12 and the 'LS' version in Figure 13.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX805 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

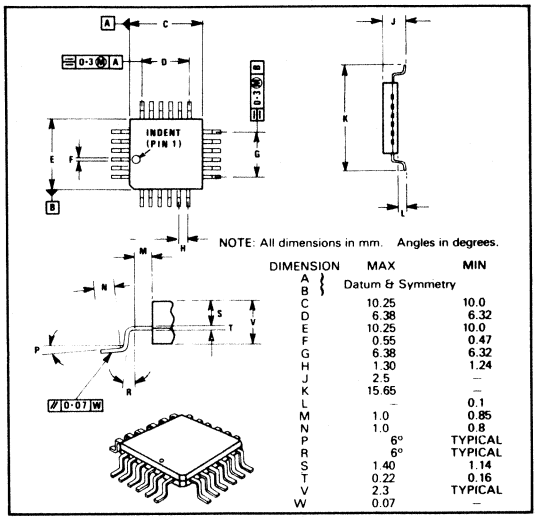
*Fig. 11* **FX805J** *24-pin DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. | DIMENSION | MAX. | MIN. |
|---|---|---|---|---|---|
| A | 32.03 | 31.50 | F | 0.46 | TYPICAL |
| B | 14.81 | 13.06 | G | 4.30 | 4.10 |
| C | 15.61 | 15.14 | H | 4.35 | 3.99 |
| D | 28.04 | 27.84 | I | 1.40 | TYPICAL |
| E | 2.54 | TYPICAL | J | 18.20 | 16.54 |

*Fig. 12* **FX805LG** *24-pin Package*



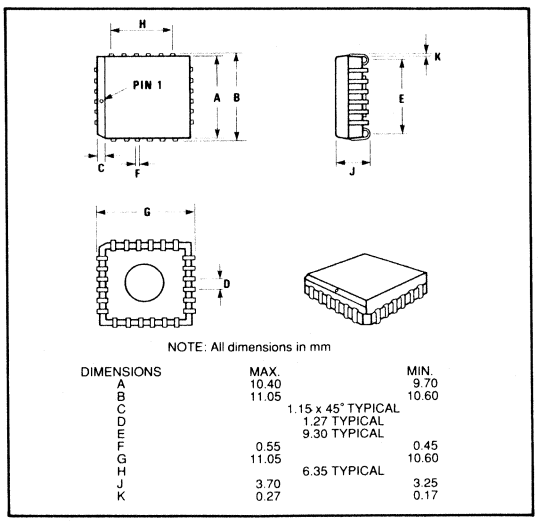

NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B, C | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

## Ordering Information

| | |
|---|---|
| **FX805J** | 24-pin cerdip DIL |
| **FX805LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX805LS** | 24-lead plastic leaded chip carrier |

*Fig. 13* **FX805LS** *24-lead Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

# FX806A
# AUDIO PROCESSOR

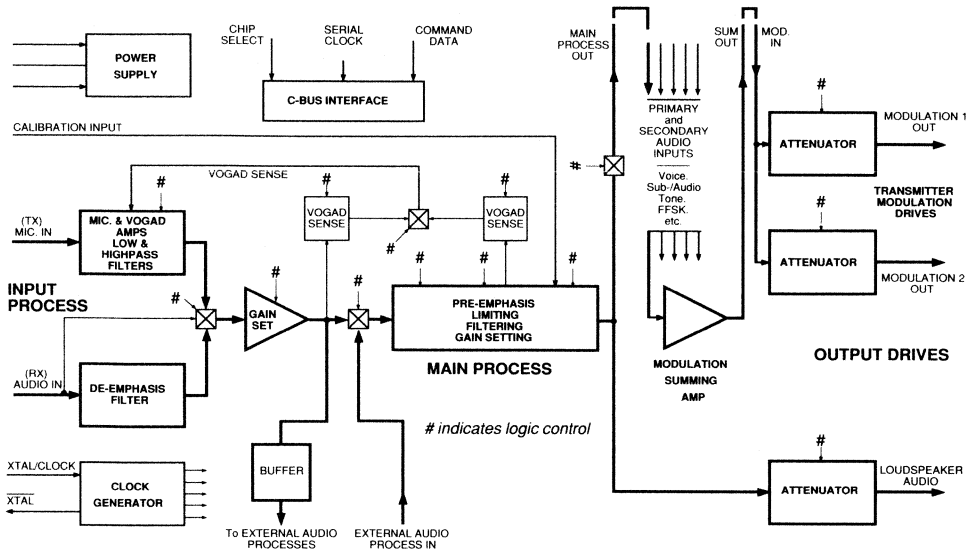



*Fig.1 FX806A Audio Processor*

## Brief Description

Intended primarily to operate as the "Audio Terminal" of Radio Systems using the DBS 800 Digitally-integrated Baseband System, the FX806A is a PMR Audio Processor which meets EIA and CEPT audio specifications.
Using a unique filter line-up, the FX806A offers lower distortion versus modulation level figures than conventional filter/limiter configurations.

The FX806A is a half-duplex device whose signal paths and level-setting elements are dynamically configured and adjusted by digital information sent from the Radio µController using "C-BUS" hardware and software protocol.

Figure 5 shows a complete functional block diagram of the FX806A signal paths which can be viewed as 3 sections:

- **Input Process**

Selectable transmit or receive input paths.

The transmit path with low-noise input and VOGAD amplifiers and bandpass filtered stages provides good signal-to-noise performance at low input levels and minimum distortion for high-drive modulation signals.

De-emphasis is software selectable at the Rx Audio Input for FM or PM radio configurations.

This initial audio, after in-line gain adjustment, is available for switching to either external audio processes (such as scrambling) or internally to the Main Process stages.

- **Main Process**

Conditioning for Input or External Process signals with gain/pre-emphasis, high and lowpass switched capacitor filters and a transmitter deviation limiter. The Main Process Output may be switched to $V_{BIAS}$.

- **Summation and Output Drives**

Main "voice audio" from the Main Process is combined with signalling and data from other DBS 800 facilities, to provide the composite (in and outband) signal for the digitally adjustable Transmitter Modulation Drives.
Received audio is level (volume) adjusted for output to loudspeaker circuitry.

Signal-level stability and therefore output accuracy, of the FX806A is maintained by a voltage-controlled gain system (VOGAD) with specific gain sensors that are selected automatically by the Internal/External Mode Command. The VOGAD system permits high deviation with low distortion. This is achieved by reducing the path gain (and so reducing the distortion introduced by the Peak Deviation limiter) when the input signal is large.

Signal levels can be controlled to provide 'dynamic-compensation' for such factors as temperature drift, VCO non-linearity, etc.

FX806A audio output stages can be completely disabled or the whole microcircuit placed into a "Powersave" mode, leaving only clock and "C-BUS" circuitry active.

The FX806A is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.

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Provisional Issue

## Pin Number Function

| FX806A J/LG/LS | |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal circuit is employed. See Figure 2, INSET 2. |
| 2 | **Xtal/clock**: The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, INSET 2. This clock provides timing for on-chip elements, filters etc. |
| 3 | **Serial Clock:** The "C-BUS," serial data loading clock input. This clock, produced by the µController, is used for transfer timing of Command Data to the Audio Processor. See Timing diagrams and System Support Document. |
| 4 | **Command Data:** The "C-BUS," serial data input from the µController. Command Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. The Command/Data instruction is acted upon at the end of loading the whole instruction. Command information is detailed in Tables 1, 2, 3, 4 and 5. See Timing diagrams and System Support Document. |
| 5 | **$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** The "C-BUS," data loading control function. This input is provided by the µController. Command Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing diagrams and System Support Document. |
| 6 | **VOGAD Out:** The output of the relevant VOGAD sensor. This output, with external attack and decay setting components, should be connected as in Figures 2 and 3, to the VOGAD In pin. |
| 7 | **Rx Audio In:** The audio input to the FX806A from the radio receiver's demodulator circuits. This input, which requires to be a.c. coupled with capacitor $C_{12}$, is selected by a Control Command bit. |
| 8 | **VOGAD In:** The gain control signal from the selected VOGAD sensor (VOGAD Out) to the "Input Process" Voltage Controlled Amplifier. VOGAD operation is enabled via a Mode Command (Bit5). Individual sensors, automatically selected, permit gain control from either the Input Process or an external process. External attack and decay setting components should be applied as recommended in Figures 2 and 3. |
| 9 | **$V_{BIAS}$:** The output of the on-chip analogue circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ by a capacitor $C_{10}$, See Figure 2. |
| 10 | **Mic In (+):** The non-inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2, INSET 1. |
| 11 | **Mic In (–):** The inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2, INSET 1. |
| 12 | **$V_{SS}$:** Negative supply rail (GND). |

## Pin Number Function

| FX806A J/LG/LS | |
|---|---|
| 13 | **Mic Out:** The output of the microphone Op-Amp, used with the Mic In (–) input to provide the required gain/attenuation using external components as shown in Figure 2. The external components shown are to assist in the use of this amplifier with either inverting or non-inverting inputs. During Powersave (Volume Command) this output is placed at $V_{SS}$. |
| 14 | **Processed Audio In:** The input to the device from such external audio processes as Voice Store and Retrieve or Frequency Domain Scrambling. This input, which requires to be a.c. coupled with a capacitor, $C_{13}$, is selected by a Mode Command bit. |
| 15 | **External Audio Process:** The buffered output of the Input Processing stage. For further external audio processing prior to re-introduction at the Processed Audio In pin. |
| 16 | **CALibration Input:** A unique input, intended to be used for dynamic balancing of the modulator drives and for measuring Deviation Limiter levels. A CUE (beep) input from the FX803 Audio Tone Processor can be entered on this line. This input is selected via a Mode Command bit ($11_H$) and is self-biased. |
| 17 | **Main Process Out:** The output of the Main Process stage. This output is summed with additional system inputs as required (Audio, Sub-Audio Signalling, FFSK – See System Overview) in the on-chip Modulation Summing Amplifier. External components as shown in Figure 2 should be used as required. |
| 18 | **Sum In:** The input and output terminals of the on-chip Modulation Summing Amplifier. External components are required for input signals, with gain/attenuation setting as shown in Figure 2. For single-signal, no-gain requirements, Main Process Out may be linked directly to Modulation In. |
| 19 | **Sum Out:** |
| 20 | **Modulation In:** The final, composite modulating signal to VCO (Mod 1) and Reference (Mod 2) Output Drives. |
| 21 | **Audio Output:** The processed audio signal output intended as a received audio (volume) output. Though normally used in the Rx mode, operation in Tx is permitted. The output level of this attenuator is controlled via a Volume Set command. During Powersave this output is placed at $V_{SS}$. |
| 22 | **Modulation 1 Drive:** The drive to the radio modulator Voltage Controlled Oscillator (VCO), from the composite audio summing stage. |
| 23 | **Modulation 2 Drive:** The drive to the radio modulator Reference Oscillator, from the composite audio summing stage.<br>**NOTE:** These VCO output attenuators are individually adjustable using the Modulator Levels command. During Powersave these outputs are placed at $V_{SS}$. |
| 24 | **$V_{DD}$:** Positive supply rail. A single, stable +5 volt supply is required. Levels and voltages within the Audio Processor are dependant upon this supply. |

# Analogue Application Information

## External Components

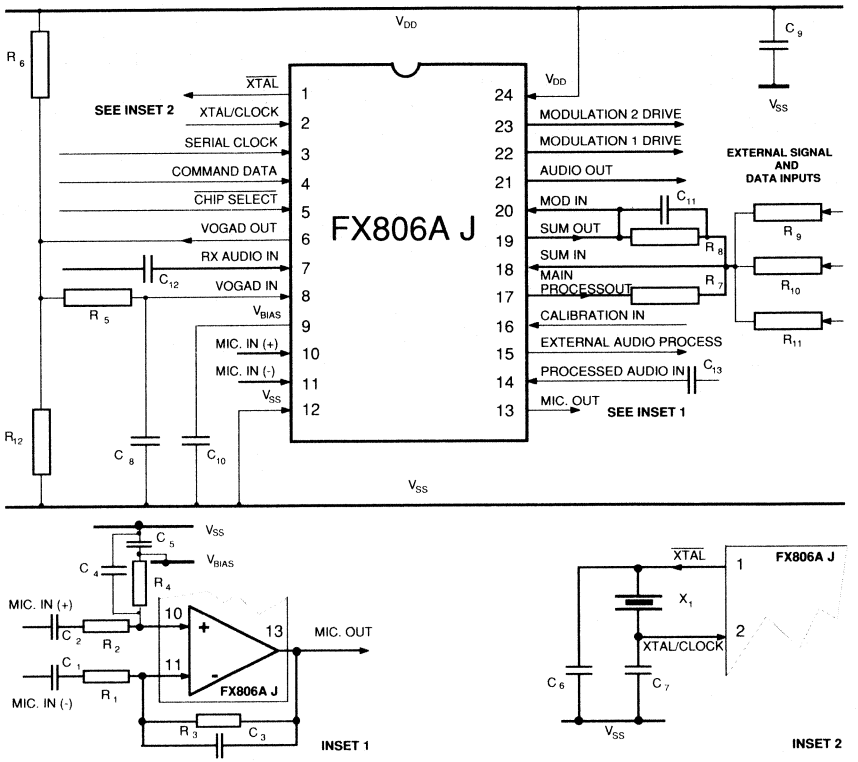



*Fig.2 Recommended External Components*

| Component | | Value | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $R_1$ | = | 10.0kΩ | $R_{10}$ | = | 100kΩ | $C_7$ | = | 5 – 65pF |
| $R_2$ | | 10.0kΩ | $R_{11}$ | | 100kΩ | $C_8$ | | 1.0µF |
| $R_3$ | | 20.0kΩ | $R_{12}$ | | 2.2MΩ | $C_9$ | | 1.0µF |
| $R_4$ | | 20.0kΩ | $C_1$ | | 470nF | $C_{10}$ | | 1.0µF |
| $R_5$ | | 10.0kΩ | $C_2$ | | 470nF | $C_{11}$ | | 22pF |
| $R_6$ | | 2.2MΩ | $C_3$ | | 270pF | $C_{12}$ | | 100nF |
| $R_7$ | | 100kΩ | $C_4$ | | 270pF | $C_{13}$ | | 10.0nF |
| $R_8$ | | 100kΩ | $C_5$ | | 0.1µF | $X_{13}$ | | 4.0MHz |
| $R_9$ | | 100kΩ | $C_6$ | | 33pF | Tolerance: R = ±10%. C = ± 20% | | |

### Notes

To demonstrate the versatility of the Mic. inputs, Input Op-Amp gain/attenuation components for a voltage gain of 6.0dB are shown (INSET 1) in a differential configuration. Components for a single (+ or -) input may be employed.

Resistor values $R_7$ to $R_{11}$ (summation components) are dependant upon application and configuration requirements.

Xtal circuit capacitors $C_6$ ($C_D$) and $C_7$ ($C_G$) shown (INSET 2) are recommended in accordance with *CML Application Note D/XT/1 April 1986*. Circuit drive and drain resistors are incorporated on-chip.

Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast reaction fuse).

---

**VOGAD Components Calculations** – Figures 2 and 3

Provided $R_5$ >>1.0kΩ and $R_6 = R_{12}$ >>$R_5$

Then:

**Attack Time ($T_A$)** = $R_5 \times C_8$

**Decay Time ($T_D$)** = $\frac{R_6 \times C_8}{2}$

# Analogue Application Information .....

## The Gain Control System

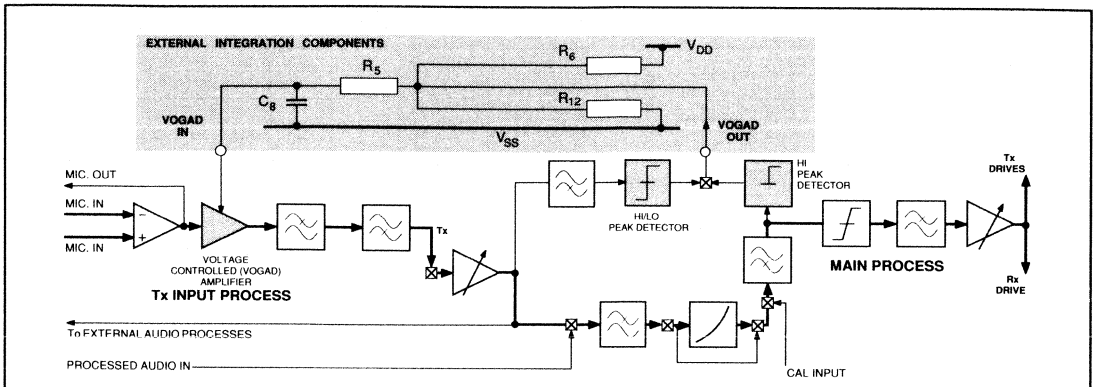



*Fig.3 "VOGAD" Sensors and Timing Components – (part of Fig.4)*

Tx gain control of the FX806A is by 1 of 2 selectable signal peak detectors whose output is fed via external integrating components to the Voltage Controlled Amplifier positioned in the Tx Input Process Path.

The integrated level to the VOGAD In pin causes the Voltage Controlled Amplifier gain to be reduced. VOGAD attack and decay calculations are described at the foot of the proceeding page.

The FX806A automatically chooses the appropriate peak detector when the signal path is set by a Mode Command. The Hi/Lo Peak Detector is employed when external audio processes are used.

The Hi Peak Detector is employed when external audio processes are not used.

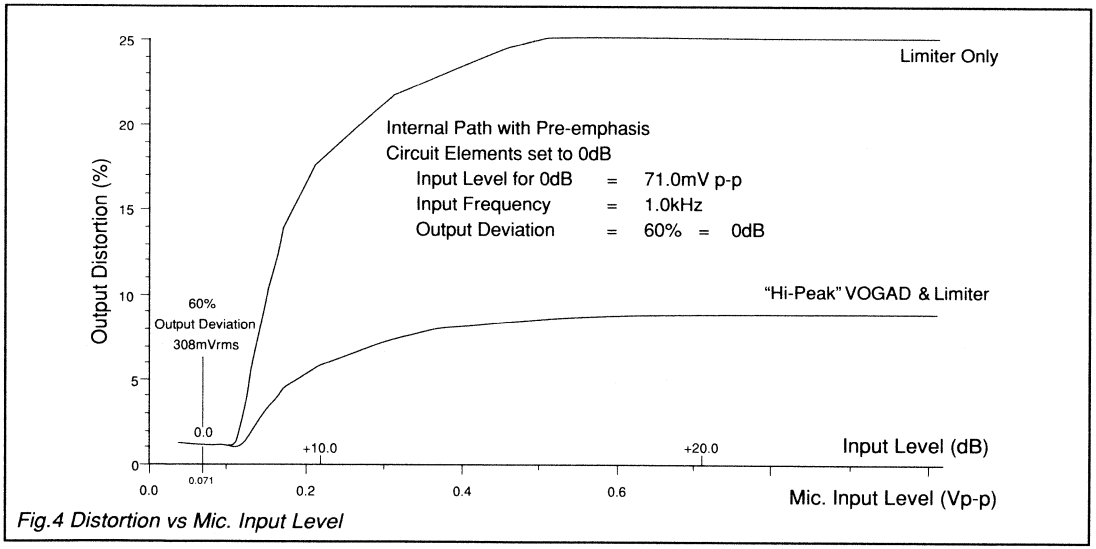



*Fig.4 Distortion vs Mic. Input Level*

### Suggested Calibration Methods

To effectively null all internal microcircuit tolerances, the following initial calibration routine is suggested:

**Tx Calibration :** *From Mic. In to Modulator Drives Out*

Disable Peak Detectors (Mode Command).
Set Transmitter Drives to 0dB (Mod Levels Set).
Pre-emphasis may be employed as required (Control Command).
Set Input Level Amp to 0dB (Control Command).

(1) Mic. In = 250mVrms at 1kHz; Set Process Gain Amp for output of 1440mV p - p (100% deviation).

(2) With Process Gain Amp set as (1); Mic In = 25mVrms at 1kHz, set Input Level Amp for output level of 308 mVrms (60% deviation).

**Rx Calibration:** *From Rx Audio In to Audio Output*

Set Audio Output Drive to 0dB (Volume Set).
Leave Process Gain Amp set as In (1) (above).

(3) With Rx Audio In level of between 154mVrms and 308mVrms (see Specification page), at 1kHz, set the Input Level Amp for an output level of 308mVrms.

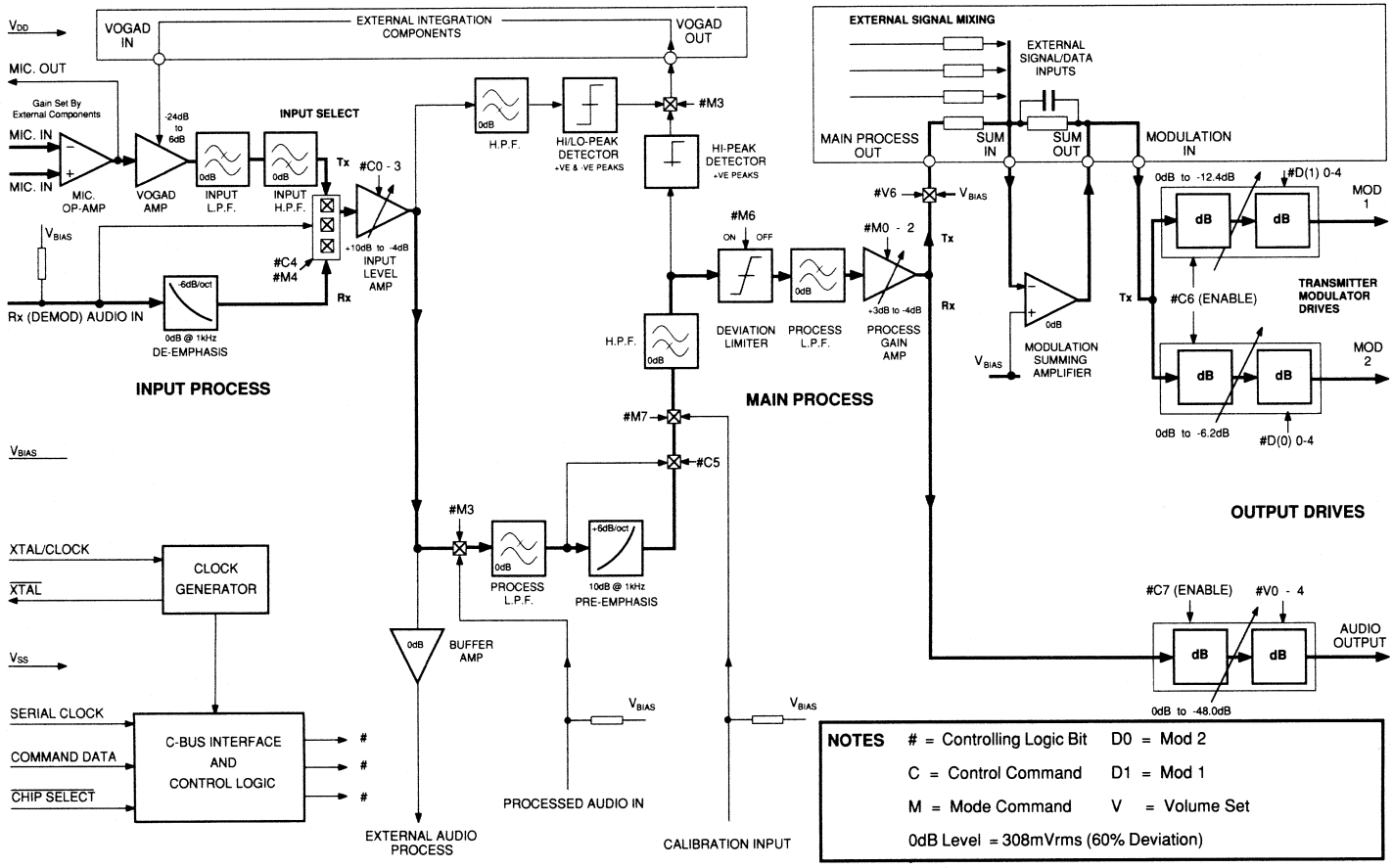



*Fig.5 PLMR Audio Processor – Facilities*

# Controlling Protocol

Control of the functions and levels within the FX806A PLMR Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the FX806A. The use of these instructions is detailed in the following paragraphs and tables.

| Command Assignment | Address/Command (A/C) Byte Hex | Binary MSB LSB | | Command Data | Table |
|---|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | | |
| Control Command | 10 | 0 0 0 1 0 0 0 0 | + | 1 byte | 2 |
| Mode Command | 11 | 0 0 0 1 0 0 0 1 | + | 1 byte | 3 |
| Mod. Levels Set | 12 | 0 0 0 1 0 0 1 0 | + | 2 bytes | 4 |
| Volume Set | 13 | 0 0 0 1 0 0 1 1 | + | 1 byte | 5 |

*Table 1 "C-Bus" Address/Commands*

In "C-BUS" protocol the FX806A is allocated Address/Command (A/C) values $10_H$ to $13_H$. "C-BUS" Command, Mode, Modulation and Volume assignments and data requirements are given in Table 1 and illustrated in Figure 5 (Main Block Diagram). Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after $\overline{\text{Chip Select}}$ (logic "0") as an Address/Command.

Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command ($01_H$) will be required. This command is provided to "reset" all devices on the "C-BUS" and has the following effect on the FX806A.

| | |
|---|---|
| Control Address Command | Loaded as $00_H$ |
| Mode Address Command | Loaded as $00_H$ |
| Volume Set | Loaded as $00_H$ |

## Control Command

*(Preceded by A/C $10_H$)*

| Setting | | | | Control Bits |
|---|---|---|---|---|
| ***MSB*** | | | | ***Transmitted First*** |
| ***Bit 7*** | | | | **Audio Output (Rx)** |
| 0 | | | | Disabled |
| 1 | | | | Enabled |
| ***6*** | | | | **Modulation Drives** |
| 0 | | | | Disabled |
| 1 | | | | Enabled |
| ***5*** | | | | **Pre-Emphasis** |
| 0 | | | | By-Pass |
| 1 | | | | Enabled |
| ***4*** | | | | **Input Select** |
| 0 | | | | Rx Audio In |
| 1 | | | | Mic. In |
| ***3*** | ***2*** | ***1*** | ***0*** | **Input Level Set** |
| 0 | 0 | 0 | 0 | Input Amp Disabled |
| 0 | 0 | 0 | 1 | -4.0dB |
| 0 | 0 | 1 | 0 | -3.0dB |
| 0 | 0 | 1 | 1 | -2.0dB |
| 0 | 1 | 0 | 0 | -1.0dB |
| 0 | 1 | 0 | 1 | 0dB |
| 0 | 1 | 1 | 0 | 1.0dB |
| 0 | 1 | 1 | 1 | 2.0dB |
| 1 | 0 | 0 | 0 | 3.0dB |
| 1 | 0 | 0 | 1 | 4.0dB |
| 1 | 0 | 1 | 0 | 5.0dB |
| 1 | 0 | 1 | 1 | 6.0dB |
| 1 | 1 | 0 | 0 | 7.0dB |
| 1 | 1 | 0 | 1 | 8.0dB |
| 1 | 1 | 1 | 0 | 9.0dB |
| 1 | 1 | 1 | 1 | 10.0dB |

*Table 2 Control Commands*

## Mode Command

*(Preceded by A/C $11_H$)*

| Setting | | | Mode Bits |
|---|---|---|---|
| ***MSB*** | | | ***Transmitted First*** |
| ***Bit 7*** | | | **Drive Source** |
| 0 | | | Signals |
| 1 | | | Calibration |
| ***6*** | | | **Deviation Limiter** |
| 0 | | | Disabled |
| 1 | | | Enabled |
| ***5*** | | | **VOGAD** |
| 0 | | | Disabled |
| 1 | | | Enabled |
| ***4*** | | | **De-Emphasis** |
| 0 | | | Enabled |
| 1 | | | By-Passed |
| ***3*** | | | **Signal Select** |
| 0 | | | Internal |
| 1 | | | External |
| ***2*** | ***1*** | ***0*** | **Process Gain Set** |
| 0 | 0 | 0 | -4.0dB |
| 0 | 0 | 1 | -3.0dB |
| 0 | 1 | 0 | -2.0dB |
| 0 | 1 | 1 | 1.0dB |
| 1 | 0 | 0 | 0dB |
| 1 | 0 | 1 | 1.0dB |
| 1 | 1 | 0 | 2.0dB |
| 1 | 1 | 1 | 3.0dB |

*Table 3 Mode Commands*

## Modulator Levels

*(Preceded by A/C12$_H$)*

| Setting | Modulator Drives |
|---|---|
| ***Byte 1*** | ***First byte for transmission*** |
| ***MSB*** ***7*** ***6*** ***5*** | |
| 0 0 0 | Must be "0" |
| ***4*** ***3*** ***2*** ***1*** ***0*** | **Mod. 1** Attenuation |
| 0 0 0 0 0 | 12.4dB |
| 0 0 0 0 1 | 12.0dB |
| 0 0 0 1 0 | 11.6dB |
| 0 0 0 1 1 | 11.2dB |
| 0 0 1 0 0 | 10.8dB |
| 0 0 1 0 1 | 10.4dB |
| 0 0 1 1 0 | 10.0dB |
| 0 0 1 1 1 | 9.6dB |
| 0 1 0 0 0 | 9.2dB |
| 0 1 0 0 1 | 8.8dB |
| 0 1 0 1 0 | 8.4dB |
| 0 1 0 1 1 | 8.0dB |
| 0 1 1 0 0 | 7.6dB |
| 0 1 1 0 1 | 7.2dB |
| 0 1 1 1 0 | 6.8dB |
| 0 1 1 1 1 | 6.4dB |
| 1 0 0 0 0 | 6.0dB |
| 1 0 0 0 1 | 5.6dB |
| 1 0 0 1 0 | 5.2dB |
| 1 0 0 1 1 | 4.8dB |
| 1 0 1 0 0 | 4.4dB |
| 1 0 1 0 1 | 4.0dB |
| 1 0 1 1 0 | 3.6dB |
| 1 0 1 1 1 | 3.2dB |
| 1 1 0 0 0 | 2.8dB |
| 1 1 0 0 1 | 2.4dB |
| 1 1 0 1 0 | 2.0dB |
| 1 1 0 1 1 | 1.6dB |
| 1 1 1 0 0 | 1.2dB |
| 1 1 1 0 1 | 0.8dB |
| 1 1 1 1 0 | 0.4dB |
| 1 1 1 1 1 | 0dB |
| ***Byte 0*** | ***Last byte for transmission*** |
| ***MSB*** ***7*** ***6*** ***5*** | |
| 0 0 0 | Must be "0" |
| ***4*** ***3*** ***2*** ***1*** ***0*** | **Mod. 2** Attenuation |
| 0 0 0 0 0 | 6.2dB |
| 0 0 0 0 1 | 6.0dB |
| 0 0 0 1 0 | 5.8dB |
| 0 0 0 1 1 | 5.6dB |
| 0 0 1 0 0 | 5.4dB |
| 0 0 1 0 1 | 5.2dB |
| 0 0 1 1 0 | 5.0dB |
| 0 0 1 1 1 | 4.8dB |
| 0 1 0 0 0 | 4.6dB |
| 0 1 0 0 1 | 4.4dB |
| 0 1 0 1 0 | 4.2dB |
| 0 1 0 1 1 | 4.0dB |
| 0 1 1 0 0 | 3.8dB |
| 0 1 1 0 1 | 3.6dB |
| 0 1 1 1 0 | 3.4dB |
| 0 1 1 1 1 | 3.2dB |
| 1 0 0 0 0 | 3.0dB |
| 1 0 0 0 1 | 2.8dB |
| 1 0 0 1 0 | 2.6dB |
| 1 0 0 1 1 | 2.4dB |
| 1 0 1 0 0 | 2.2dB |
| 1 0 1 0 1 | 2.0dB |
| 1 0 1 1 0 | 1.8dB |
| 1 0 1 1 1 | 1.6dB |
| 1 1 0 0 0 | 1.4dB |
| 1 1 0 0 1 | 1.2dB |
| 1 1 0 1 0 | 1.0dB |
| 1 1 0 1 1 | 0.8dB |
| 1 1 1 0 0 | 0.6dB |
| 1 1 1 0 1 | 0.4dB |
| 1 1 1 1 0 | 0.2dB |
| 1 1 1 1 1 | 0dB |

*Table 4 Modulator Drive Levels*

## Volume Set

*(Preceded by A/C13$_H$)*

| Setting | Volume Set |
|---|---|
| ***MSB*** ***7*** ***6*** | ***Transmitted First*** |
| 0 0 | **Main Process Out** |
| 0 1 | Enabled<br>Biased |
| ***5*** | **Powersave** |
| 0 | Chip Enabled |
| 1 | Powersaved |
| ***4*** ***3*** ***2*** ***1*** ***0*** | **Volume Set** Attenuation |
| 0 0 0 0 0 | Off |
| 0 0 0 0 1 | 48.0dB |
| 0 0 0 1 0 | 46.4dB |
| 0 0 0 1 1 | 44.8dB |
| 0 0 1 0 0 | 43.2dB |
| 0 0 1 0 1 | 41.6dB |
| 0 0 1 1 0 | 40.0dB |
| 0 0 1 1 1 | 38.4dB |
| 0 1 0 0 0 | 36.8dB |
| 0 1 0 0 1 | 35.2dB |
| 0 1 0 1 0 | 33.6dB |
| 0 1 0 1 1 | 32.0dB |
| 0 1 1 0 0 | 30.4dB |
| 0 1 1 0 1 | 28.8dB |
| 0 1 1 1 0 | 27.2dB |
| 0 1 1 1 1 | 25.6dB |
| 1 0 0 0 0 | 24.0dB |
| 1 0 0 0 1 | 22.4dB |
| 1 0 0 1 0 | 20.8dB |
| 1 0 0 1 1 | 19.2dB |
| 1 0 1 0 0 | 17.6dB |
| 1 0 1 0 1 | 16.0dB |
| 1 0 1 1 0 | 14.4dB |
| 1 0 1 1 1 | 12.8dB |
| 1 1 0 0 0 | 11.2dB |
| 1 1 0 0 1 | 9.6dB |
| 1 1 0 1 0 | 8.0dB |
| 1 1 0 1 1 | 6.4dB |
| 1 1 1 0 0 | 4.8dB |
| 1 1 1 0 1 | 3.2dB |
| 1 1 1 1 0 | 1.6dB |
| 1 1 1 1 1 | 0dB |

*Table 5 Volume Set*

**Command Loading** Address/Commands and data bytes must be loaded in accordance with the information given in Figure 6 (Timing ).

The **Powersave** function is instigated by bit 5 of the Volume Set Command (Table 5).

During Powersave, all internal elements except the Clock Generator and "C-BUS" Interface are off, with the Mic Op-Amp and Output Drive stage outputs connected to $V_{SS}$.

**Modulator Drives** are controlled separately, but the whole two-byte Modulator Drive command must be loaded for each required adjustment.

**$\overline{\text{Chip Select}}$** must be held at a logic "1" for the period "$t_{CSOFF}$" between transactions.

## Command Loading and Timing

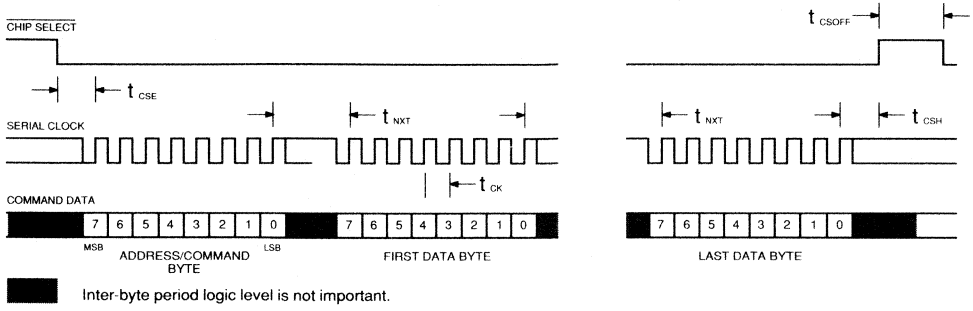



*Fig.6 "C-BUS" Timing Information*

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $t_{CSE}$ | 2.0 | – | – | µs |
| $t_{CSH}$ | 4.0 | – | – | µs |
| $t_{CSOFF}$ | 2.0 | – | – | µs |
| $t_{NXT}$ | 4.0 | – | – | µs |
| $t_{CK}$ | 2.0 | – | – | µs |

**Notes**

(1) Command Data is transmitted to the peripheral MSB (bit7) first, LSB (bit0) last.
(2) Data is clocked into the peripheral on the rising clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX806A will work with either polarity Serial Clock pulses.

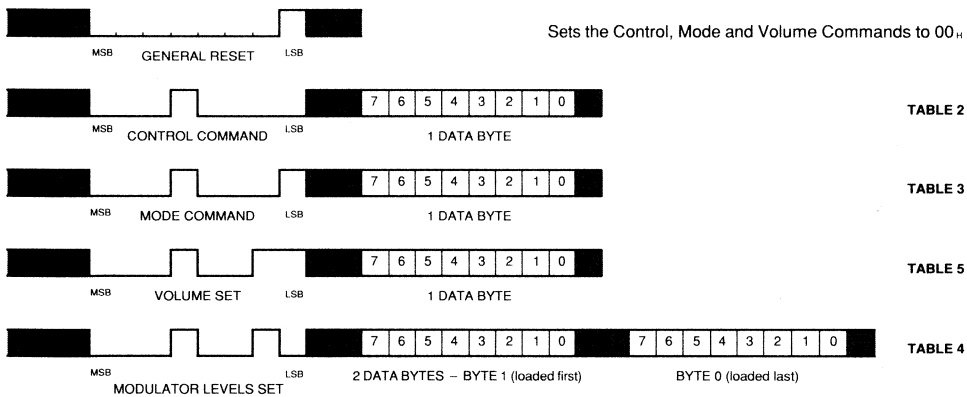



*Fig.7 Examples of "Command Data" Configurations*

To assist in rapid setting, the "quick-reference" guide below should be used together with Figure 5.

| | | | |
|---|---|---|---|
| **Control** | **A/C = $10_H$** | **Modulator Levels** | **A/C = $12_H$** |
| Bit 7 | Audio Out (Rx) Enable | Byte 1 | |
| 6 | Modulator Drive Enable | Bit 7 – 5 | "0" |
| 5 | Pre-Emphasis Enable | 4 – 0 | Mod 1 Attenuation (0 to 12.4dB) |
| 4 | Input Select (Rx/Tx) | | |
| 3 – 0 | Input Level Set (-4dB to 10dB) | Byte 2 | |
| **Mode** | **A/C = $11_H$** | 7 – 5 | "0" |
| Bit 7 | Drive Source | 4 – 0 | Mod 2 Attenuation (0 to 6.2dB) |
| 6 | Deviation Limiter Enable | | |
| 5 | VOGAD Enable | **Volume Set** | **A/C = $13_H$** |
| 4 | De-Emphasis Enable | Bit 7 – 6 | "0" |
| 3 | Signal Select | 5 | Powersave |
| 2 – 0 | Process Gain Set (-4dB to 3dB) | 4 – 0 | Volume Set Attenuation (0 to 48dB) |

*Table 6 "Quick-Reference" to Command Allocations*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX806A J** | -40°C to +85°C (cerdip) |
| | **FX806A LG/LS** | -40°C to +85°C (plastic) |
| Storage temperature range: | **FX806A J** | -55°C to +125°C (cerdip) |
| | **FX806A LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.0MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz *(60% deviation, FM).*

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current (All Elements Enabled) | | – | 8.0 | – | mA |
| (Maximum Powersave) | | – | 0.7 | – | mA |
| **"C-BUS" Interface** | | | | | |
| Input Logic "1" | | 3.5 | – | – | V |
| Input Logic "0" | | – | – | 1.5 | V |
| Input Leakage Current (logic "1 or 0") | | -1.0 | – | 1.0 | µA |
| Input Capacitance | | – | – | 7.5 | pF |
| **Dynamic Values** | | | | | |
| **Overall Performance** | | | | | |
| Microphone Input | 4, 5 | – | 25.0 | – | mVrms |
| Rx Audio In | 6, 5 | 154 | – | 308 | mVrms |
| **Output Drive Levels** | | | | | |
| For 60% Deviation | 5, 7 | 291 | 308 | 326 | mVrms |
| For 100% Deviation | 5, 7, 8 | – | 1,440 | – | mV p - p |
| **Passband Frequencies** | 1 | 297 | – | 3000 | Hz |
| Passband Ripple | 2 | -2.0 | | 0.5 | dB |
| **Stopband Attenuation** | 1, 3 | | | | |
| f = 150Hz | | 10.0 | 12.0 | – | dB |
| f = 3400Hz | | – | 2.0 | – | dB |
| f = 6000Hz | | 30.0 | 36.0 | – | dB |
| f = 8000Hz to 20,000Hz | | – | 60.0 | – | dB |
| **Signal Path Noise** | | | | | |
| Rx | 11 | – | -60.0 | – | dBp |
| Rx | 10 | – | -55.0 | – | dB |
| Tx | 11 | – | -50.0 | – | dBp |
| Tx | 10 | – | -45.0 | – | dB |
| Distortion | | – | 1.0 | – | % |
| **Circuit Elements** – Figure 5 | | | | | |
| **Mic Amp or Mod Summation Amp** | | | | | |
| Open Loop Gain | | – | 50.0 | – | dB |
| Bandwidth | | 20.0 | – | – | kHz |
| Input Impedance | | 10.0 | – | – | MΩ |
| Output Impedance (Open Loop) | | – | 6.0 | – | kΩ |
| (Closed Loop) | | – | 600 | – | Ω |
| **De-emphasis** | | | | | |
| Slope | | – | -6.0 | – | dB/oct. |
| Gain (at 1.0kHz) | | – | 0 | – | dB |
| Input Impedance | | – | 500 | – | kΩ |
| **Voltage Controlled Gain Amp** | | | | | |
| Gain (Non-Compressing) | 5 | – | 6.0 | – | dB |
| (Full Compression) | | – | -24.0 | – | dB |
| VOGAD In Input Impedance | | – | 10.0 | – | MΩ |

## Specification.....

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **VOGAD Peak Detectors** | | | | | |
| Output Impedance - Logic "1" (Compress) | | – | 1.0 | – | kΩ |
| - Logic "0" | | – | 10.0 | – | MΩ |
| Hi/Lo Peak Detector Thresholds | | – | 1,300 | – | mV p - p |
| Hi Peak Detector Threshold | | – | 650 | – | mV +ve pk |
| **Input (Low + Highpass) Filter** | | | | | |
| Gain (at 1.0kHz) | | -1.0 | 0 | 1.0 | dB |
| **Input Level Amp** | | | | | |
| Nominal Adjustment Range | | -4.0 | | 10.0 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| Step Size | | 0.75 | 1.0 | 1.25 | dB |
| **External Audio Buffer** | | | | | |
| Gain | | -0.1 | 0 | 0.1 | dB |
| **Pre-emphasis** (Main Process and VOGAD) | | | | | |
| Slope | | – | 6.0 | – | dB/oct. |
| Gain (at 1.0kHz) | | – | 10.0 | – | dB |
| **Process Highpass Filter** | | | | | |
| Gain (at 1.0kHz) | | -1.0 | 0 | 1.0 | dB |
| **Deviation Limiter** | | | | | |
| Threshold | | – | 1,300 | – | mV p - p |
| Gain | | -0.5 | – | 0.5 | dB |
| **Process Lowpass Filter** | | | | | |
| Gain (at 1.0kHz) | | -1.0 | 0 | 1.0 | dB |
| **Process Gain Amp** | | | | | |
| Nominal Adjustment Range | | -4.0 | | 3.0 | dB |
| Error of any Setting | | -0.5 | – | 0.5 | dB |
| Step Size | | 0.75 | 1.0 | 1.25 | dB |
| Output Impedance | | – | 600 | – | Ω |
| **Transmitter Modulator Drives** | | | | | |
| Input Impedance | | – | 15.0 | – | kΩ |
| **Mod.1 Attenuator** | | | | | |
| Nominal Adjustment Range | | 0 | | 12.4 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| Step Size | | 0.2 | 0.4 | 0.6 | dB |
| Output Impedance | | – | 600 | – | Ω |
| **Mod.2 Attenuator** | | | | | |
| Nominal Adjustment Range | | 0 | | 6.2 | dB |
| Error of any Setting | | -0.6 | – | 0.6 | dB |
| Step Size | | 0.1 | 0.2 | 0.3 | dB |
| Output Impedance | | – | 600 | – | Ω |
| **Audio Output Attenuator** | | | | | |
| Nominal Adjustment Range | | 0 | | 48.0 | dB |
| Error of any Setting | | -1.5 | – | 1.5 | dB |
| Step Size | | – | 1.6 | – | dB |
| Output Impedance | | – | 600 | – | Ω |
| **Miscellaneous Impedances** | | | | | |
| Processed Audio Input | | – | 500 | – | kΩ |
| Calibration Input | | – | 500 | – | kΩ |
| External Process Out | | – | 100 | – | Ω |
| Rx with De-Emphasis By-Pass | | – | 25.0 | – | kΩ |

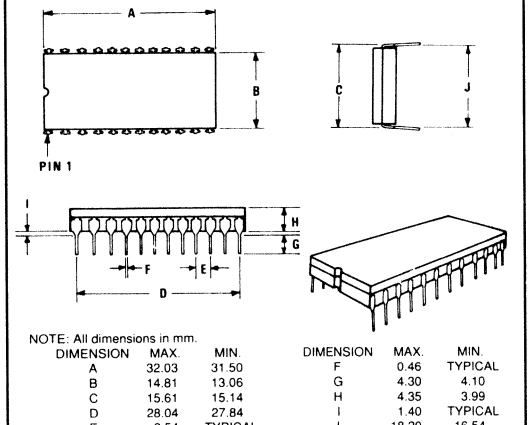
**Notes**

1. Between Mic. or Rx inputs to Modulator or Audio outputs.
2. The deviation from the ideal overall response that includes the pre- or de-emphasis slope.
3. Excluding the effect of the pre- or de-emphasis slope.
4. Producing an output of 0dB with the Mic. Op-Amp set to 6dB (as shown in Figure 2) and the Modulator Drives set to 0dB.
5. With Output Drives set to 0dB and the system calibrated, as described in the Application pages.
6. Input level range for 0dB output, by adjustment of the Input Level Amp.
7. It is recommended that these output levels will produce 60% or 100% deviation in the transmitter.
8. With the microphone input level 20dB above the level required to produce 0dB at the Output Drives.
9. Using external components recommended in Figure 2.
10. In a 30kHz bandwidth.
11. dBp = Psophometrically weighted measurement.

## Package Outline

The FX806AJ, the dual-in-line package is shown in Figure 8, the 'LG' version in Figure 9 and the 'LS' version in Figure 10.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).

*Fig.8* ***FX806AJ*** *24-pin DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. | DIMENSION | MAX. | MIN. |
|---|---|---|---|---|---|
| A | 32.03 | 31.50 | F | 0.46 | TYPICAL |
| B | 14.81 | 13.06 | G | 4.30 | 4.10 |
| C | 15.61 | 15.14 | H | 4.35 | 3.99 |
| D | 28.04 | 27.84 | I | 1.40 | TYPICAL |
| E | 2.54 | TYPICAL | J | 18.20 | 16.54 |

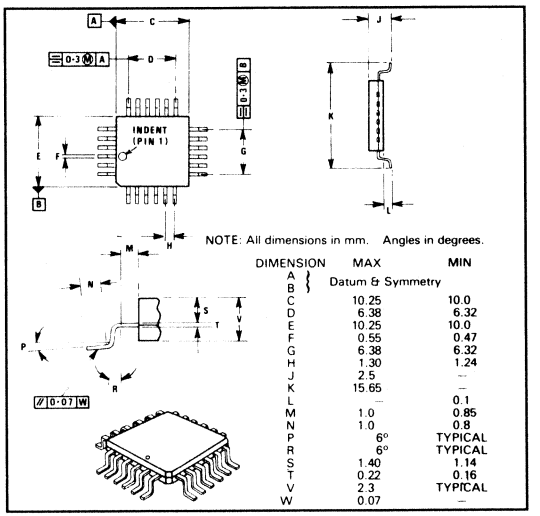
## Ordering Information

| | |
|---|---|
| **FX806AJ** | 24-pin cerdip DIL |
| **FX806ALG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX806ALS** | 24-lead plastic leaded chip carrier |

## Handling Precautions

The FX806A is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

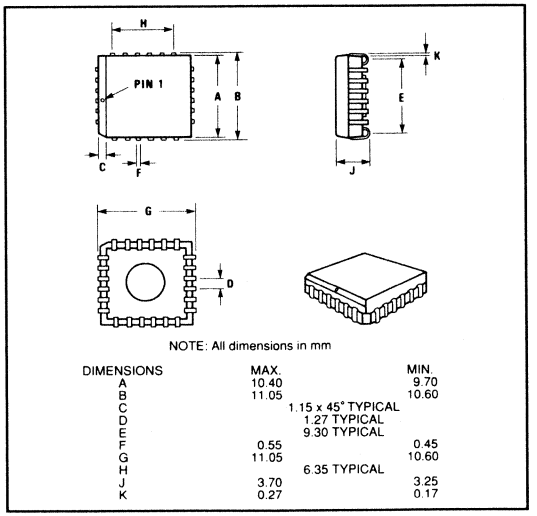
*Fig.9* ***FX806ALG*** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig.10* ***FX806ALS*** *24-lead Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

# FX809
# FFSK Modem

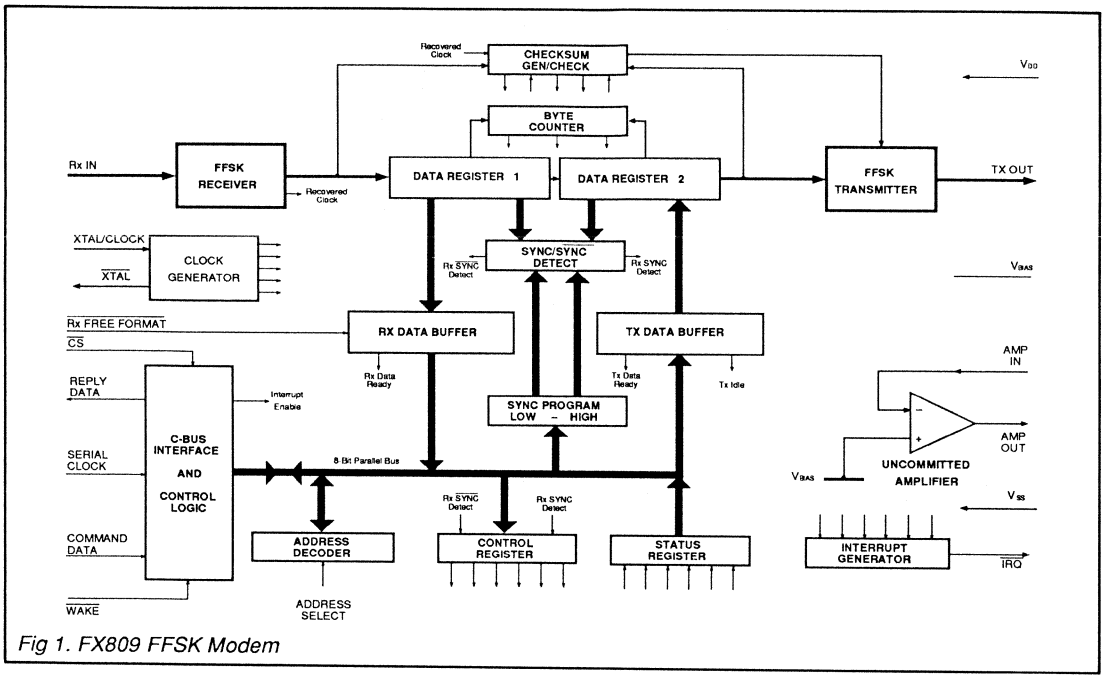



*Fig 1. FX809 FFSK Modem*

## Brief Description

An intelligent, half-duplex, FFSK/MSK modem which operates under "C-BUS" control. In addition this modem provides software selectable checksum generation and error checking, in accordance with MPT1327.

The FX809, using Interrupt and Status Register procedures, performs the functions described below:

**In Tx mode the FX809 will:**

1. (a) Accept from the host and transmit, 8-bit bytes of data as instructed (Preamble, Sync, Address and data).

   (b) internally calculate and insert a 2 byte checksum based upon the preceeding 6 bytes of data, or

   (c) disable the internal checksum generator and continuously transmit the data supplied.
2. Transmit 1 hang-bit and go to Tx Idle when all loaded data bytes have been transmitted.

**In Rx mode the FX809 will:**

1. Detect and achieve bit synchronization within 16 bits.
2. (a) Search and detect the user-programmed Sync (or its opposite logic sense) Word and achieve frame sychronization. Data will then be output in 8-bit bytes via the Rx Data Buffer.

   (b) Use the received checksum to calculate the presence of any errors, setting the Status Register accordingly.
3. Make the incoming data directly available, via the Rx Data Buffer (Rx Freeformat), overriding synchronization requirements.

The FX809 achieves Rx input timing by recovering an Rx clock from the incoming data stream. Output tones are timed to the internally generated transmit clock. Filter, register clocks and transmit FFSK tone frequencies are derived internally from the external Xtal or clock pulse input.

For compliance with the MPT 1327 Signalling Specification a 4.032MHz Xtal or clock input will be required.

*NOTE: All information contained in this data sheet is specified using a 4.032 MHz Xtal, 1200 bps baud rate , Mark and Space frequencies 1200 Hz and 1800 Hz.*

The FX809 is a low-power 5-volt integrated circuit, incorporating "Powersave" modes to further reduce power requirements.

An uncommitted amplifier is provided on chip for general purpose applications within DBS 800.

The FX809 is available in 24-pin cerdip DIL and 24-pin/lead plastic SMD packages.

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## Pin Number Function

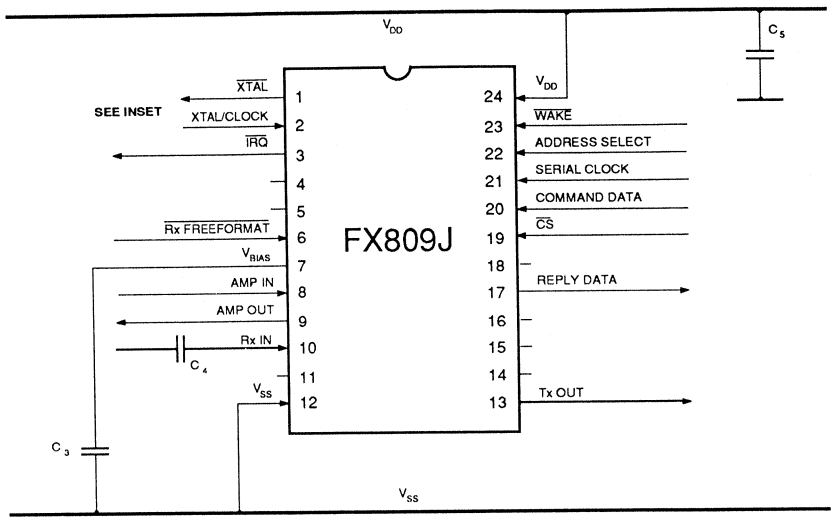
| FX809 J/LG/LS | |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2, INSET. |
| 2 | **Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, INSET. |
| 3 | **Interrupt Request ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low-impedance pulldown to logic "0" when active and a high-impedance when inactive.<br>The conditions that cause interrupts are indicated in the Status Register and are shown below:<br>Tx Idle — Rx Data Ready — Tx Data Ready<br>Rx SYNC Detect — Rx $\overline{\text{SYNC}}$ Detect<br>Interrupt outputs can be disabled by bit 3 of the Control Register. |
| 4 | No Internal connection. |
| 5 | No Internal connection. |
| 6 | **Rx Freeformat:** Used in the Rx mode, this input, when a logic "0," allows received data to be read from the Rx Data Buffer via the Reply Data line without having to acheive byte synchronization (SYNC/$\overline{\text{SYNC}}$) first. Data will continue to be available after this input goes to a logic "1" until either a SYNC or $\overline{\text{SYNC}}$ Prime bit is set or the modem set to Tx mode. When held at a logic "1" the modem operates normally. This pin has an internal 1MΩ pullup resistor.<br>**NOTE:** If this input is held at a logic "0" in the Tx mode, the Rx Data Ready bit in the Status Register may occasionally be set, but not cause an interrupt. If this input is a logic "0" when going into the Rx mode, an Rx Data Ready interrupt may be generated immediately, in this case the first byte of Rx data should be ignored. |
| 7 | **$V_{BIAS}$ :** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$ by capacitor $C_3$, see Figure 2. |
| 8 | **Amp In:** The inverting input to the on-chip uncommitted amplifier . |
| 9 | **Amp Out:** The output of the on-chip uncommitted amplifier. |
| 10 | **Rx In:** The 1200 baud, 1200Hz/1800Hz, received FFSK signal input. The input signal to this pin must be a.c. coupled via capacitor $C_4$, see Figure 2. |
| 11 | No Internal connection. |
| 12 | **$V_{SS}$:** Negative Supply (GND). |

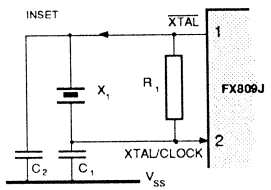
| Pin Number FX809 J/LG/LS | Function |
|---|---|
| 13 | **Tx Out:** The 1200 baud, 1200Hz/1800Hz FFSK Tx output. When not transmitting data the output impedance of this pin is high. On power-up, this output can be any level, a General Reset command is required to ensure that this output attains $V_{BIAS}$ initially. |
| 14 | No Internal connection. |
| 15 | No Internal connection. |
| 16 | No Internal connection. |
| 17 | **Reply Data:** The "C-BUS", serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams and System Support Document, Document 2. |
| 18 | No Internal connection. |
| 19 | **Chip Select ($\overline{CS}$):** The "C-BUS" data loading control function, this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing Diagrams and System Support Document, Document 2. |
| 20 | **Command Data:** The "C-BUS," serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams and System Support Document, Document 2. |
| 21 | **Serial Clock:** The "C-BUS," serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the FFSK Modem. See Timing Diagrams and System Support Document, Document 2. |
| 22 | **Address Select:** This pin enables two FX809 devices to be used on the same "C-BUS," providing full-duplex operation. When at a logic "1" Address/Command bytes (with the exception of a General Reset) must have bit 3 set to a logic "1" to address this device. See Tables 1 and 2. |
| 23 | **$\overline{Wake}$:** This input can be used to reactivate the FX809 from the 'Powersave' condition. The device will be in a 'Powersave' condition when both this pin and bit 2 of the Control Register are set to a logic "1." Recovery from Powersave is achieved by putting either the $\overline{Wake}$ pin or the Powersave bit in the Control Register to a logic "0." This allows FX809 activation by the µController or an external signal, such as R.S.S.I. or Carrier Detect. |
| 24 | $V_{DD}$: Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the FFSK Modem are dependant upon this supply. |

| Powersave (CR bit 2) | $\overline{Wake}$ | FX809 Condition |
|---|---|---|
| 1 | 1 | Powersave |
| 0 | 1 | Enabled |
| 1 | 0 | Enabled |
| 0 | 0 | Enabled |

**NOTE**: Pins 4, 5, 11, 14, 15, 16 and 18 may be connected to $V_{SS}$ to improve screening.

## External Components




| Component | | Value |
|---|---|---|
| $R_1$ | = | 1.0MΩ |
| $C_1$ | | 33.0pF |
| $C_2$ | | 33.0pF |
| $C_3$ | | 1.0µF |
| $C_4$ | | 0.1µF |
| $C_5$ | | 1.0µF |
| $X_1$ | | 4.032MHz |

Tolerance: R = ±10% C = ±20%

*Fig.2 External Components*

## Modem Performance

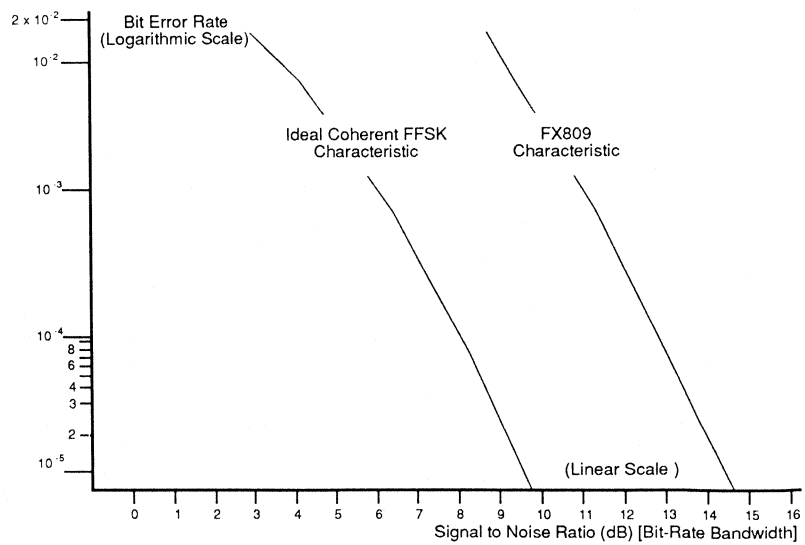



*Fig.3 Bit Error Rate vs Signal-to-Noise Ratio*

## Controlling Protocol

Control of the functions within the FX809 FFSK Modem is by a group of Address/Commands (A/Cs) and appended data to and from the system µController via "C-BUS." Provision is made to address 2 separate FFSK Modems. The use of these instructions is detailed in the following paragraphs and tables.

| Command Assignment | Address/Command (A/C) Byte Hex | Binary MSB LSB | | Notes |
|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | Control Register bits set to logic "0" |
| Write to Control Register | 40 | 0 1 0 0 0 0 0 0 | + | 1 byte instruction to Control Reg. |
| Read Status Register | 41 | 0 1 0 0 0 0 0 1 | + | 1 byte reply from Status Reg. |
| Read Rx Data Buffer | 42 | 0 1 0 0 0 0 1 0 | + | 1 byte of data from Rx Data Buffer |
| Write to Tx Data Buffer | 43 | 0 1 0 0 0 0 1 1 | + | 1 byte of data to Tx Data Buffer |
| Write to SYNC Program | 44 | 0 1 0 0 0 1 0 0 | + | 2 bytes of SYNC Word to SYNC Prog. Reg. |

*Table 1 Modem No.1 "C-Bus" Address/Commands* – (Address Select input at a logic "0")

### Address/Commands

Instruction and data transactions to and from the FX809 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data, or
(ii) a Status or Rx data Reply.

Control and configuration is by writing instructions from the µController to the Control Register [$40_H$, ($48_H$)].

Reporting of FX809 configurations is by reading the Status Register [($41_H$, ($49_H$)]. Instructions and data are transferred, via "C-BUS," in accordance with the timing information given in Figure 4.

Data for transmission as FFSK is sent to the Tx Data Buffer via the Command Data line. Received data is read from the Rx Data Buffer via the Reply Data line.

Instruction and data transactions to and from this device are preceded by the relevant Address/Command (A/C).

"C-BUS" allocations for the FX809 are shown in Tables 1 and 2.

A complete list of DBS 800 "C-BUS" Address/Command allocations is published in the System Support Document, Document 2.

| Command Assignment | Address/Command (A/C) Byte Hex | Binary MSB LSB | | Notes |
|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | Control Register bits set to logic "0" |
| Write to Control Register | 48 | 0 1 0 0 1 0 0 0 | + | 1 byte instruction to Control Reg. |
| Read Status Register | 49 | 0 1 0 0 1 0 0 1 | + | 1 byte reply from Status Reg. |
| Read Rx Data Buffer | 4A | 0 1 0 0 1 0 1 0 | + | 1 byte of data from Rx Data Buffer |
| Write to Tx Data Buffer | 4B | 0 1 0 0 1 0 1 1 | + | 1 byte of data to Tx Data Buffer |
| Write to SYNC Program | 4C | 0 1 0 0 1 1 0 0 | + | 2 bytes of SYNC Word to SYNC Prog. Reg. |

*Table 2 Modem No.2 "C-Bus" Address/Commands* – (Address Select input at a logic "1")

### Address Select

This input allows, using the correct addressing, 2 FFSK Modems on the same BUS.

When operating in a system employing 2 FFSK Modems, 1 FFSK Modem is designated No.1 and requires its Address Select input to be held at a logic "0", and the second FFSK Modem (No. 2) requires its Address Select input to be held at logic "1."

All "C-BUS" transactions with Modem 1 will use Address/Command allocations $40_H$ to $44_H$ (Table 1) and transactions with Modem 2 will use $48_H$ to $4C_H$ (Table 2).

For explanation purposes further descriptions in this publication of FX809 FFSK Modem internal register functions will deal primarily with FFSK Modem No. 1 (Address Select at logic "0").

## Controlling Protocol...

**"Write to Control Register"** This 'Write Only' register directs the modem's operation.

| Setting | Control Bits |
|---|---|
| ***MSB*** | ***Transmitted First*** |
| ***Bit 7*** | Not used<br>Set to<br>"0" |
| ***6*** | Not used<br>Set to<br>"0" |
| ***5*** | **$\overline{\text{SYNC}}$ Prime** |
| 0 | |
| 1 | Primed |
| ***4*** | **SYNC Prime** |
| 0 | |
| 1 | Primed |
| ***3*** | **Interrupt Enable** |
| 0 | Disable |
| 1 | Enable |
| ***2*** | **Powersave** |
| 0 | Normal Operation |
| 1 | Powersave |
| ***1*** | **Checksum Enable** |
| 0 | Disable |
| 1 | Enable |
| ***0*** | **Rx/Tx Mode** |
| 0 | Rx |
| 1 | Tx |

*Table 3 Control Register*

**$\overline{\text{SYNC}}$ Prime** When set, this bit enables $\overline{\text{SYNC}}$ Word detection.
Cleared on a successful $\overline{\text{SYNC}}$ Word detection.

**SYNC Prime** When set, this bit enables SYNC Word detection.
Cleared on a successful SYNC Word detection.

**Interrupt Enable** When set, this bit allows interrupts to be output by the FX809 on the $\overline{\text{IRQ}}$ line.

**Powersave** Used in conjunction with the $\overline{\text{Wake}}$ input (see Pin Functions) to control the Powersave state of the FX809.

**Checksum Enable** When set:
**In Tx:** a 2-byte checksum is generated and transmitted after every 6 bytes transmitted.
**In Rx:** After every 8 received bytes (6 information + 2 checksum) the checksum word is checked. If the checksum is correct, the Rx Checksum True bit in the Status Register is set to a logic "1."
When this bit is a logic "0" no checksums are generated or checked.
**NOTE:** Checksum operation is inhibited during the SYNC/$\overline{\text{SYNC}}$ search period.

### "Read Rx Data Buffer"

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Rx Data Buffer** | | | | | | | |

### Rx Data Buffer

This "Read Only' register contains the last byte of data received from the Data Register. Received Bit 7 (MSB) first.

### "Write to Tx Data Buffer"

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Tx Data Buffer** | | | | | | | |

### Tx Data Buffer

This "Write Only" register contains the next byte of data to be transmitted. Bit 7 (MSB) will be transmitted first.

### "Write to Sync Program"

| MSB Byte 1 | | | | | | | | | | | Byte 0 | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **SYNC High** | | | | | | | | **SYNC Low** | | | | | | | |

### SYNC Program

This "Write Only" register is loaded with the required Sync Word. This word (or its opposite logic sense, $\overline{\text{SYNC}}$) is compared with the received synchronization word. If the required SYNC Word is less than 16 bits, the remaining bits must be programmed as preamble (10101010..etc.) bit 15 (MSB) is loaded first.

## Controlling Protocol...

**"Read Status Register"** This 'Read Only' register will indicate the source of FX809 interrupts ($\overline{IRQ}$'s).

| *Reading* | *Status Bits* |
|---|---|
| ***MSB*** | ***Received First*** |
| ***Bit 7*** | Undefined |
| 0 | "0" or, |
| 1 | "1" |
| ***6*** | Undefined |
| 0 | "0" or, |
| 1 | "1" |
| ***5*** | **Rx $\overline{SYNC}$ Detect** |
| 0 | |
| 1 | $\overline{SYNC}$ |
| ***4*** | **Rx SYNC Detect** |
| 0 | |
| 1 | SYNC |
| ***3*** | **Tx Idle** |
| 0 | |
| 1 | Idle |
| ***2*** | **Tx Data Ready** |
| 0 | |
| 1 | Tx Data Ready |
| ***1*** | **Rx ChecksumTrue** |
| 0 | |
| 1 | True |
| ***0*** | **Rx Data Ready** |
| 0 | |
| 1 | Rx Data Ready |

*Table 4 Status Register*

**Rx Checksum True**
Set and an Interrupt generated by successful comparison of the received and self generated checksums.

Cleared by (i) reading the Status Register and the Rx Data Buffer,
(ii) $\overline{Rx}$/Tx being taken to logic "1."

**Rx $\overline{SYNC}$ Detect**
Set and an Interrupt generated when the correct $\overline{SYNC}$ Word is detected (if $\overline{SYNC}$ Prime is set).

Cleared by (i) reading the Status Register,
(ii) Setting Rx/Tx to logic "1."

**Rx SYNC Detect**
Set and an Interrupt generated when the correct SYNC Word is detected (if SYNC Prime is set).

Cleared by (i) reading the Status Register,
(ii) Setting Rx/Tx to logic "1."

**Tx Idle**
Set and an Interrupt generated when all loaded Tx data and 1 'hang-bit' have been transmitted.

Cleared by (i) writing to the Tx Data Buffer,
(ii) Setting Rx/Tx to logic "0."

**Tx Data Ready**
Set and an Interrupt generated indicating that a byte of data should be written to the Tx Data Buffer.

Cleared by (i) reading the Status Register and writing a byte of data to the TX Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "0."

**Rx Data Ready**
Set and an Interrupt generated, indicating that the Rx Data Buffer is full, a byte of data is to be read from the Rx Data Buffer, this must be read within 8 bit periods.

Cleared by (i) reading the Status Register and the Rx Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "1."

---

### Interrupt Requests ($\overline{IRQ}$)

The conditions that cause interrupts to be output (if enabled by the Control Register) from the FX809 are:

**Tx Idle**
**Tx Data Ready**
**Rx $\overline{SYNC}$ Detect**
**Rx Data Ready**
**Rx SYNC Detect**

To ascertain the cause of the interrupt the Status Register should be read.

Interrupts are cleared:

(i) by a read of the Status Register, or

(ii) by changing the state of the $\overline{Rx}$/Tx bit.

### General Reset

Upon Power-Up, the bits in the FX809 Modem registers and buffers will be random (either "0" or "1"). The General Reset command ($01_H$) will "reset" all microcircuits on the "C-BUS" and has the following effect on the FX809:

All bits in the Control Register will be set to logic "0." The Tx Out output will be set to $V_{BIAS}$.

**NOTE:** That the Status Register, Rx Data Buffer, Tx Data Buffer and Sync Program register are not affected by the General Reset command.

# "C-BUS" Timing Information

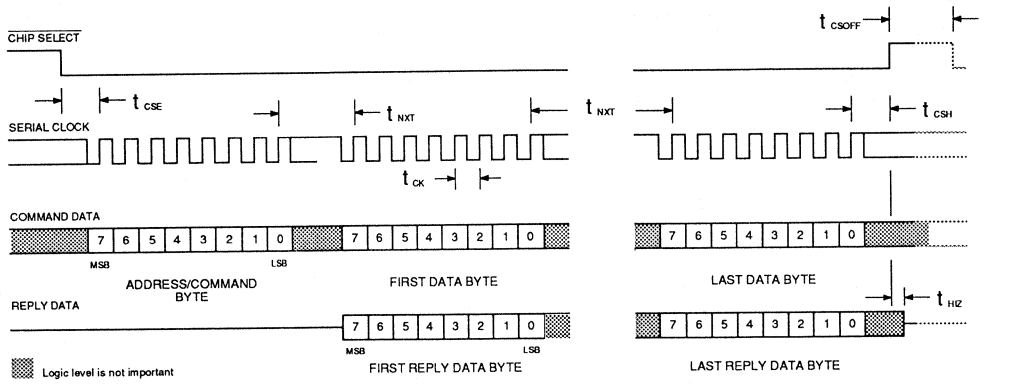



*Fig.4 "C-BUS" Timing*

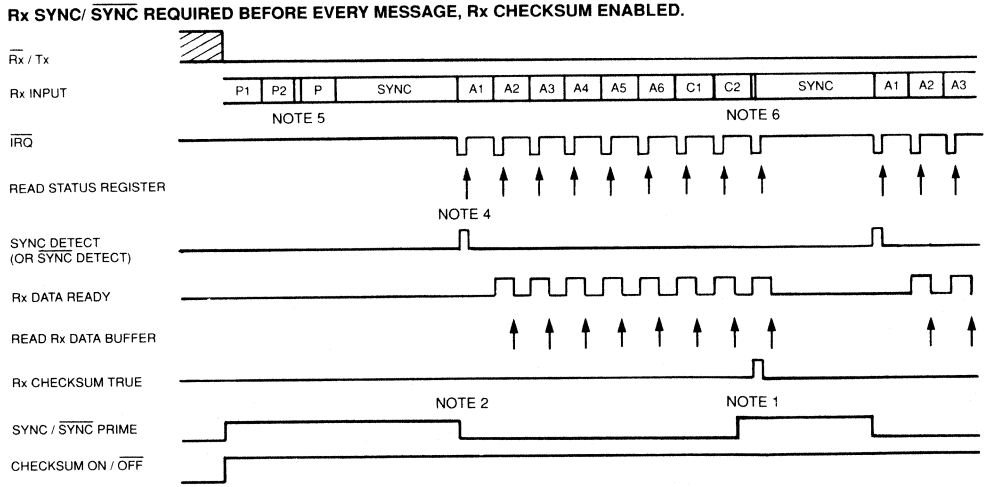
**"C-BUS" Timing** – Figure 4

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| $t_{CSE}$ | 2.0 | – | µs |
| $t_{CSH}$ | 4.0 | – | µs |
| $t_{HIZ}$ | – | 2.0 | µs |
| $t_{CSOFF}$ | 2.0 | – | µs |
| $t_{NXT}$ | 4.0 | – | µs |
| $t_{CK}$ | 2.0 | – | µs |

**Notes**

(1) Depending on the command, 1 or 2 bytes of Command Data is transmitted to the peripheral MSB (bit7) first, LSB (bit0) last. Reply Data is read from the peripheral MSB (bit7) first, LSB (bit0) last.
(2) Data is clocked into and out of the peripheral on the rising Serial Clock edge.
(3) Loaded commands are acted upon at the end of each command.
(4) To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity Serial Clock pulses.

# Modem Timing Information

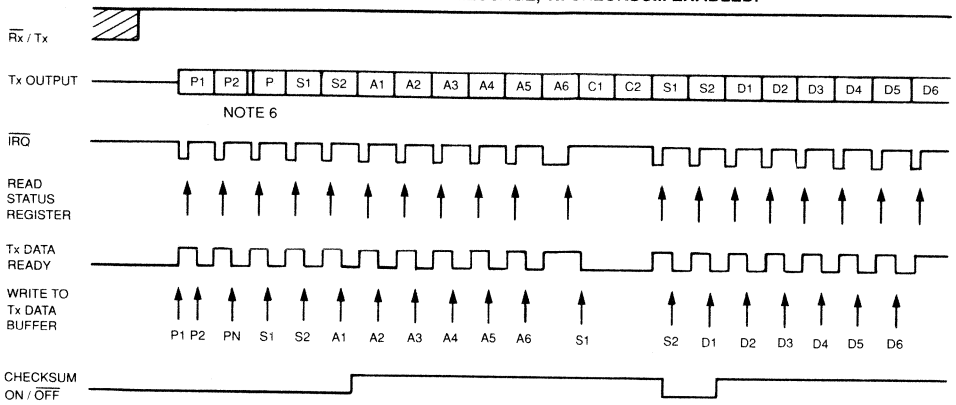



NOTES
1). The SYNC and SYNC detector searches the incoming bit stream starting at the end of the byte in which SYNC/SYNC prime was set.
2). After detection of a SYNC/SYNC word the SYNC/SYNC prime bits automatically go low (control bits 5 and 6: detector off).
3). The checksum checker is inhibited during the time SYNC/SYNC search is operating.
4). The status register will indicate whether SYNC or SYNC was detected here.
5). Any number of preamble bits can occur here.
6). Any number of bits can occur here.
7). Rx Freeformat set high.

*Fig.5 Rx 1*

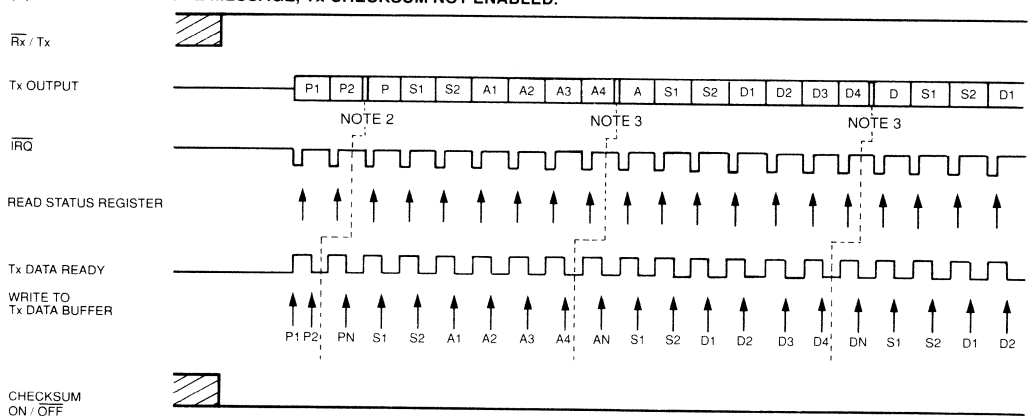
# Tx Timing Information

**(a) Tx MORE THAN ONE MESSAGE, SYNC BEFORE EVERY MESSAGE, Tx CHECKSUM ENABLED.**




NOTES
1). Preamble and SYNC bytes are loaded as data from the µC.
2). The Tx output will be held at bias level when no data is being transmitted.
3). Tx byte synchronisation is established by the loading of the first preamble byte from the µC.
4). Checksum must be turned off during preamble and SYNC words.
5). When Rx/Tx is low Tx output is at bias.
6). Any number of preamble bytes can occur here.

**(b) Tx MORE THAN ONE MESSAGE, Tx CHECKSUM NOT ENABLED.**

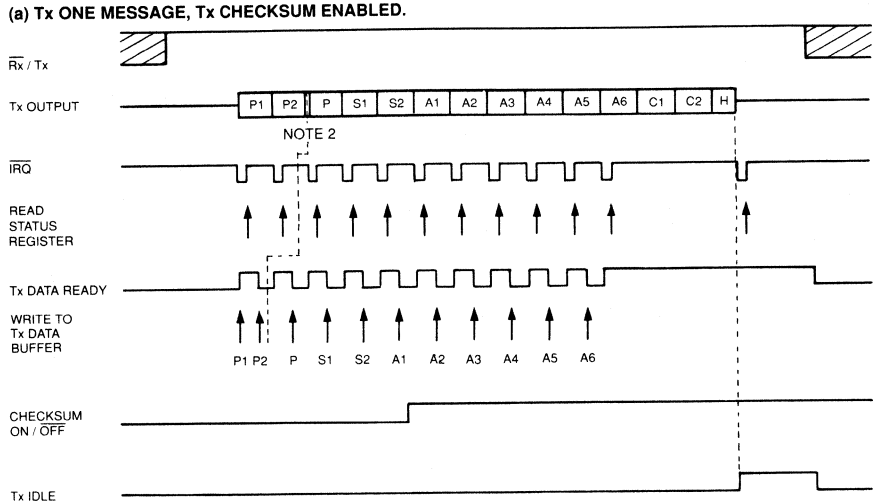



NOTES
1). Preamble, SYNC words and checksums are supplied by the µC in this format as data bytes.
2). Any number of preamble bytes can occur here.
3). Any number of address/data bytes can occur here.

*Fig.6 Tx Timing*

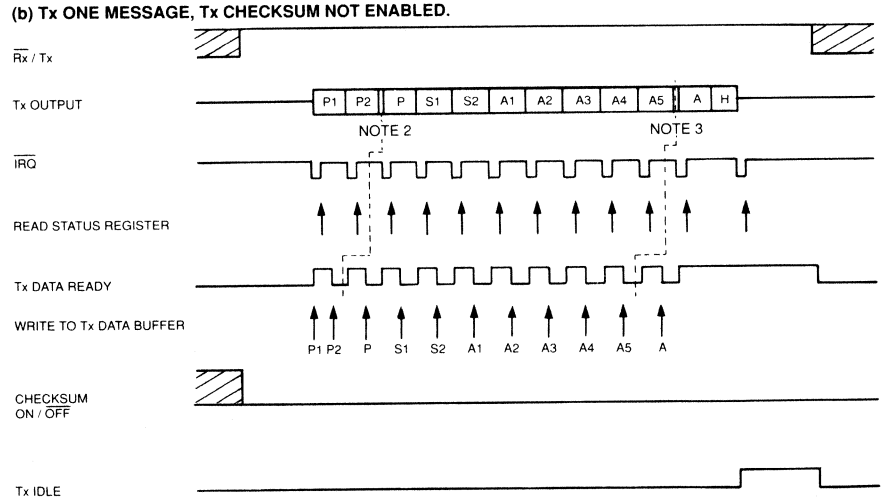
# Tx Timing Information...

**(a) Tx ONE MESSAGE, Tx CHECKSUM ENABLED.**




NOTES
1). H is the "Hangover" bit (Logic 1) appended to the transmitted message before transmission is terminated.
2). Any number of preamble bytes can occur here.
3). Transmission terminates after C1, C2 and H. Termination occurs when no further data bytes are written to the Tx data buffer.

**(b) Tx ONE MESSAGE, Tx CHECKSUM NOT ENABLED.**



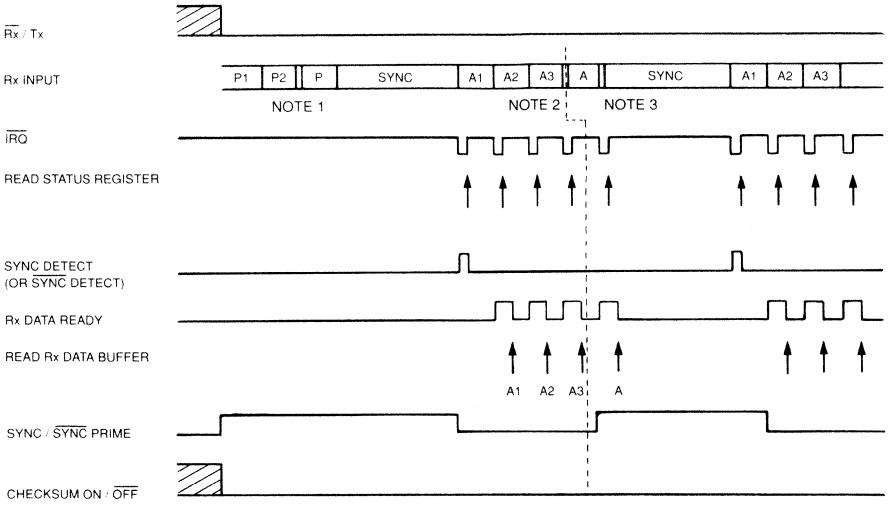

NOTES
1). H is the "Hangover" bit (Logic 1) appended to the transmitted message before transmission is terminated.
2). Any number of preamble bytes can occur here.
3). Any number of address/data bytes can occur here.
4). Transmission terminates when no more data bytes are loaded into the Tx data buffer.

NOTES
i). A – Address bytes.
ii). C – Checksum bytes.
iii). D – Data bytes.
iv). H – Hang bit.
v). P – Preamble bytes.
vi). X – Don't care state.
vii). Tx only – In Tx, Preamble and SYNC are loaded as data from the microcontroller.

*Fig.7 Tx Timing*

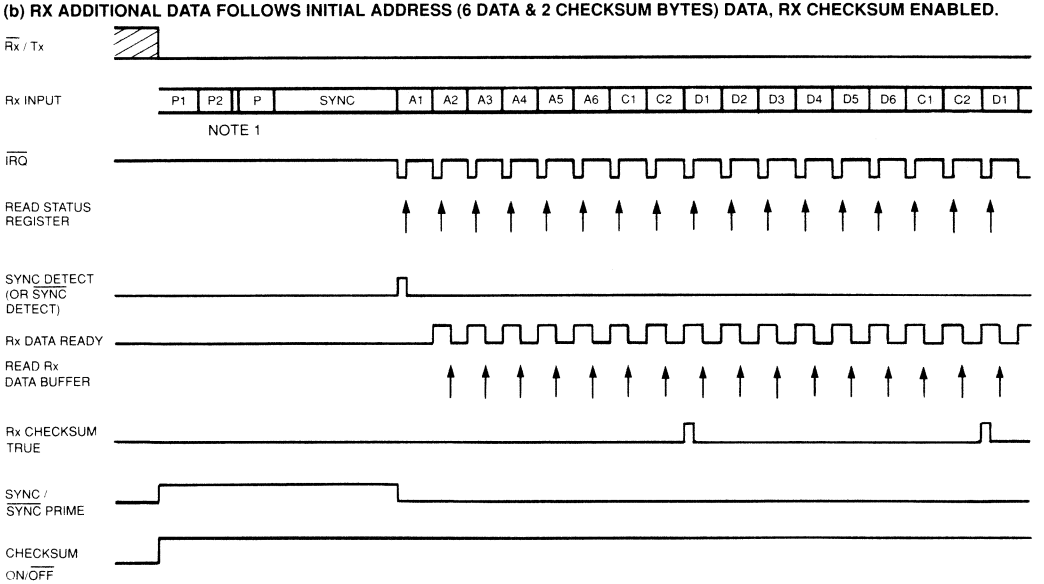
# Rx Timing Information

**(a) Rx SYNC/ $\overline{\text{SYNC}}$ REQUIRED BEFORE EVERY MESSAGE, Rx CHECKSUM NOT ENABLED.**




NOTES
1). Any number of preamble bits can occur here.
2). Any number of address/data bytes can occur here.
3). Any number of bits can occur here.
4). Rx Freeformat set high.

**(b) RX ADDITIONAL DATA FOLLOWS INITIAL ADDRESS (6 DATA & 2 CHECKSUM BYTES) DATA, RX CHECKSUM ENABLED.**




NOTES
1). Any number of preamble bits can occur here.
2). Rx Freeformat set high.

NOTES
i). A – Address bytes.
ii). C – Checksum bytes.
iii). D – Data bytes.
iv). H – Hang bit.
v). P – Preamble bytes.
vi). Z – Don't care state.
vii). Tx only – In Tx, Preamble and SYNC are loaded as data from the microcontroller.

*Fig.8 Rx Timing*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX809J** | -40°C to +85°C (cerdip) |
| | **FX809LG/LS** | -40°C to +85°C (plastic) |
| Storage temperature range: | **FX809J** | -55°C to +125°C (cerdip) |
| | **FX809LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.032MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz.

Bit Rate = 1200bp/s.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | | | | |
| Enabled | | – | 5.0 | – | mA |
| Powersave | | – | 2.0 | – | mA |
| **Dynamic Values** | | | | | |
| **Digital Interface** | | | | | |
| Input Logic "1" | 1 | 3.5 | – | – | V |
| Input Logic "0" | 1 | – | – | 1.5 | V |
| Output Logic "1" ( IOH = -120µA) | 2 | 4.6 | – | – | V |
| Output Logic "0" ( IOL = 360µA) | 2, 3 | – | – | 0.4 | V |
| Digital Input Current | | | | | |
| $V_{IN}$ = Logic "1" or "0" | 1 | – | – | 1.0 | µA |
| Digital Input Capacitance | 1 | – | – | 7.5 | pF |
| Tri-state "Off" Leakage Current | 8 | -4.0 | – | 4.0 | µA |
| **Analogue Impedances** | | | | | |
| Rx Input | | 100 | – | – | kΩ |
| Tx Output | | | | | |
| Transmitting Data | | – | 6.0 | 10.0 | kΩ |
| Not Transmitting Data | | – | 1.0 | – | MΩ |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | – | – | MΩ |
| $R_{OUT}$ | | 5.0 | – | 15.0 | kΩ |
| Gain | | – | 15.0 | – | dB |
| Frequency | 4 | – | 4.032 | – | MHz |
| **Receiver** | | | | | |
| Signal Input Levels | 5 | -9.0 | -2.0 | 10.5 | dB |
| Bit Error Rate | | | | | |
| at 12dB SNR | | – | 7.0 | – | $10^{-4}$ |
| at 20dB SNR | | – | 1.0 | – | $10^{-8}$ |
| Synchronization at 12dB SNR | 6 | | | | |
| Probability of Bit 8 being correct | | – | 99.0 | – | % |
| Probability of Bit 16 beng correct | | – | 99.5 | – | % |

## Specification...

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Dynamic Values .....** | | | | | |
| **Transmitter** | | | | | |
| Output Level | | – | 0 | – | dB |
| Output Level Variation | | -1.0 | – | 1.0 | dB |
| Output Distortion | | – | 3.0 | 5.0 | % |
| 3rd Harmonic Distortion | | – | 2.0 | 3.0 | % |
| Logic "1" Frequency | 7 | – | 1200 | – | Hz |
| Logic "0" Frequency | 7 | – | 1800 | – | Hz |
| Isochronous Distortion | | | | | |
| 1200Hz – 1800Hz | | – | 25.0 | 40.0 | µs |
| 1800Hz – 1200Hz | | – | 20.0 | 40.0 | µs |
| **Uncommitted Amplifier** | | | | | |
| Bandwidth | | – | 200 | – | kHz |
| Gain | | – | 50.0 | – | dB |
| Input Impedance | | 1.0 | – | – | MΩ |
| Output Impedance | | – | – | 10.0 | kΩ |

**Notes**

1. Device control pins; Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. $\overline{\text{IRQ}}$ output.
4. For baud rate specified (1200 baud).
5. Signal-to-Noise Ratio = 50dB.
6. The response time is measured using a 10101010.....101 signal input pattern at 230mVrms (-2.5dB) with no noise.
7. Dependant upon Xtal tolerance.
8. $\overline{\text{IRQ}}$ and Reply Data outputs, for $V_{SS} < V_{OUT} < V_{DD}$.

---

**Generation**

The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
This 16–bit word is used as the "Checksum."

**Checking**

The checksum checker does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

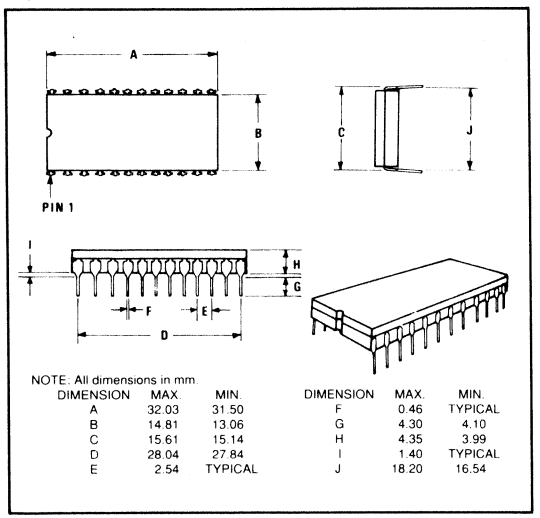
$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero.
Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).
If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (Status Register bit-1) is set.

## Package Outline

The FX809J, the dual-in-line package, is shown in Figure 9. The 'LG' version is shown in Figure 10 and the 'LS' version in Figure 11.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).

*Fig. 9* **FX809J** *24-pin DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. | DIMENSION | MAX. | MIN. |
|---|---|---|---|---|---|
| A | 32.03 | 31.50 | F | 0.46 | TYPICAL |
| B | 14.81 | 13.06 | G | 4.30 | 4.10 |
| C | 15.61 | 15.14 | H | 4.35 | 3.99 |
| D | 28.04 | 27.84 | I | 1.40 | TYPICAL |
| E | 2.54 | TYPICAL | J | 18.20 | 16.54 |

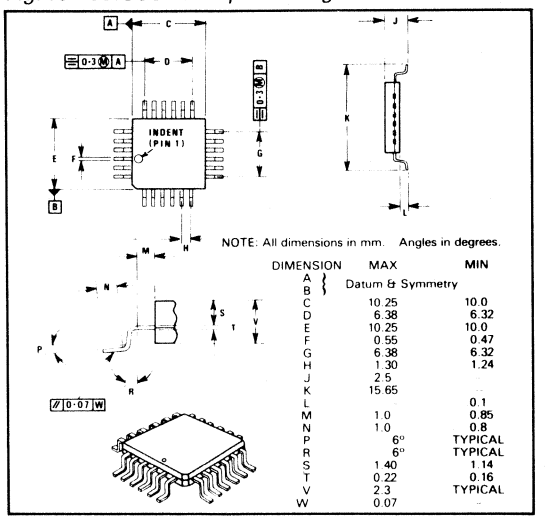
## Ordering Information

| | |
|---|---|
| **FX809J** | 24-pin cerdip DIL |
| **FX809LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX809LS** | 24-lead plastic leaded chip carrier |

## Handling Precautions

The FX809 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

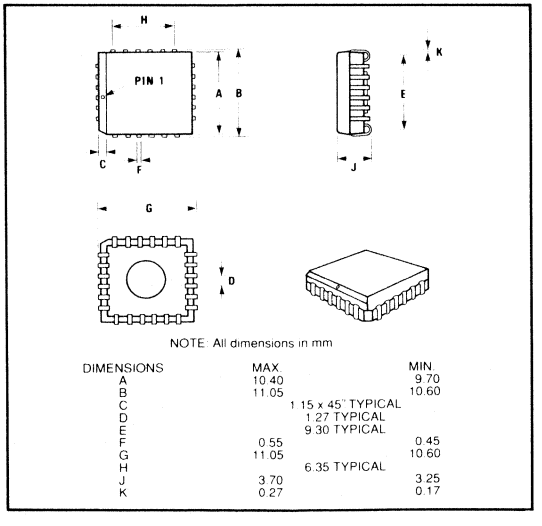
*Fig. 10* **FX809LG** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | |
| K | 15.65 | |
| L | | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | |

*Fig. 11* **FX809LS** *24-lead Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

# CML Semiconductor Products

PRODUCT INFORMATION

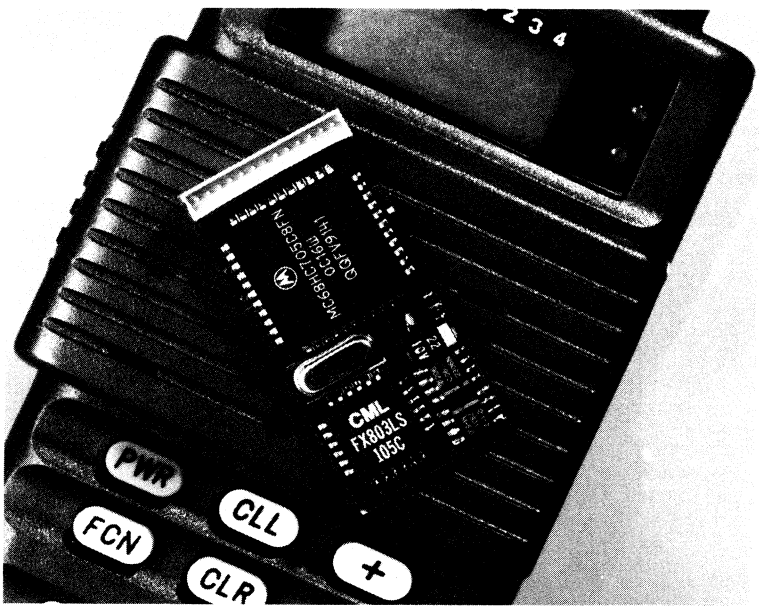
# CM1481 Non-Predictive Selcall Module

Publication Adv/1481/2 February 1993
Advance Information

## Applications

- Selcall in Two-Way Radio
- Alarm Systems
- Remote Control/Switching
- 'SECURE' Control and Switching
- Industrial Control
- Automatic User Identification

★ *'N'-TONE SELCALL ENCODING & NON-PREDICTIVE DECODING + GROUP CALLING* ★




**CM1481**

Module actual size is
*45mm x 22mm x 8mm*

## Features

★ Encoding and Non-Predictive All-Tone Decoding

★ All-System Group-Call

★ Transponding and ANI

★ Over-Air *"Stun" and "Release", "Re-Configuration" and "Reset"*

★ PTT Lockout

★ Low-Power Requirement (4.0mA @ 6V to 26V D.C. [typ])

★ CCIR, EEA and ZVEI Tonesets

★ Simple, Serial Configuration

★ PTT Time-Out Timer

★ Multiple Coded Audio Alerts

'Typical' power is specified with reference to operating periods of: 10% Tx, 10% Rx and 80% standby; No loading.

# CM1481 - An Introduction

**CM1481**

A compact 5- or 6-Tone CCIR, EEA and ZVEI Selcall module with individual address encoding, non-predictive all-tone decoding, transponding and full, all-system group-call and ANI capabilities.

In addition to normal Selective Call facilities, the CM1481 offers, ***As Standard .....***

*Over-Air — "Stun" and "Release"* - Allowing base control in respect of disabling an addressed unit remotely due to theft, unpaid fees or air misuse/abuse!

*Over-Air — "Address/Mode Re-Configuration"* - Rapid, remote address and mode re-configuration - allowing unit participation in an alternative working group.

*Over-Air — "Reset"* - The base will call, and on completion of the transaction, may reset the unit, remotely, without operator intervention.

The CM1481 has a low-power requirement of 4.0mA (typ) at supply inputs between 6 and 26 volts d.c.

*Typical' power is specified with reference to operating periods of: 10% Tx, 10% Rx and 80% standby. No loading.*

The CM1481 is completely software configured, and as such, requires no internal links or switches.

Initial configuration of all module parameters is via a simple serial link to the on-board µController from the printer port of a "PC" or compatible computer employing the menu-driven software provided.
Parameter variations available are described in the table on the Back Page of this document.

Major inputs and outputs can be software configured to active "high" or "low" levels.

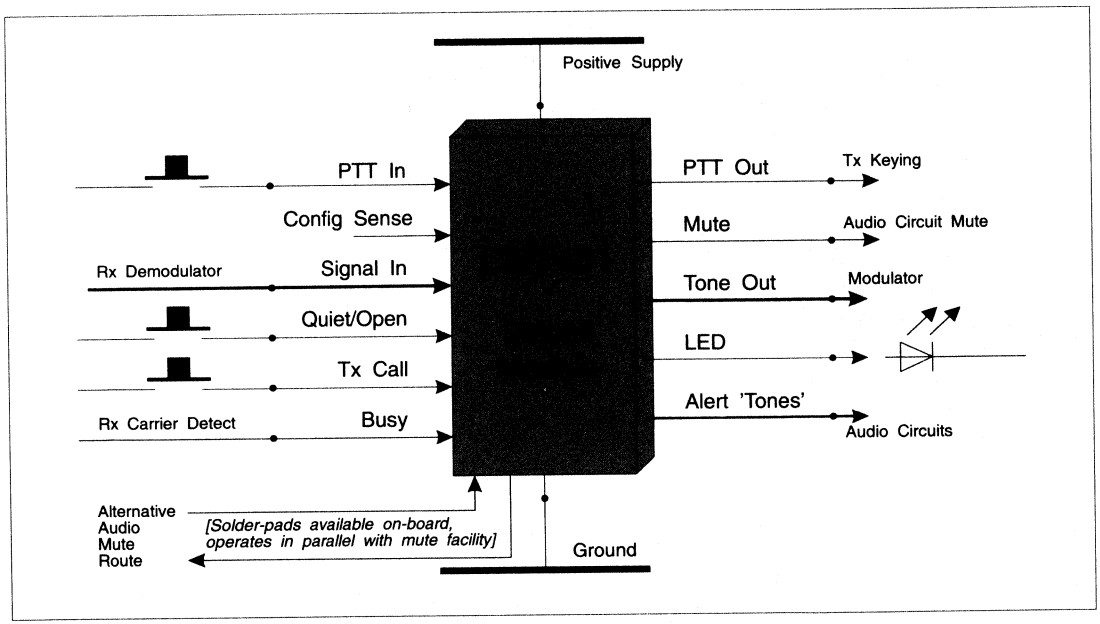
The supplied Configuration software and the CM1481 have the added ability, with a radio Tx/Rx, to originate and progress Over-Air operations from a PC terminal; this includes supplying security checks

Selective Call activity is indicated by multiple coded audio alerts; an LED drive output is available.

**Applications Include**

Selcall in Two-Way Radio systems
Alarms
Remote Control via radio or wire requiring security and noise immunity.

## CM1481 - The Radio Interface - connection of the CM1481 to a radio unit is via a simple 13-pin radio interface.

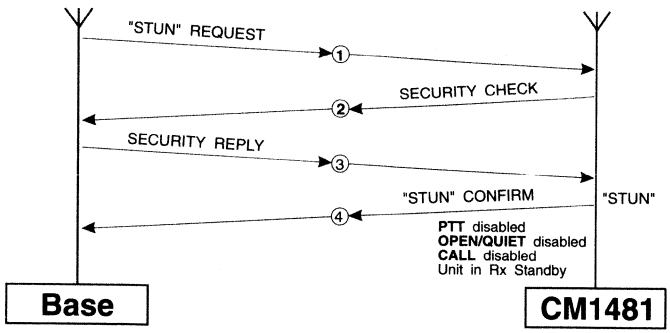



## CM1481 - A Summary of Standard Functions and Features

- **Configuration by Menu-Driven Serial 'PC' Link**
- **CCIR, EEA and ZVEI Toneset/Length Capabilities**
- **HSC Signalling Control Features**
- **Over-Air "Stun" & "Release"**
- **Rapid Over-Air "Re-Configuration"**
- **Remote Reset**
- **Individual Addressing**
- **Extended Group & Data Tone Facilities**
- **Simple Radio Interface**
- **Low-Power Requirement (4.0mA typ)**
- **"Muted" Call Initiation**
- **Programmable I/O Polarities**
- **Lead/Trail Automatic Number Identification (ANI)**
- **Programmable Lead-In Tone/Delay**
- **Transponding Facility**
- **Single or Dual Button Operation**
- **Timed Mute Reset**
- **Tx (PTT) Time Out + Warning**
- **Operators Audio Alerts**
- **PTT (Busy) Lockout**
- **CMOS Compatible Logic**
- **Coded Call-Alert Capability**

# CM1481 - Special Over-Air Functions

**Over-Air Stun and Release** - To completely disable (or enable) any unit by a simple, but secure authentication command. To prevent mistaken or accidental operations, CM1481 over-air transactions, "Stun", "Release" and "Re-Configure", are carried out using a secure authentication protocol based upon the synchronization of two pseudo-random number generators. The system is similar to that used in the over-air synchronization of rolling-code speech scramblers. The diagram below describes, basically, a "Stun" transaction sequence.




Once a unit has been "STUNned", it can only be "Released" by a base conducted Re-Configuration or by performing an over-air "Release".

**Operation**

1. Base initiates "STUN" Request.
2. CM1481 transmits 'SEED' for security-check pseudo-random number generation and an address check. Both units generate a 'number.'
3. Base replies with its 'number.'
4. CM1481 compares 'numbers', a valid comparison places unit into the "STUN" mode and confirms this action to base.

## Over-Air Re-Configuration

An over-air function which allows the base station to remotely change the following CM1481 parameters:

| | |
|---|---|
| Tx Address | Rx Address |
| Transpond Address | Transpond Mode |
| ANI Address | ANI Mode |

Employs the same secure type authentication sequence as described above.

## Remote Reset

An over-air function which allows the base station to remotely reset a CM1481 unit.

The base sends the unit's Selcall address with the Remote Reset tone 'C' or 'D' appended.

Secure authentication is not used in this transaction.

## Selective Calling - Message Composition and Coding

| a1 | a2 | a3 | a4 | a5 | (a6) | (C/D) | (B) | | |
|---|---|---|---|---|---|---|---|---|---|
| 5 Tone Hexadecimal Sequential Code (HSC) Address | | | | | Optional 6th 'Address' Tone | Optional Remote Reset Tone | Optional Data Prefix (B) Tone | Additional (HSC) Function Tones | |

All calls, commands and interrogations to, and calls and replies from, the CM1481 are prefixed with a 5 (or 6) tone HSC format address. Full international group-calling is possible to more than one user group via GROUP (A) and REPEAT (E) tones. Data function tones appended after the data-prefix tone (B) to the control the operation of all CM1481 transactions.

### HSC Tone Signalling

| | |
|---|---|
| **'0' thro' '9'** | Decimal digit value. |
| **'A'** | Address GROUP character or character 'A' in the data-field. |
| **'B'** | Data prefix character. |
| **'C' & 'D'** | Address code suffixes - to signal Remote Reset (Mute). |
| **'E'** | REPEAT character. |
| **'F'** | Available as a Lead-In Tone and used as the transpond 'BEEP' character. |

### CM1481 Function Tones

| | |
|---|---|
| **'0'** | *Reserved for future functions.* |
| **'1'** | "STUN" Request. |
| **'2'** | "SECURITY" Check. |
| **'3'** | "SECURITY" Reply. |
| **'4'** | "CONFIGURE" Request. |
| **'5'** | "RELEASE" Request. |
| **'6'** | "STUN" Confirm. |
| **'7'** | "RELEASE" Confirm. |
| **'8'** | "CONFIGURE" Confirm. |
| **'9'** | *Reserved for future functions.* |

# CM1481 - Specifications

## Technical Details

| | | |
|---|---|---|
| Temperature Range | 0°C to +70°C | |
| Supply Voltage | 6 to 26 volts d.c. | |
| Operating Current | 4.6mA -duty cycle (no LED) | |
| | 10% Tx, 10% Rx, 80% standby | |
| Standby Current | 2.5mA | typ |
| Logic "1" In | 3.5 to 26 volts d.c. | typ |
| Logic "0" In | 0 to 1 volt d.c. | typ |
| PTT & Mute Out | Open Collector | 50mA max |
| LED Drive Current | 25mA | max |
| Tone Out Accuracy | ±0.1% | max |
| Level | 308mV rms | typ |
| Decode Sensitivity | 31mV rms | min |

**Alert Signals -**

| | |
|---|---|
| Unit Muted | - short duration high-pitch beep |
| Unit Unmuted | - short duration low-pitch beep |
| Call Received | - continuous rapid mid-pitch beeps |
| Group Call Received | - 3 short duration mid-pitch beeps |
| Call Transmitted | - short duration mid-pitch beep |
| Tx Time-Out Warning | - short duration high-pitch beep |
| PTT Action Disabled | - continuous low-pitch tone |
| Call Action Disabled | - continuous low-pitch tone |

| | |
|---|---|
| PCB Size | 45mm x 22mm x 8mm |
| Interface Connector | 13-pin SIL male |

**Toneset Details** - the table below details the relevant system tone frequencies available within the CM1481. All tones are available; Configuration will allocate the active set.

| Tone | EEA | CCIR | ZVEI 1 | PZVEI | ZVEI 2 | ZVEI 3\DZVEI |
|---|---|---|---|---|---|---|
| **0** | 1981 Hz | 1981 Hz | 2400 Hz | 2400 Hz | 2400 Hz | 2200 Hz |
| **1** | 1124 | 1124 | 1060 | 1060 | 1060 | 970 |
| **2** | 1197 | 1197 | 1160 | 1160 | 1160 | 1060 |
| **3** | 1275 | 1275 | 1270 | 1270 | 1270 | 1160 |
| **4** | 1358 | 1358 | 1400 | 1400 | 1400 | 1270 |
| **5** | 1446 | 1446 | 1530 | 1530 | 1530 | 1400 |
| **6** | 1540 | 1540 | 1670 | 1670 | 1670 | 1530 |
| **7** | 1640 | 1640 | 1830 | 1830 | 1830 | 1670 |
| **8** | 1747 | 1747 | 2000 | 2000 | 2000 | 1830 |
| **9** | 1860 | 1860 | 2200 | 2200 | 2200 | 2000 |
| **A** | 1055 | 2400 | 2800 | 970 | 885 | 825 |
| **B** | 930 | 930 | 810 | 810 | 810 | 740 |
| **C** | 2247 | 2247 | 970 | 2800 | 740 | 2600 |
| **D** | 991 | 991 | 885 | 885 | 680 | 885 |
| **E** | 2110 | 2110 | 2600 | 2600 | 970 | 2400 |
| **F** | 2400 | 1055 | 680 | 680 | 2600 | 680 |

**CM1481 - Configuration Menu** - the diagram shown below indicates the functions of the CM1481 and the options that may be achieved via software configuration.

| | |
|---|---|
| Toneset | **EEA** CCIR ZVEI1 ZVEI2 ZVEI3 PZVEI |
| Tone Length | **30ms** to 150ms in 10ms steps |
| Lead-In Delay | **0** to 2550ms in 10ms steps |
| Lead-In Tone Length | **0** to 2550ms in 10ms steps |
| Lead-In Tone Digit | **0** 1 2 3 4 5 6 7 8 9 A B C D E F |
| NoTone Timer | **20ms** to 300ms in 20ms steps |
| PTT Time-Out | **0** to 248sec in 1sec steps |
| Pseudo Iterations | **1** to 255 in steps of 1 |
| Timed Mute Reset | **0** to 255secs in 1sec steps |

| | | | |
|---|---|---|---|
| PTT In: | Active | **LOW** | HIGH |
| PTT Out: | Active | **LOW** | HIGH |
| Busy: | Active | **LOW** | HIGH |
| Mute: | Active | **HIGH** | LOW |
| LED: | Active | **HIGH** | LOW |
| Quiet/Open: | Active | **LOW** | HIGH |
| Call: | Active | **LOW** | HIGH |

| | |
|---|---|
| Transmit Address | **5** or *6* Tones |
| Receive Address | **5** or *6* Tones |
| ANI Address | **5** or *6* Tones |
| Transpond Address | **5** or *6* Tones |
| Extended Group Tone (Tx) | **No** Yes |
| Number of Called Alerts | **4** to 60 in steps of 4 |
| Extended Data Tone Tx) | **No** Yes |
| Call When Muted | **No** Yes |
| Radio "Stunned" | **No** Yes |
| Operation | **Single** Dual -Button |
| Start-Up State | **Muted** Unmuted |
| ANI Mode | **OFF** Lead Trail Lead & Trail |
| Transpond Mode | **OFF** Address Beep |
| Tones per Address | **5** *6* |
| Lead-In Gap | **No** Yes |
| Over-Air Functions | **No** Yes |

** A comprehensive Operating and Programming Manual is supplied with the CM1481 module **

# Integrated Circuits Data Book

Section 3

# Cellular Radio

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX304 C-Net Audio Processor

Publication D/304/5 December 1991
Provisional Issue

## Features/Applications

- Full Duplex Audio Processing
- Designed to meet Net-C Cellular Specification
- On-Chip Audio Bandpass Filters (300-3000Hz)
- Fixed Frequency Inversion
- Clear/Invert Facility
- Output Enable/Disable
- High Baseband and Carrier Rejection
- Independent I/P Gain Adjustment
- On-Chip Clock Oscillator Circuits
- Crystal Oscillator Stability
- Single 5V CMOS Process
- Surface Mount and DIL Package Styles

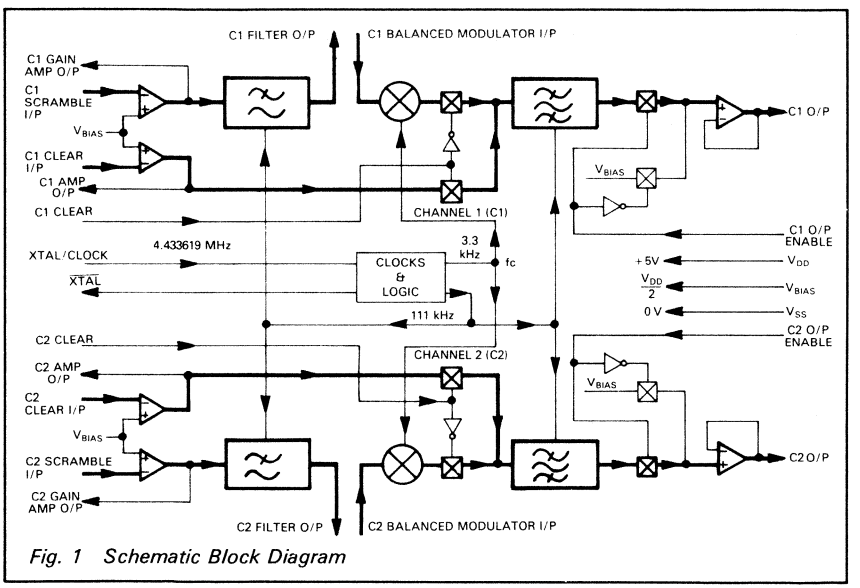



*Fig. 1 Schematic Block Diagram*

**FX304**

## Brief Description

The FX304 is a duplex filter array and frequency inversion scrambler compatible with the Net-C specification. The two channels, C1 and C2 are identical and independent, each consisting of:

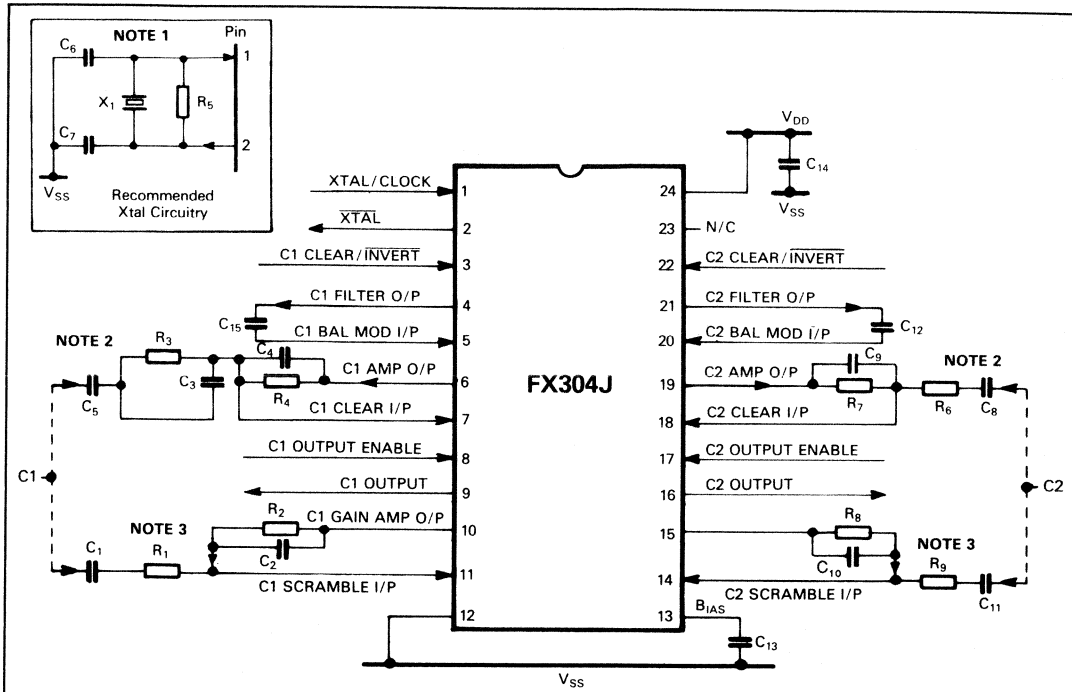
1. A 10th order 3.1kHz input lowpass filter in the 'Invert' path.
2. A balanced modulator providing fixed frequency inversion (3.3kHz) and having high baseband and carrier rejection.
3. A 14th order channel output bandpass filter (300Hz to 3kHz).
4. Input Op-Amps in both 'Clear' and 'Invert' paths allowing external components to set input gains, and pre-emphasis or de-emphasis in the 'Clear' path.
5. Clear/$\overline{\text{Invert}}$ switching causing automatic changover of signal routes and input circuitry.
6. A buffered low noise output with switching clock filter.
7. An output enable switching facility.

Both filter sets meet the Net-C specification and use switched capacitor technology. The common carrier frequency and filter switching clock are generated on-chip using an external 4.433619MHz Xtal or clock input.
The FX304 is a low-power, single 5V CMOS device and is available in 24-pin DIL and 24-pin plastic SMD packages.

| Pin Number | | | Functions |
|---|---|---|---|
| DIL FX304J | Quad Plastic FX304LG | PLCC FX304LS | |
| 1 | 1 | 1 | **Xtal/Clock:** 4.433619MHz Xtal or externally derived clock is injected at this pin. See Fig. 2. |
| 2 | 2 | 2 | **$\overline{\text{Xtal}}$:** Output of clock oscillator inverter. |
| 3 | 3 | 3 | **C1 Clear/$\overline{\text{Invert}}$:** Controls the operation of channel 1 modulation. See Table 1. Internal 1MΩ pull-up. |
| 4 | 4 | 4 | **C1 Filter Output:** The output of the channel 1 input filter. It is to be coupled to "C1 balanced modulator input" via a 1.0μF capacitor ($C_{15}$). See Fig. 2. |
| 5 | 5 | 5 | **C1 Balanced Modulator Input:** The input to channel 1 balanced modulator. Internally biased at $V_{DD}/2$, it is to be coupled to "C1 Filter Output" via a 1.0μF capacitor ($C_{15}$). See Fig. 2. |
| 6 | 6 | 6 | **C1 Amp Output:** Channel 1 amplifier, with external components (see Fig. 2) can be used to provide pre-emphasis, de-emphasis and/or gain in the 'Clear' path. |
| 7 | 7 | 7 | **C1 Clear Input:** The negative input of channel 1 amplifier for use in the 'Clear' path. Recommended external components shown in Fig. 2. |
| 8 | 8 | 8 | **C1 Output Enable:** Controls the status of channel 1 output. See Table 1. Internal 1MΩ pull-up. |
| 9 | 9 | 9 | **C1 Output:** The analogue output of channel 1, Internally biased at $V_{DD}/2$. Output state is dependent on channel 1 "Clear/Invert" and "Output Enable" pins. See Table 1. |
| 10 | 10 | 10 | **C1 Gain Amp Output:** The output pin of Channel 1 gain adjusting op-amp, see Fig. 2 for gain setting components. |
| 11 | 11 | 11 | **C1 Scramble Input:** The analogue signal input to channel 1 in the 'Invert' mode. This input is to a gain adjusting op-amp whose gain is set by external components. See Fig. 2. |
| 12 | 12 | 12 | **$V_{SS}$:** Negative Supply (GND). |
| 13 | 13 | 13 | **Bias:** The analogue bias line at $V_{DD}/2$. It should be decoupled to $V_{SS}$ via a 1.0μF or greater capacitor. See Fig. 2. |
| 14 | 14 | 14 | **C2 Scramble Input:** The analogue signal input to channel 2 in the 'Invert' mode. This input is to a gain adjusting op-amp whose gain is set by external components. See Fig. 2. |
| 15 | 15 | 15 | **C2 Gain Amp Output:** The output pin of Channel 2 gain adjusting op-amp, see Fig. 2 for gain setting components. |
| 16 | 16 | 16 | **C2 Output:** The analogue output of channel 2, internally biased at $V_{DD}/2$. Output state is dependent on channel 2 "Clear/Invert" and "Output Enable" pins. See Table 1. |
| 17 | 17 | 17 | **C2 Output Enable:** Controls the status of channel 2 output. See Table 1. Internal 1MΩ pull-up. |
| 18 | 18 | 18 | **C2 Clear Input:** The negative input of channel 2 amplifier for use in the 'Clear ' path. Recommended external components shown in Fig. 2. |
| 19 | 19 | 19 | **C2 Amp Output:** Channel 2 amplifier with external components (see Fig. 2) can be used to provide pre-emphasis, de-emphasis and/or gain in the 'Clear' path. |
| 20 | 20 | 20 | **C2 Balanced Modulator Input:** The input to channel 2 balanced modulator. Internally biased at $V_{DD}/2$, it is to be coupled to 'C2 Filter Output' via 1.0μF capacitor ($C_{12}$). See Fig. 2. |
| 21 | 21 | 21 | **C2 Filter Output:** The output of the channel 2 input filter. It should be coupled to "C2 Balanced Modulator Input" via a 1.0μF capacitor ($C_{12}$). See Fig. 2. |
| 22 | 22 | 22 | **C2 Clear/$\overline{\text{Invert}}$:** Controls the operation of channel 2 modulation. See Table 1. Internal 1MΩ pull-up. |
| 23 | 23 | 23 | **No Connection.** |
| 24 | 24 | 24 | **$V_{DD}$:** A positive 5V supply. |

*Table 1 Output Control*

| Channel 1/2 | | |
|---|---|---|
| **Clear/$\overline{\text{Invert}}$** | **Output Enable** | **Output** |
| 1 | 1 | Clear |
| 0 | 1 | Frequency Inverted |
| X | 0 | $V_{DD}/2$ |




| Component References | | |
|---|---|---|
| Component | Unit Value | Note |
| $R_1$ | 100k | 3 |
| $R_2$ | 100k | 3 |
| $R_3$ | 200k | 2 |
| $R_4$ | 75k | 2 |
| $R_5$ | 1M | 1 |
| $R_6$ | 240k | 2 |
| $R_7$ | 330k | 2 |
| $R_8$ | 100k | 3 |

| Component References | | |
|---|---|---|
| Component | Unit Value | Note |
| $R_9$ | 100k | 3 |
| $C_1$ | 0.1$\mu$ | |
| $C_2$ | 120p | 3 |
| $C_3$ | 1n | 2 |
| $C_4$ | 120p | 2 |
| $C_5$ | 0.1$\mu$ | |
| $C_6$ | 33p | 1 |
| $C_7$ | 47p | 1 |

| Component References | | |
|---|---|---|
| Component | Unit Value | Note |
| $C_8$ | 2.2n | |
| $C_9$ | 1n | 2 |
| $C_{10}$ | 120p | 3 |
| $C_{11}$ | 0.1$\mu$ | |
| $C_{12}$ | 1.0$\mu$ | |
| $C_{13}$ | 1.0$\mu$ | |
| $C_{14}$ | 0.47$\mu$ | |
| $C_{15}$ | 1.0$\mu$ | |
| $X_1$ | 4.433619MHz | |

**Tolerance**
*Resistors ±10%*
*Capacitors ±20%*

**Notes:**

1. *Xtal circuitry shown is in accordance with CML Application Note D/XT/1 April '86.*
2. *'Clear' channel inputs are shown with Ch1 (pre-emphasis) and Ch2 (de-emphasis) components. See figures 4 and 5.*
3. *Gain setting components for the 'scrambled paths' are shown for a gain of 0dB. See figure 6.*

*Fig. 2 External Component Connections*

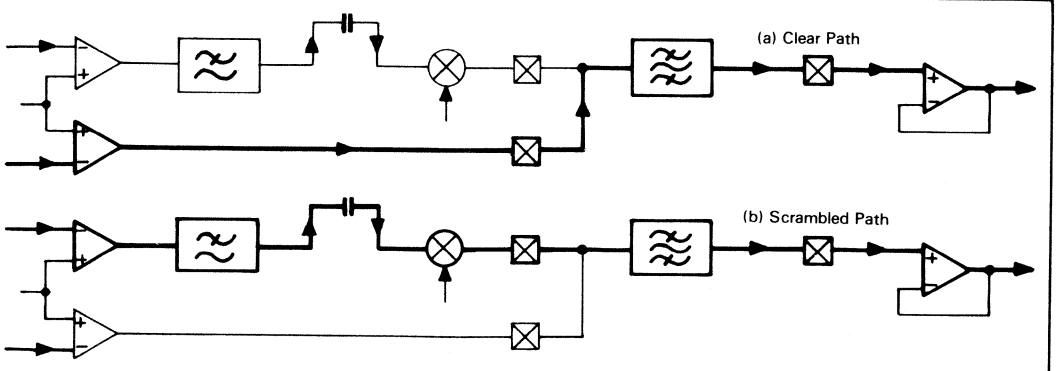



*Fig. 3 Simplified Signal Paths*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (supply pins) | | ±30mA |
| (other pins) | | ±20mA |
| Total device dissipation @ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX304J** | −30°C to +85°C (Ceramic) |
| | **FX304LG/LS** | −30°C to +70°C (Plastic) |
| Storage temperature range: | **FX304J** | −55°C to +125°C (Ceramic) |
| | **FX304LG/LS** | −40°C to +85°C (Plastic) |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

$V_{DD}$ = 5V, $T_{amb}$ = 25°C, $\phi$ = 4.433619MHz, Audio Level Ref: 0dB = 775mVrms @ 1kHz.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | 1 | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | — | 7.0 | — | mA |
| Input Impedance (Digital) | | 100 | — | — | kΩ |
| Input Impedance (Amplifiers) | | 1.0 | 10 | — | MΩ |
| Input Impedance (Bal Mod) | | — | 20 | — | kΩ |
| Output Impedance (L P Filters) | | — | 2.0 | — | kΩ |
| Output Impedance (C1, C2) | | — | 150 | 800 | Ω |
| Output Impedance (C1, C2 Amps) | | — | 10 | — | kΩ |
| Inputs Logic '1' | | 3.5 | — | — | V |
| Inputs Logic '0' | | — | — | 1.5 | V |
| **Dynamic Values:** | 1 | | | | |
| Analogue Signal Input Levels | | −30 | — | +6 | dB |
| Analogue Signal Output Levels | | −30 | — | +6 | dB |
| Unwanted Modulation Products | 2 & 3 | — | — | −40 | dB |
| Carrier Breakthrough | 2 & 3 | — | −55 | — | dB |
| Baseband Breakthrough | 2 & 3 | — | — | −40 | dB |
| Carrier Frequency | | — | 3299 | — | Hz |
| Analogue Output Noise | 4 | — | −50 | — | dB |
| **Filters:** | | | | | |
| **Input Low Pass Filter** | | | | | |
| Cut-off Frequency (−3dB) | | — | 3100 | — | Hz |
| Passband Ripple (300Hz—3kHz) | | — | 1.0 | — | dB |
| Attenuation at 3.3kHz | | — | 30 | — | dB |
| Attenuation at 3.6kHz | | — | 50 | — | dB |
| Passband Gain | | — | 0.5 | — | dB |
| **Output Band Pass Filter** | 5 | | | | |
| Passband Frequencies | | 300 | | 3000 | Hz |
| Passband Ripple | | — | 1.0 | — | dB |
| Low Freq. Roll-off <200Hz | | 12 | — | — | dB/oct |
| High Freq. Roll-off >3.4kHz | | 24 | — | — | dB/oct |
| Passband Gain | | 3 | 4 | 5 | dB |
| **Overall Modulated or De-Modulated Channel Response** | | | | | |
| Passband Frequencies | | 300 | | 3000 | Hz |
| Passband Ripple | | −3 | | +1 | dB |
| Low Freq. Roll-off <250Hz | | 18 | — | — | dB/oct |
| High Freq. Roll-off >3.4kHz | | 18 | — | — | dB/oct |
| Passband Gain | 5 | — | 2 | — | dB |
| Distortion | 2 | — | 2.0 | — | % |

**Notes:** *1. Dynamic Characteristics specified at 5V $V_{DD}$.*
*2. Measured with Input Level −3dB.*
*3. Single Modulated Channel.*
*4. Short circuit input, any analogue output, in 30kHz bandwidth.*
*5. Op Amp gain 0dB.*

## Channel Performances

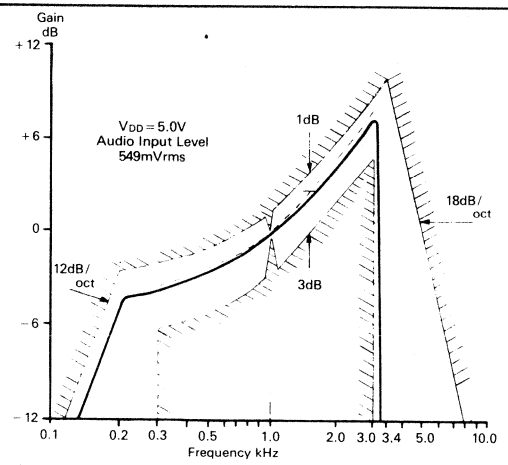



*Fig. 4 Typical Audio Frequency Response of Transmit Path in 'Clear'*

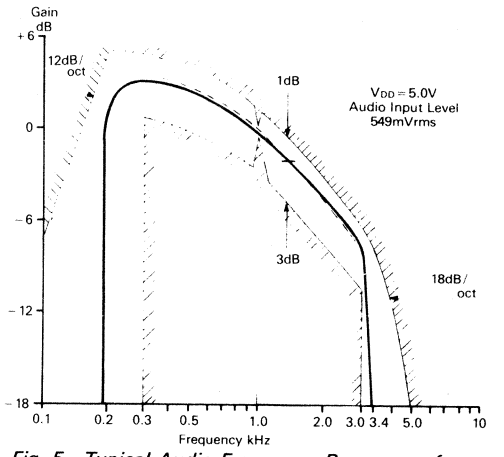



*Fig. 5 Typical Audio Frequency Response of Receive Path in 'Clear'*

### Clear and Scramble Passbands

Gain levels on these diagrams are with respect to an audio input level of 549mVrms.

Figure 4 shows the FX304 'Clear' path response compared with the Net-C specification, using Pre-emphasis components at the input with a time constant of 200 $\mu$s. See figure 2.

Figure 5 shows the FX304 'Clear' path response compared with the Net-C specification, using De-emphasis components at the input with a time constant of 200$\mu$s. See figure 2.

Figure 6 shows the FX304 overall response of a scrambled or de-scrambled channel compared with the Net-C specification.

An attenuation of approximately 4dB from the balanced modulator and a gain of 4dB from the output bandpass filter result in 0dB Passband Gain in the 'Scramble' path.

In the 'Clear' path the 4dB gain of the output bandpass filter must be considered and compensated for by the input components (as in figure 2) for an overall Passband Gain of 0dB.

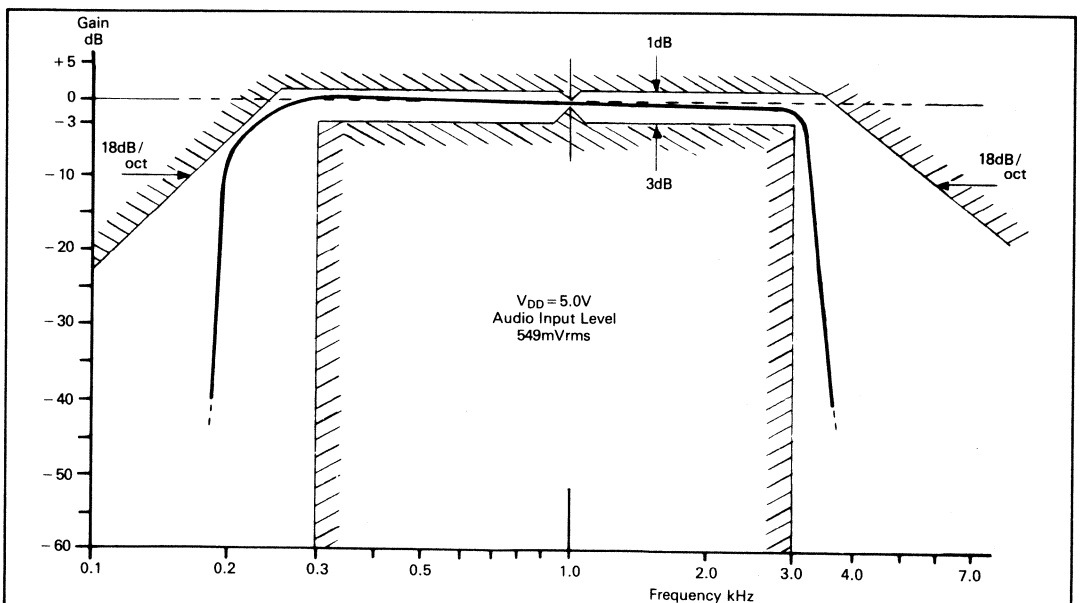
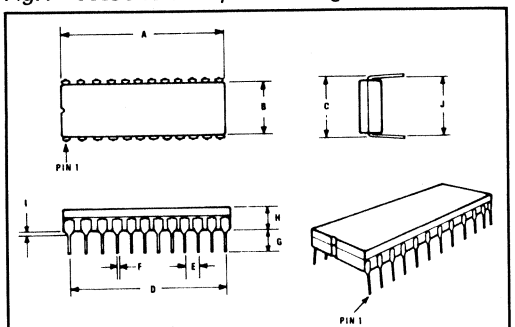



*Fig. 6 Typical Audio Frequency Response of a Single Scrambled or De-Scrambled Channel*

## Package Outlines

The FX 304J, the cerdip package, is illustrated in figure 7. The 'LG' version is shown in figure 8 and the 'LS' version in figure 9.
To allow complete identification the FX304LG and LS packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 7* **FX304J** *Cerdip DIL Package*



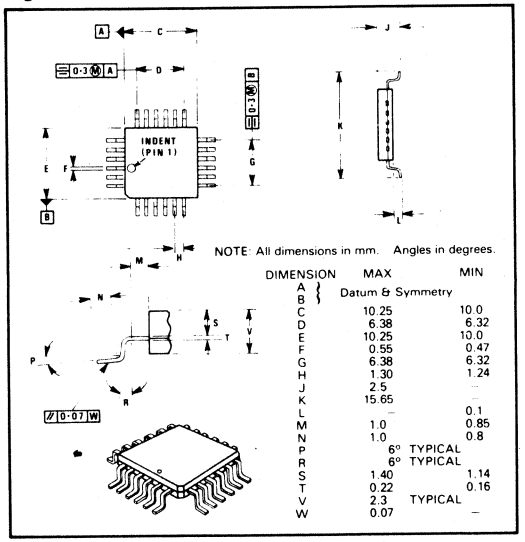

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 32.03 | 31.50 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 } | TYPICAL |
| F | 0.46 } | |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 | TYPICAL |
| J | 18.20 | 16.54 |

## Handling Precautions

The FX304J/LG/LS is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

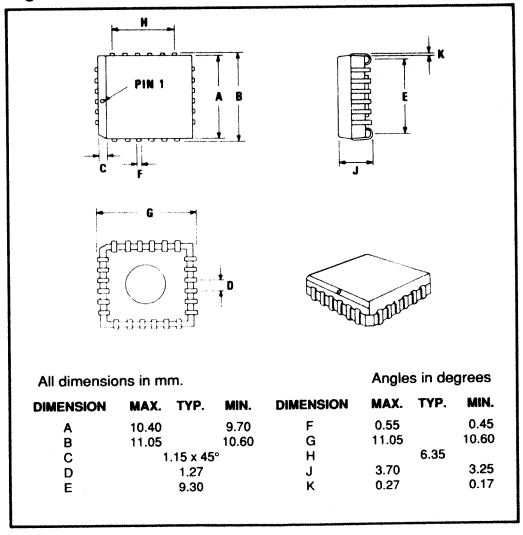
*Fig. 8* **FX304LG** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A } | Datum & Symmetry | |
| B } | | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° TYPICAL | |
| R | 6° TYPICAL | |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 TYPICAL | |
| W | 0.07 | – |

*Fig. 9* **FX304LS** *Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.40 | | 9.70 | F | 0.55 | | 0.45 |
| B | 11.05 | | 10.60 | G | 11.05 | | 10.60 |
| C | 1.15 x 45° | | | H | | 6.35 | |
| D | 1.27 | | | J | 3.70 | | 3.25 |
| E | 9.30 | | | K | 0.27 | | 0.17 |

## Ordering Information

| | |
|---|---|
| **FX304J** | **24-pin cerdip DIL.** |
| **FX304LG** | **24-pin quad plastic encapsulated, bent and cropped.** |
| **FX304LS** | **24-lead plastic leaded chip carrier.** |

# CML Semiconductor Products

PRODUCT INFORMATION

# FX306 Audio Filter Array

Publication D/306/5 June 1987
Provisional Issue

## Features/Applications

- Cellular Radio Audio Processing to NMT TACS AMPS Specification
- Low Group Delay Distortion
- Switched Capacitor Filters
- On-Chip Uncommitted Amplifier
- Xtal Controlled
- Chip Enable Powersave Feature
- Low-Power CMOS Process
- Choice of Package Styles
- Few External Components
- Single 5-Volt Supply

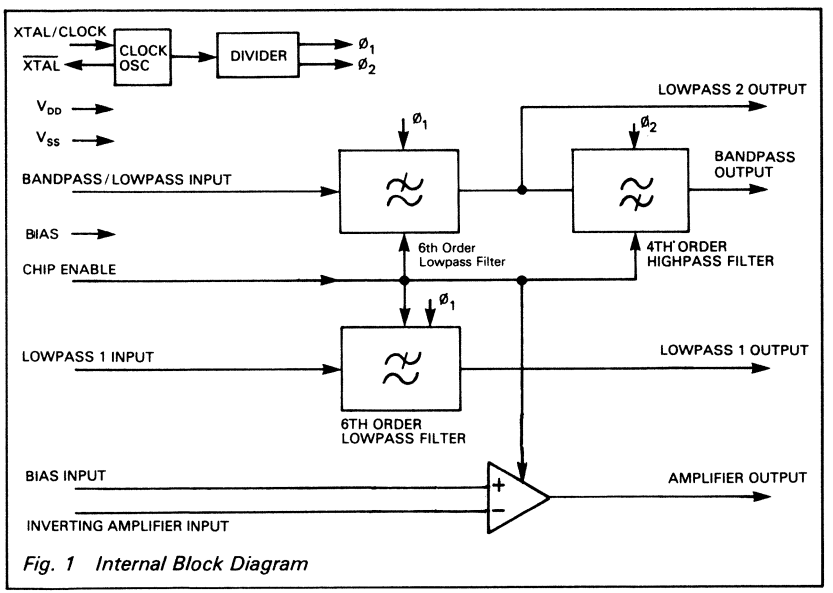



*Fig. 1 Internal Block Diagram*

FX306

## Brief Description

The FX306 is a low-power CMOS switched capacitor filter array designed to meet the NMT TACS and AMPS audio processing specifications. The device consists of:

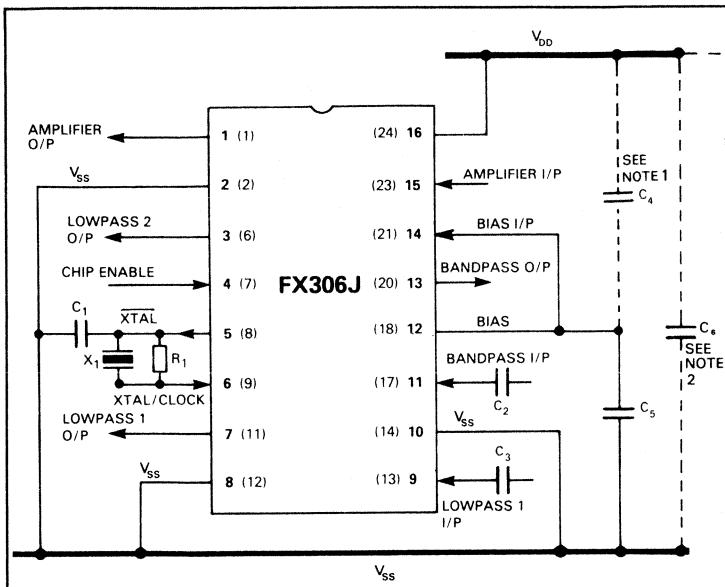
(1) a 3.4 kHz lowpass filter.
(2) a 300 Hz—3.4 kHz bandpass filter (lowpass filter identical to that of (1) in series with a highpass filter).
(3) an uncommitted amplifier.

The two 6th order lowpass filters provide a low group delay distortion path. The amplifier may be used for any specific applications such as, pre-emphasis, de-emphasis, buffering etc. An on-chip oscillator uses a 1 MHz Xtal and provides all reference clocks for the switched capacitor filters via a divider chain. Alternatively an external clock maybe used.

The chip enable feature is used to disable the filter sections and the amplifier, thus reducing current consumption.

| Pin Number | | Function |
|---|---|---|
| FX306J | FX306LG | |
| 1 | 1 | **Amp O/P:**<br>Uncommitted amplifier output. |
| 2 | 2 | **$V_{SS}$:**<br>Negative Supply. |
| 3 | 6 | **LP (2) O/P:**<br>Buffered output from the intermediate lowpass filter (Bandpass arrangement). |
| 4 | 7 | **Chip Enable:**<br>Internally pulled to $V_{DD}$. A logic '0' applied to this input will disable all filters (powersave mode). |
| 5 | 8 | **$\overline{\text{Xtal}}$:**<br>1 MHz Xtal O/P. Inverting output of on-chip oscillator. |
| 6 | 9 | **Xtal/Clock:**<br>1 MHz Xtal I/P or externally derived clock can be injected into this I/P. Input to on-chip inverting oscillator. |
| 7 | 11 | **LP (1) O/P:**<br>Output of separate lowpass filter. |
| 8 | 12 | **$V_{SS}$:**<br>Negative Supply. |
| 9 | 13 | **LP (1) I/P:**<br>Input of separate lowpass filter. |
| 10 | 14 | **$V_{SS}$:**<br>Negative Supply. |
| 11 | 17 | **BP I/P / LP (2) I/P:**<br>Bandpass/lowpass filter (2) input. |
| 12 | 18 | **Bias:**<br>$V_{SS}/2$ Bias Pin. Externally decoupled by $C_4$ and $C_5$. (See Fig 2, Note 1.) |
| 13 | 20 | **BP O/P:**<br>Bandpass filter output. |
| 14 | 21 | **Bias: I/P:**<br>Connect externally to 'Bias' pin. |
| 15 | 23 | **Amp I/P:**<br>Uncommitted inverting amplifier input. |
| 16 | 24 | **$V_{DD}$:**<br>Positive Supply. |

**FX306LG** Pin numbers 3, 4, 5, 10, 15, 16, 19, 22 are not connected.




| Component References | | |
|---|---|---|
| Component | Unit Value | Tolerance |
| $R_1$ | 1M | ± 10% |
| $R_2$ | (See note 3) | |
| $C_1$ | 33p | ± 20% |
| $C_2$ | 0.1μ | |
| $C_3$ | 0.1μ | |
| $C_4$ | 0.1 μ | |
| $C_5$ | 0.1 μ | (See note 1) |
| $C_6$ | (See note 2, 3) | |

**NOTES:**

1. *Bias may be decoupled to $V_{SS}$ and $V_{DD}$ using $C_4$, $C_6$ when input signals are referenced to the bias pin. For input signals referenced to $V_{SS}$, decouple Bias to $V_{SS}$ using $C_6$ only.*
2. *Use $C_6$, when input signals are referenced to $V_{SS}$, to decouple $V_{DD}$.*
3. *Use $R_2$ to assist decoupling of high frequency power supply noise ($R_2$ $C_6$ typically 300μs)*

*Fig.2 External Component Connections*

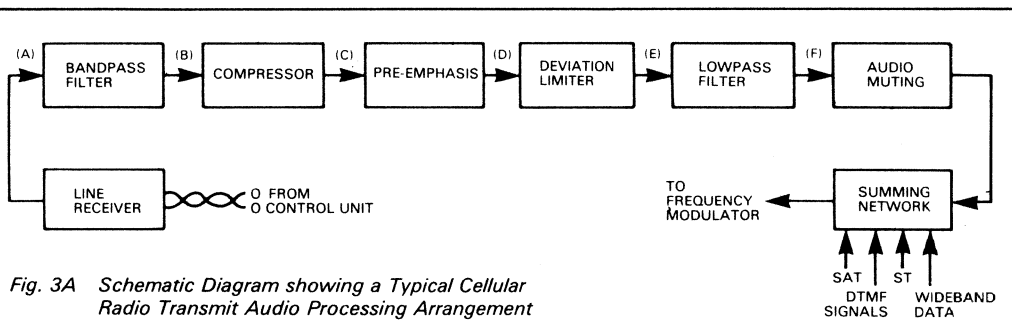



*Fig. 3A Schematic Diagram showing a Typical Cellular Radio Transmit Audio Processing Arrangement*

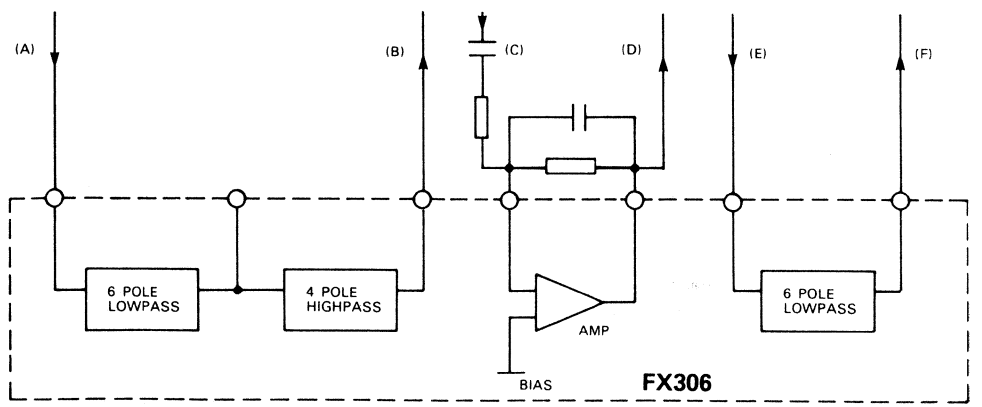



*Fig. 3B The FX306 used in the above application*

# Specification

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX306J | −30°C to + 85°C |
| | FX306LG | −30°C to + 70°C |
| Storage temperature range: | FX306J | −55°C to +125°C |
| | FX306LG | −40°C to +85°C |
| Maximum device dissipation: | | All versions 100mW |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5V, $T_{amb}$ = 25°C, Ø = 1MHz, $\Delta f \phi$ = 0, $f_{in}$ = 1kHz.

| Characteristics | | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| Supply voltage | | | 4.5 | 5 | 5.5 | V |
| Supply current (Enabled) | | | — | 3.5 | | mA |
| Supply current (Disabled) | | | — | 500 | | µA |
| Input impedance (Filters & Amplifier) | | | 100 | | — | kΩ |
| Output impedance (Filters) | | | — | 3 | | kΩ |
| Output impedance (Amplifier open loop) | | | — | 800 | | Ω |
| Output impedance (Amplifier closed loop) | | | — | 6 | | Ω |
| Input logic '1' | | | 3.5 | — | — | V |
| Input logic '0' | | | — | — | 1.5 | V |
| **Dynamic Characteristics** | | | | | | |
| Signal input dynamic range | LP | 1 | | 40 | | dB |
| | BP | 1 | | 40 | | dB |
| Cut off frequency (−3dB) | LP | | | 3400 | | Hz |
| | HP | | | 260 | | Hz |
| Group Delay (900−2100Hz) | LP | | | 30 | 60 | µs |
| | BP | | | 60 | | µs |
| Noise and Distortion | LP | 2 | | 45 | | dB sinad |
| | BP | 2 | | 35 | | dB sinad |
| Passband ripple (400−3000Hz) | | | | | 2 | dB absolute |
| Lowpass attenuation | $f$ > 4kHz | 3 | | 10 | | dB |
| | $f$ > 6kHz | 3 | | 35 | | dB |
| Highpass attenuation | $f$ < 200Hz | 3 | | 15 | | dB |
| Insertion loss $f$ = 1kHz | | | | 0 | | dB |
| **Inverting Amplifier** | | | | | | |
| Open loop gain | | 3 | | 30 | | dB |
| Gain bandwidth product | | | | 1 | | MHz |

**Note:** *1. For 20dB sinad (psophometrically weighted)*
*2. −6dBm input (psophometrically weighted)*
*3. Relative to 1kHz 100mV rms input level*

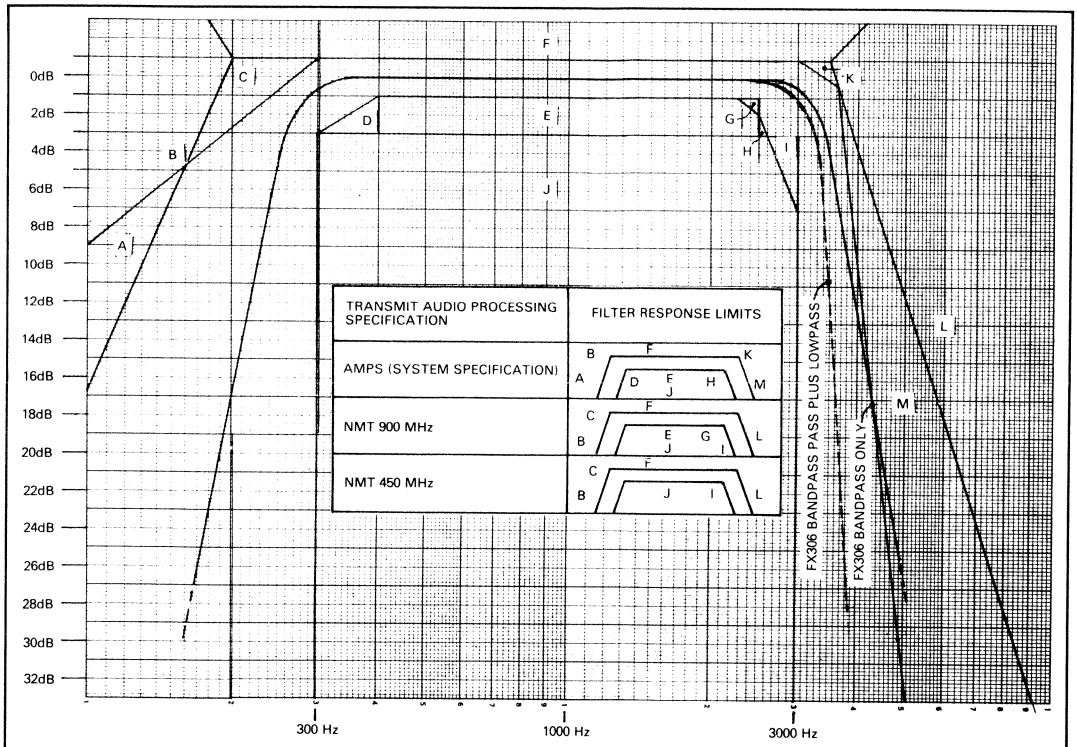



*Fig. 4 FX306 Typical Filter Response Curves*

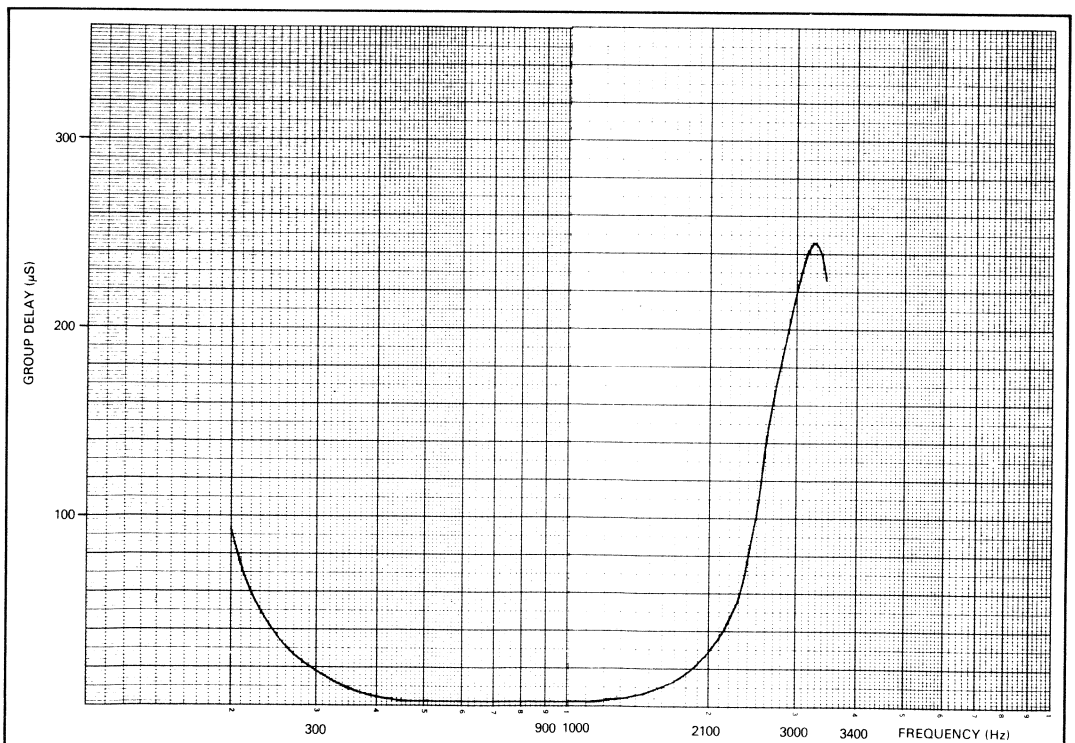



*Fig. 5 FX306 Typical Group Delay Characteristics*

## Package Outlines

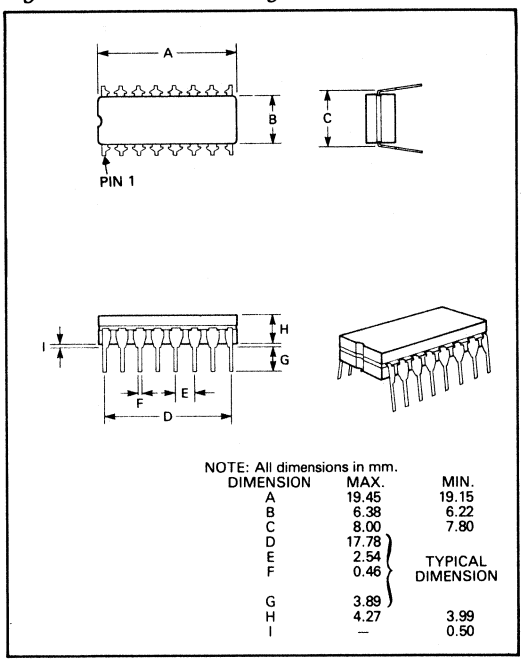
The cerdip package of the FX306J is shown in *Figure 6.* The FX306LG of *Figure 7* is supplied in a conductive tray for handling convenience.

The FX306LG has an indent (spot) adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 to allow complete identification. Pins number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX306J/LG is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

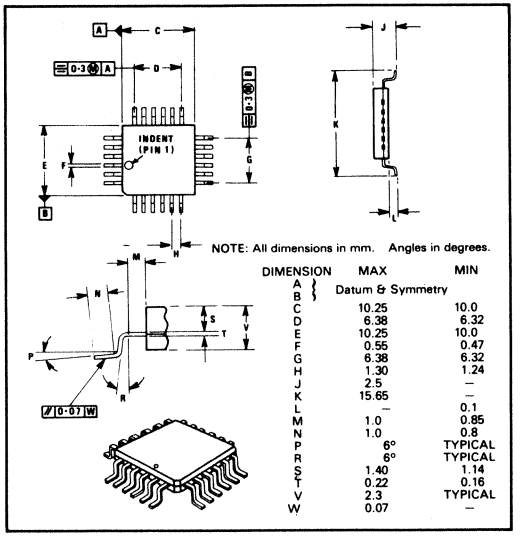
*Fig. 6* **FX306J** *DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.45 | 19.15 |
| B | 6.38 | 6.22 |
| C | 8.00 | 7.80 |
| D | 17.78 | TYPICAL DIMENSION |
| E | 2.54 | |
| F | 0.46 | |
| G | 3.89 | |
| H | 4.27 | 3.99 |
| I | — | 0.50 |

*Fig. 7* **FX306LG** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | — |
| K | 15.65 | — |
| L | — | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | — |

## Ordering Information

**FX306J** **16-pin Cerdip DIL.**

**FX306LG** **24-pin quad plastic encapsulated, bent and cropped.**

**CML Semiconductor Products**
PRODUCT INFORMATION

# FX316 NMT Audio Filter Array

Publication D/316/4 December 1989
Provisional Issue

## Features/Applications

- Cellular Radio Audio Processing
- NMT 450 & 900MHz Base Station and Mobile Specifications
- High Order Lowpass Filter including SAT Rejection
- Low Group Delay Distortion
- 4kHz SAT Recovery Bandpass Filter
- Uncommitted Amplifier
- Switched Capacitor Filters
- Xtal Controlled
- Single 5 Volt CMOS Process
- Chip Enable Powersave Feature
- Few External components
- Surface Mount or DIL Package Style

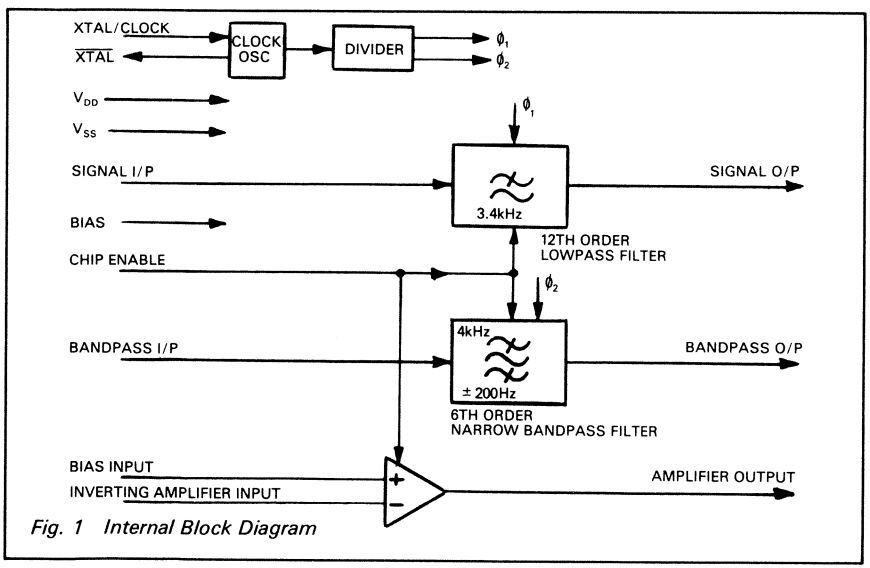



*Fig. 1 Internal Block Diagram*

**FX316**

## Brief Description

The FX316 is a low-power CMOS Switched Capacitor filter array designed to meet NMT Base and Mobile specifications.

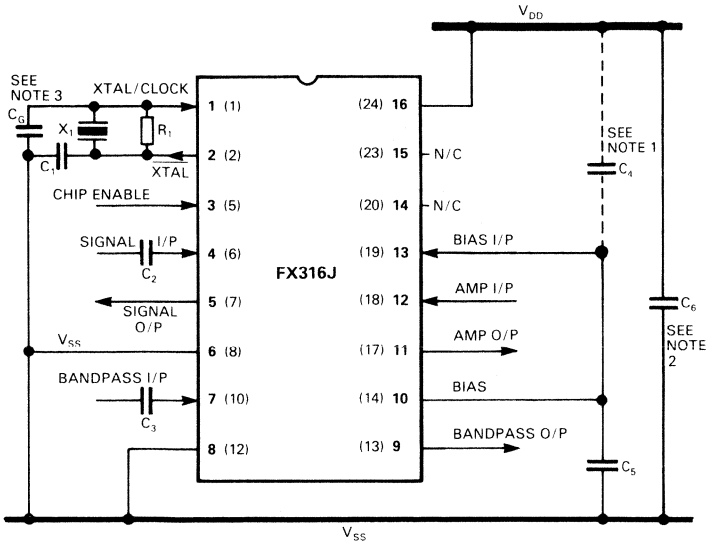
The device in detail consists of:
(1) a 12th order 3.4kHz lowpass filter with sufficient rejection of 4kHz signals to meet NMT 450 and 900 filter response specifications for both base and mobile equipments. The lowpass filter also provides a low group delay distortion path.
(2) a 6th order 4kHz narrow bandpass filter which meets the NMT 450 and 900 mobile specifications for SAT recovery.
(3) an uncommitted amplifier which may be used for any specific applications such as pre-emphasis, de-emphasis, buffering etc. An on chip oscillator uses a 1MHz Xtal and provides all reference clocks for the switched capacitor filters via a divider chain. Alternatively, an external clock may be used. The chip enable feature is used to disable the three circuit elements thus reducing current consumption.

| Pin Number | | | Function |
|---|---|---|---|
| FX316J | FX316LG | FX316LH | |
| 1 | 1 | 1 | **Xtal/Clock:** 1 MHz Xtal I/P or externally derived clock can be injected into this input. Input to on-chip inverting oscillator. |
| 2 | 2 | 2 | **$\overline{\text{Xtal}}$:** 1 MHz Xtal O/P. Inverting output of on-chip oscillator. |
| 3 | 5 | 7 | **Chip Enable:** Internally pulled to $V_{DD}$. A logic '0' applied to this input will disable all filters and the uncommitted amplifier (powersave mode). |
| 4 | 6 | 8 | **Signal I/P:** Input to lowpass filter. This input is internally biased and externally a.c. coupled by $C_2$. |
| 5 | 7 | 10 | **Signal O/P:** Lowpass filter output internally biased to $V_{DD}/2$. |
| 6 | 8 | 11 | $V_{SS}$: Negative supply. |
| 7 | 10 | 13 | **Bandpass I/P:** Input to bandpass filter. This input is internally biased and externally a.c. coupled by $C_3$. |
| 8 | 12 | 15 | $V_{SS}$: Negative supply. |
| 9 | 13 | 16 | **Bandpass O/P:** Bandpass filter output internally biased to $V_{DD}/2$. |
| 10 | 14 | 17 | **Bias:** $V_{DD}/2$ Bias Pin. Externally decoupled by $C_5$. *(See Fig. 2, Note 1).* |
| 11 | 17 | 20 | **Amp O/P:** Uncommitted amplifier output. |
| 12 | 18 | 22 | **Amp I/P:** Uncommitted amplifier inverting input. |
| 13 | 19 | 23 | **Bias I/P:** Connect externally to 'Bias' pin. |
| 14 | 20 | 24 | **No Connection:** Internally connected leave open circuit. |
| 15 | 23 | 27 | **No Connection:** Internally connected leave open circuit. |
| 16 | 24 | 28 | $V_{DD}$: Positive supply. |

**FX316LG:** Pin numbers 3, 4, 9, 11, 15, 16, 21 and 22 are not connected.

**FX316LH** Pin numbers 3, 4, 5, 6, 9, 12, 14, 18, 19, 21, 25 and 26 are not connected.

**Note: Output Loading.**
Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of typically <100Ω put in series with the load should minimise this effect.




(FX316LG SHOWN IN BRACKETS. N/C = NO CONNECTIONS)

## Component References

| Component | Typical Unit Value | |
|---|---|---|
| $R_1$ | 1M | 10%* |
| $C_1$ | 33p | 20%* |
| $C_2$ | 0.1µ | 20% |
| $C_3$ | 0.1µ | 20% |
| $C_4$ | 0.1µ | 20% |
| $C_5$ | 0.1µ Min. | 20% |
| $C_6$ | 0.1µ | 20% |
| $C_G$ | 68p | 20%* |
| $X_1$ | 1MHz* | |
| * | See Note 3 | |

**NOTES:**

1. *Bias may be decoupled to $V_{SS}$ and $V_{DD}$ using $C_4$. $C_5$ when input signals are referenced to the bias pin. For input signals referenced to $V_{SS}$, decouple Bias to $V_{SS}$ using $C_5$ only.*
2. *Use $C_6$, when input signals are referenced to $V_{SS}$, to decouple $V_{DD}$.*
3. *Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986.*

*Fig. 2 External Component Connections*

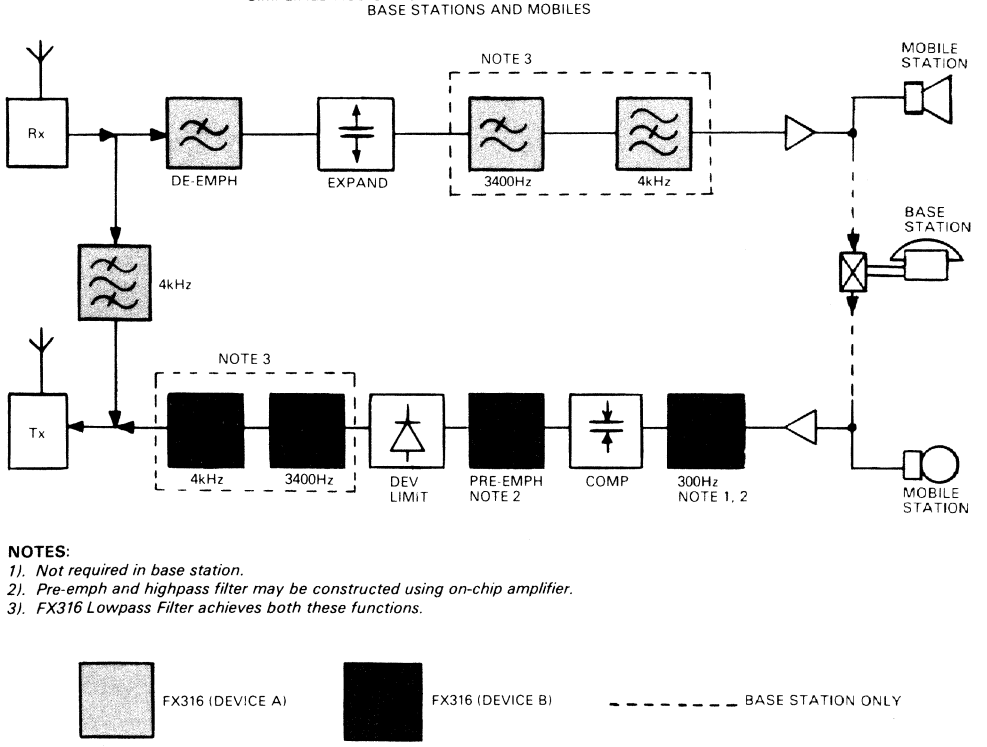



*Fig. 3 FX316 Typical Application*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX316J | −30°C to + 85°C |
| | FX316LG/LH | −30°C to + 70°C |
| Storage temperature range: | FX316J | −55°C to +125°C |
| | FX316LG/LH | −40°C to + 85°C |
| Maximum device dissipation: | | All versions 100mW |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5V, $T_{amb}$ = 25°C, $\phi$ = 1MHz, $\Delta f_{\phi}$ = 0, $f_{in}$ = 1kHz.

| Characteristics | | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| Supply voltage | | | 4.5 | 5 | 5.5 | V |
| Supply current (Enabled) | | | — | 6.0 | — | mA |
| Supply current (Disabled) | | | — | 700 | — | μA |
| Input impedance (Filters & Amplifier) | | | 100 | 1000 | — | kΩ |
| Output impedance (Filters) | | | — | 3 | — | kΩ |
| Output impedance (Amplifier open loop) | | | — | 800 | — | Ω |
| Output impedance (Amplifier closed loop) | | | — | 6 | — | Ω |
| Input logic '1' | | | 3.5 | — | — | V |
| Input logic '0' | | | — | — | 1.5 | V |
| **Dynamic Characteristics** | | | | | | |
| Passband Ripple | (300-3000Hz) LP | 5 | — | — | 2 | dB |
| | (4kHz±55Hz) BP | 5 | — | — | 2 | dB |
| Cut-off Frequency | (−3dB) LP | 4, 5 | 3000 | 3450 | 3800 | Hz |
| | (−6dB) BP | 4, 5 | 4200 | — | 3800 | Hz |
| Attenuation | (3800−4200Hz) LP | 4, 5 | 36 | 46 | — | dB |
| | (<2000Hz,>6000Hz) BP | 4, 5 | 35 | 37 | — | dB |
| Group Delay Distortion | (900-2100Hz) LP | | — | 80 | — | μs |
| | (600-3000Hz) LP | | — | 450 | — | μs |
| Output Noise (rms) | LP | 1 | — | 1.6 | — | mV |
| | BP | 1 | — | 1 | — | mV |
| Signal Input (rms) | LP | 2 | — | 0.4 | 1.0 | V |
| | BP | 2 | — | 0.4 | 1.0 | V |
| Insertion loss (1kHz) | LP | | — | 0 | — | dB |
| (4kHz) | BP | | — | 0 | — | dB |
| Aliasing Frequency | | | 50 | — | — | kHz |
| **Inverting Amplifier** | | | | | | |
| Open loop gain | | 3 | — | 30 | — | dB |
| Gain bandwidth product | | | — | 1 | — | MHz |

**Notes:** *1. Measured with input a.c. s/c.*
*2. 'MAX' figure specified for nominal 3% distortion (30dB SINAD).*
*'TYP' figure specified for minimum distortion (MAX SINAD).*
*3. Relative to 1kHz 100mV rms input level.*
*4. Refer to Figs. 4 and 5.*
*5. Specified over the full operating voltage and temperature range.*

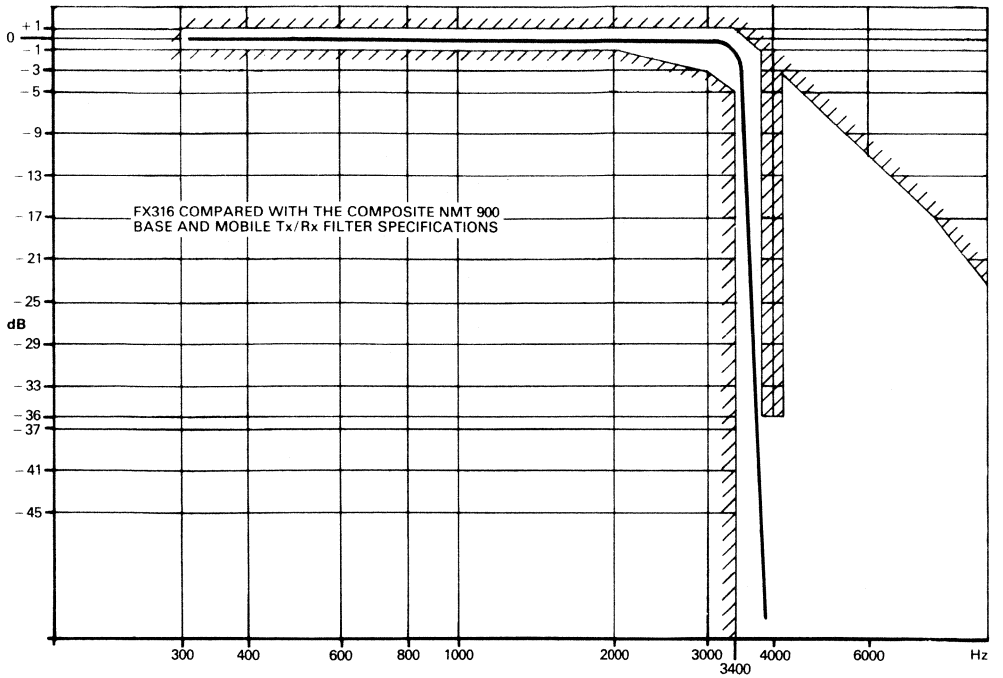



*Fig. 4 Typical FX316 Lowpass Filter Response*

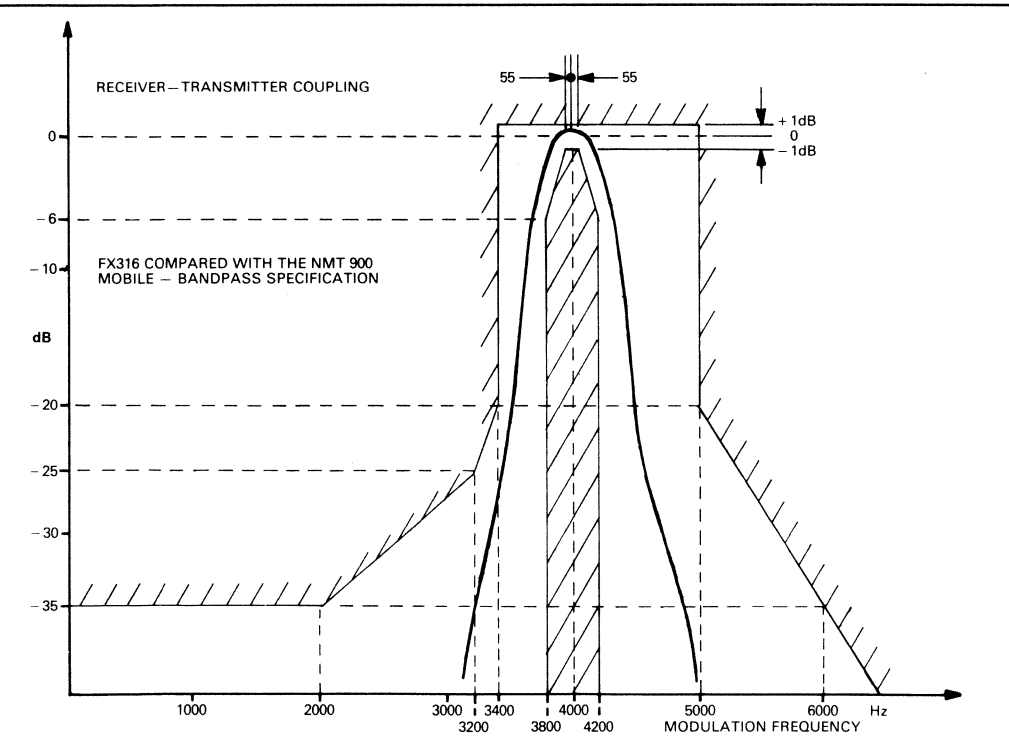
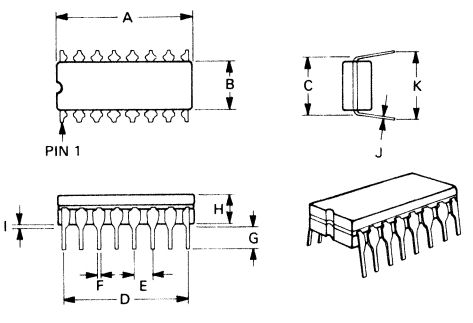



*Fig. 5 Typical FX316 4kHz Bandpass Filter Response*

## Package Outlines

The FX316J, the cerdip package is illustrated in *Figure 6.* The 'LG' version is shown in *Figure 7* and the 'LH' version in *Figure 8.* The 'LG' and 'LH' packages are supplied in conductive trays for handling convenience. To allow complete identification, the FX316LG and LH packages have an indent spot adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 for LG package, between Pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 6* **FX316J** *DIL Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 19.48 | 19.12 |
| B | 7.40 | 7.24 |
| C | 8.00 | 7.80 |
| D | 17.78 | TYPICAL |
| E | 2.54 | |
| F | 0.46 | |
| G | 4.30 | 4.10 |
| H | 4.27 | TYPICAL |
| I | 1.40 | |
| J | 0.25 | |
| K | 9.45 | 8.45 |

## Ordering Information

**FX316J** **16-pin cerdip DIL**

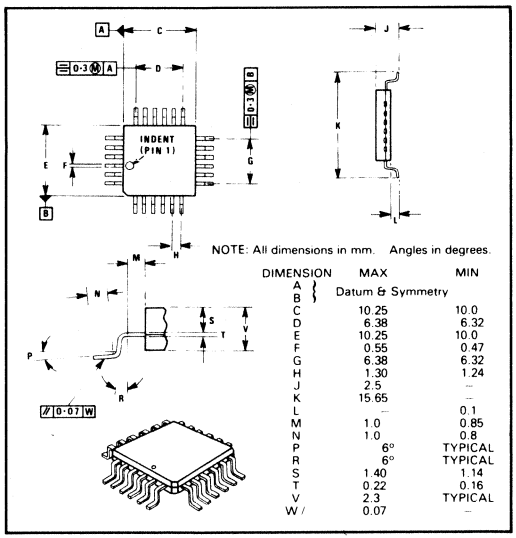
**FX316LG** **24-pin quad plastic encapsulated, bent and cropped.**

**FX316LH** **28-lead plastic leaded chip carrier.**

## Handling Precautions

The FX316J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

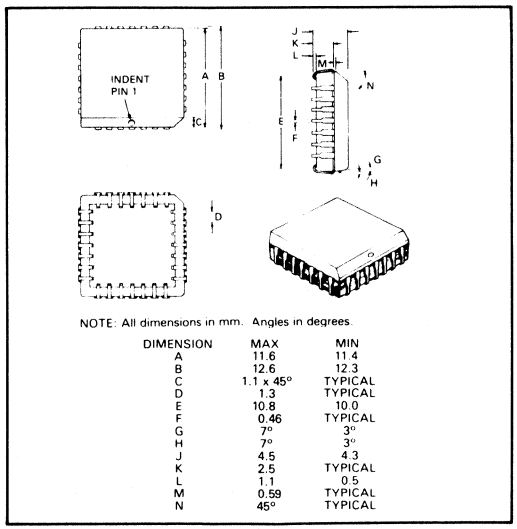
*Fig. 7* **FX316LG** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig. 8* **FX316LH** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 11.6 | 11.4 |
| B | 12.6 | 12.3 |
| C | 1.1 x 45° | TYPICAL |
| D | 1.3 | TYPICAL |
| E | 10.8 | 10.0 |
| F | 0.46 | TYPICAL |
| G | 7° | 3° |
| H | 7° | 3° |
| J | 4.5 | 4.3 |
| K | 2.5 | TYPICAL |
| L | 1.1 | 0.5 |
| M | 0.59 | TYPICAL |
| N | 45° | TYPICAL |

# CML Semiconductor Products

PRODUCT INFORMATION

# FX336 R2000 Filter Array

Publication D/336/2 November 1986
Provisional Issue

## Features/Applications

- R2000 Trunked Radio Audio Processing
- High Order 300Hz Highpass Filter
- Low Group Delay 2550Hz Lowpass Filter
- On-Chip 120 – 175Hz Bandpass
- Uncommitted Amplifier and Analogue Switch
- Typical 43dB Rejection Below 170 Hz
- Switched Capacitor Filters
- Xtal Controlled
- Single 5 Volt CMOS Process
- Chip Enable Powersave Feature
- Surface Mount or DIL Package Styles

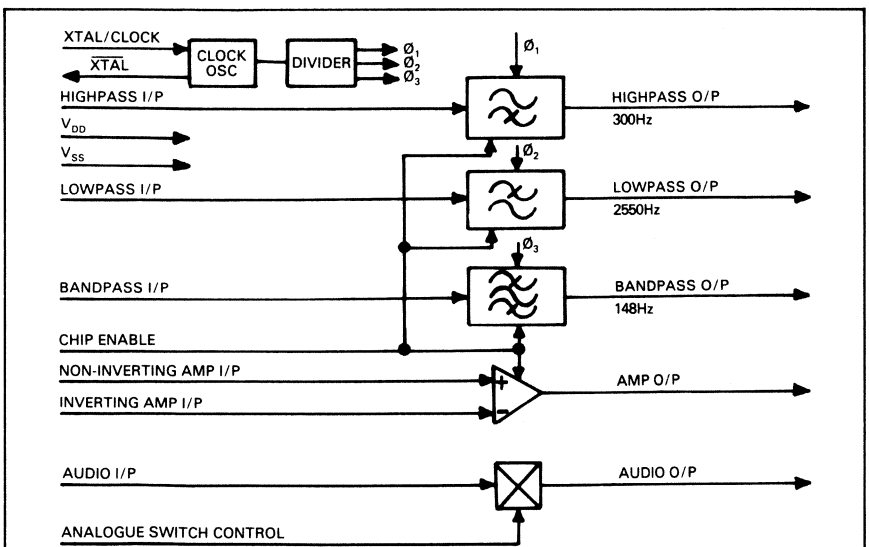



*Fig. 1 Internal Block Diagram*

FX336

## Brief Description

The device is a single chip CMOS filter array used to process speech and 50 baud FSK signals as specified in the Radiocom 2000 system specification. The device consists of:

(a) Highpass audio filter with typically 43dB attenuation of signals below 170 Hz.

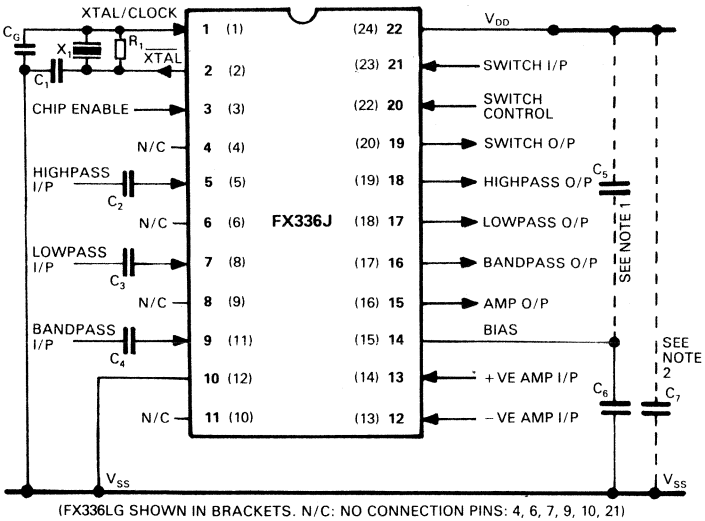
(b) Lowpass audio filter for band-limiting speech in 12.5 kHz channel spacing radios. The group delay of this lowpass filter is controlled over the range 900 – 2100Hz, hence allowing the filter to pass 1200 Baud FFSK data.

(c) Narrow bandpass filter for processing 50 baud FSK data.

(d) Uncommitted audio amplifier.

(e) Mute switch with external control.

| Pin Number | | | Function |
|---|---|---|---|
| FX336J | FX336LG | FX336LH | |
| 1 | 1 | 1 | **Xtal/Clock:** This is the input to the clock oscillator inverter. 1MHz xtal input or externally derived clock can be injected into this input. |
| 2 | 2 | 2 | **$\overline{\text{Xtal}}$:** Output of clock oscillator inverter. |
| 3 | 3 | 3 | **Chip Enable:** This input has an internal 1MΩ pull up resistor to $V_{DD}$. When pulled to $V_{SS}$ (logic '0') all internal amplifiers are disabled and current consumption is reduced. |
| 4 | 4 | 4, 5 | **No Connection.** |
| 5 | 5 | 6 | **Highpass I/P:** Input to highpass filter. |
| 6 | 6, 7 | 7, 8 | **No Connection.** |
| 7 | 8 | 9 | **Lowpass I/P:** Input to lowpass filter. |
| 8 | 9, 10 | 10, 11, 12 | **No Connection.** |
| 9 | 11 | 13 | **Bandpass I/P:** Input to narrow bandpass filter. |
| 10 | 12 | 14 | **$V_{SS}$:** Negative supply. |
| 11 | — | 15 | **No Connection.** |
| 12 | 13 | 16 | **Amp Negative:** Inverting input of uncommitted amplifier. |
| 13 | 14 | 17 | **Amp Positive:** Non-inverting input of uncommitted amplifier. |
| 14 | 15 | 18 | **Bias:** This is the bias or analogue ground pin and is set internally at $V_{DD}/2$. It should be decoupled to $V_{SS}$ by an externally connected 1.0μF (min). |
| — | — | 19 | **No Connection.** |
| 15 | 16 | 20 | **Amp O/P:** Output of uncommitted amplifier. |
| 16 | 17 | 21 | **Bandpass O/P:** Output of narrow bandpass filter. |
| 17 | 18 | 22 | **Lowpass O/P:** Output of lowpass filter. |
| 18 | 19 | 23 | **Highpass O/P:** Output of highpass filter. |
| 19 | 20 | 24 | **Switch O/P:** Output of analogue switch. This output is internally biased to approximately $V_{DD}/2$. |
| — | 21 | 25 | **No connection.** |
| 20 | 22 | 26 | **Switch Control:** Control input of analogue switch, internally pulled to $V_{DD}$ by 1MΩ resistor with switch in 'closed' position. When this input is pulled to $V_{SS}$ the switch is in 'open' position. |
| 21 | 23 | 27 | **Switch I/P:** Input of analogue switch. |
| 22 | 24 | 28 | **$V_{DD}$:** Positive supply. |
| | | | **Note: Output Loading.**<br>Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of typically <100Ω put in series with the load should minimise this effect. |




(FX336LG SHOWN IN BRACKETS. N/C: NO CONNECTION PINS: 4, 6, 7, 9, 10, 21)

**Component References**

| Component | Typical Unit Value | |
|---|---|---|
| $R_1$ | 1MΩ | Note 3 |
| $C_1$ | 33p | |
| $C_2$ | 0.1μ | |
| $C_3$ | 0.1μ | |
| $C_4$ | 0.1μ | |
| $C_5$ | 0.1μ | Note 1 |
| $C_6$ | 1.0μ Min. | Note 1 |
| $C_7$ | 0.1μ Min. | Note 3 |
| $C_G$ | 47p | Note 3 |
| $X_1$ | 1MHz | Note 3 |
| R = ±10% | C = ±20% | |

**NOTES:**

1. *Bias may be decoupled to $V_{SS}$ and $V_{DD}$ using $C_5$, $C_6$ when input signals are referenced to the bias pin. For input signals referenced to $V_{SS}$, decouple Bias to $V_{SS}$ using $C_6$ only.*
2. *Use $C_7$, when input signals are referenced to $V_{SS}$, to decouple $V_{DD}$.*
3. *Xtal circuitry shown is in accordance with CML application note D/XT/I April 1986.*

*Fig. 2 External Component Connections*

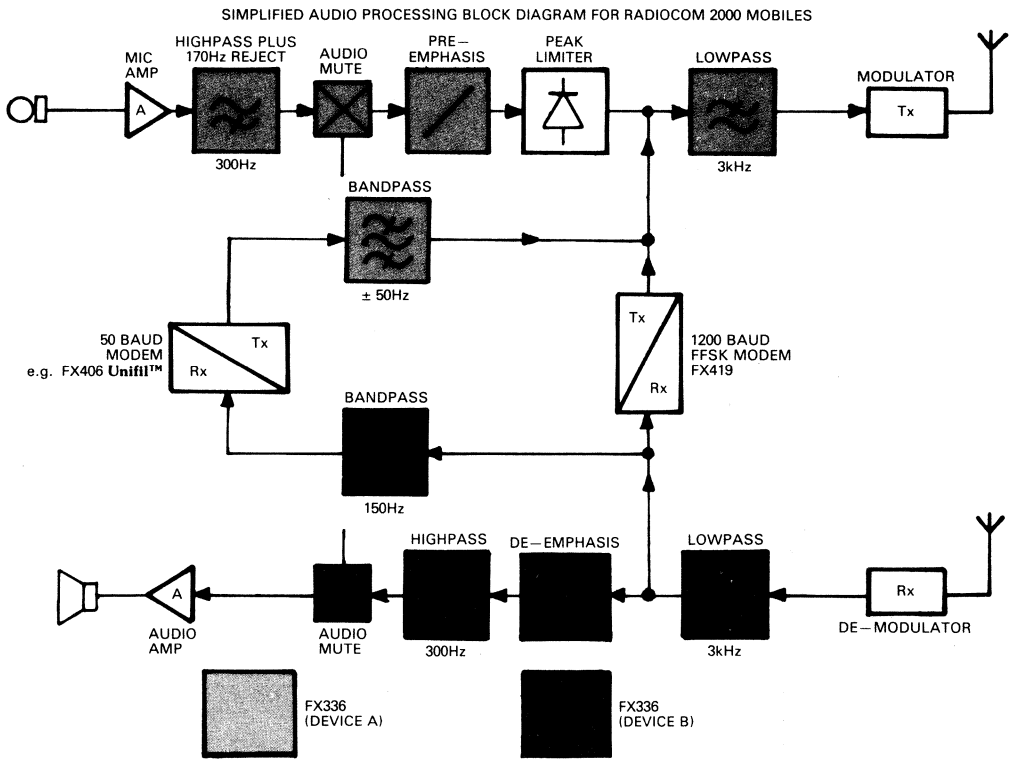



*Fig. 3 FX336 Typical Application*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX336J | −30°C to + 85°C |
| | FX336LG/LH | −30°C to + 70°C |
| Storage temperature range: | FX336J | −55°C to +125°C |
| | FX336LG/LH | −40°C to + 85°C |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5V, $T_{amb}$ = 25°C, Ø = 1MHz, $\Delta f_O$ = 0, $f_{in}$ = 1kHz, $V_{in}$ = 1.0 V(rms)

| Characteristics | | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| Supply voltage | | | 4.5 | 5 | 5.5 | V |
| Supply current (Enabled) | | | — | 6.8 | — | mA |
| Supply current (Disabled) | | | — | 600 | — | µA |
| Input impedance (Filters & Amplifier) | | | 100 | 800 | — | kΩ |
| Output impedance (Filters & Amplifier) | | | — | 1.0 | — | kΩ |
| Input logic '1' | | | 70%$V_{DD}$ | — | — | V |
| Input logic '0' | | | — | — | 30%$V_{DD}$ | V |
| **Dynamic Characteristics** | | | | | | |
| Passband Ripple | (300-2550Hz) | HP + LP 1 | — | — | 2 | dB |
| | (280-300Hz) | HP + LP 2 | +1 | 0 | −2 | dB |
| | (120−175Hz) | BP 2 | — | — | 3 | dB |
| Cut-off Frequency | (−3dB) | HP | — | 265 | — | Hz |
| | (−3dB) | LP | — | 3800 | — | Hz |
| | (−6dB)>150Hz | BP | — | 190 | — | Hz |
| | (−6dB)<150Hz | BP | — | 115 | — | Hz |
| Stopband Attenuation | <170Hz | HP | 40 | 43 | — | dB |
| | >9000Hz | LP | 40 | 47 | — | dB |
| | <65Hz>290Hz | BP | 30 | 40 | — | dB |
| Group Delay Distortion | (900-2100Hz) | LP | — | 30 | 60 | µs |
| | (900-2100Hz) | HP + LP | — | 300 | — | µs |
| | (136-164Hz) | BP 3 | — | 1.7 | — | ms |
| Output Noise | | LP 4 | — | 2.0 | — | mV(rms) |
| | | HP 4 | — | 2.0 | — | mV(rms) |
| | | BP 4 | — | 2.0 | — | mV(rms) |
| Signal Input | | LP 5 | — | 0.5 | 1.0 | V(rms) |
| | | HP 5 | — | 0.5 | 1.0 | V(rms) |
| | | BP 5 | — | 0.5 | 1.0 | V(rms) |
| Passband Gain | (1kHz) | HP + LP | −0.5 | +0.5 | +1.5 | dB |
| | (150Hz) | BP | −1 | 0 | +1 | dB |
| Aliasing Frequency | | | 50 | — | — | kHz |
| **Audio Switch** | | | | | | |
| Output Noise | (rms) | 4 | — | — | 1 | mV |
| Channel Resistance | (on) | | — | 500 | — | kΩ |
| Channel Resistance | (off) | | 10 | — | — | MΩ |
| **Uncommitted Amplifier** | | | | | | |
| Open loop gain | | | 35 | 50 | — | dB |
| Bandwidth | | | — | 200 | — | kHz |

**Notes:** 1. *Absolute ripple—see Fig. 4.*
2. *Absolute ripple—see Fig. 5.*
3. *Relative delay between 136 and 164Hz.*
4. *Measured with input a.c. s/c; at 30kHz Bw.*
5. *'MAX' figure specified for nominal 3% distortion (30dB).*
*'TYP' figure specified for minimum distortion (MAX SINAD).*

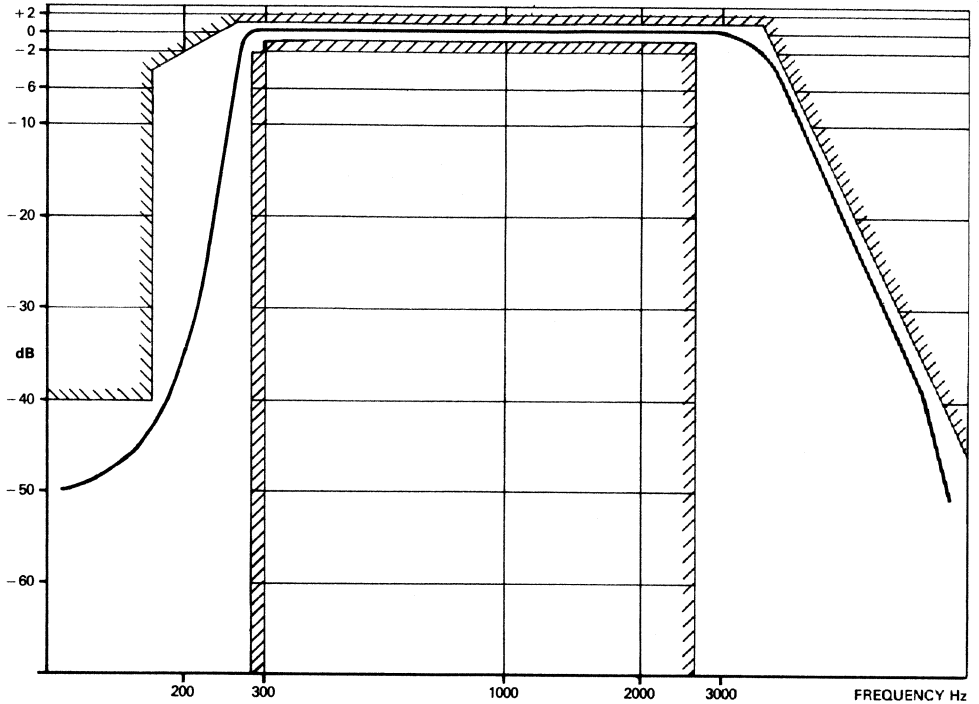



*Fig. 4 Typical audio bandpass filter frequency response versus R2000 filter specification.*

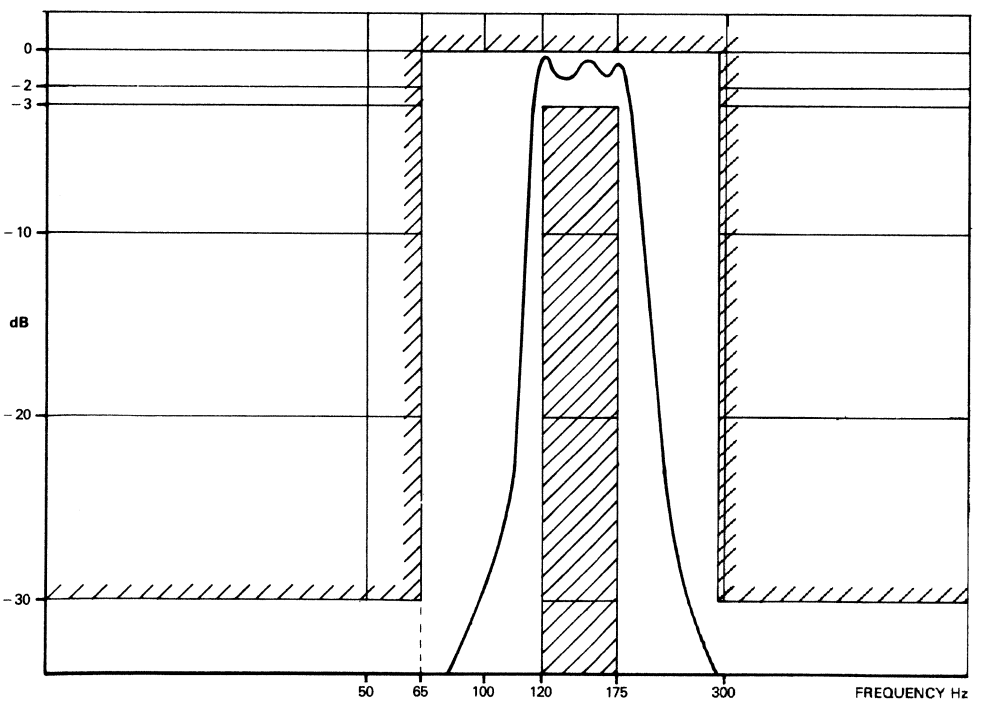
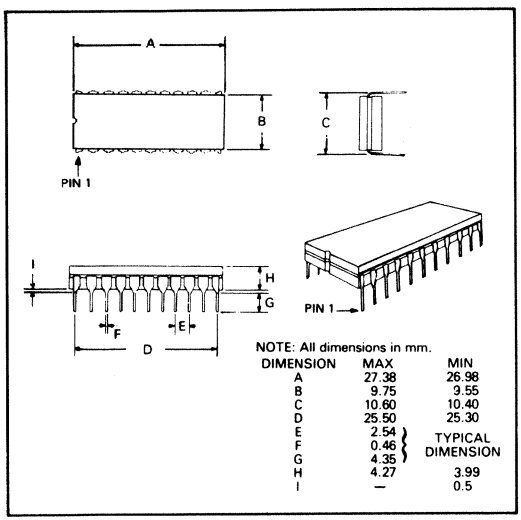



*Fig. 5 Typical data bandpass filter frequency response versus R2000 filter specification.*

## Package Outlines

The FX336J, the cerdip package is illustrated in *Figure 6.* The 'LG' version is shown in *Figure 7* and the 'LH' version in *Figure 8.* Both 'LG' and 'LH' packages are supplied in conductive trays for handling convenience. To allow complete identification, the FX336LG and LH packages have an indent spot adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 for LG package, between Pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 6* **FX336J** *DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 | TYPICAL |
| F | 0.46 | DIMENSION |
| G | 4.35 | |
| H | 4.27 | 3.99 |
| I | — | 0.5 |

## Ordering Information

**FX336J** 22-pin cerdip D I L

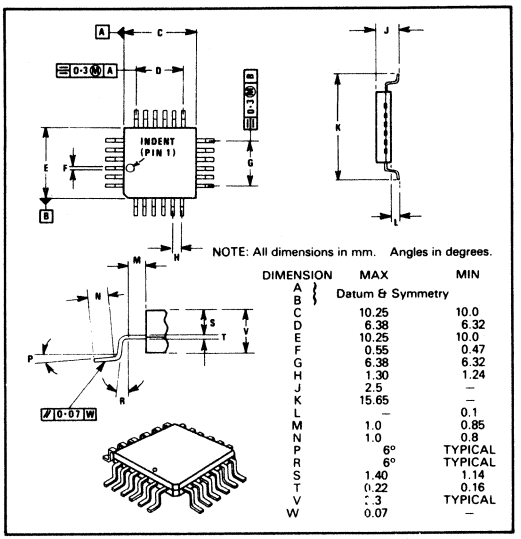
**FX336LG** 24-pin quad plastic encapsulated, bent and cropped

**FX336LH** 28-lead plastic leaded chip carrier

## Handling Precautions

The FX336J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

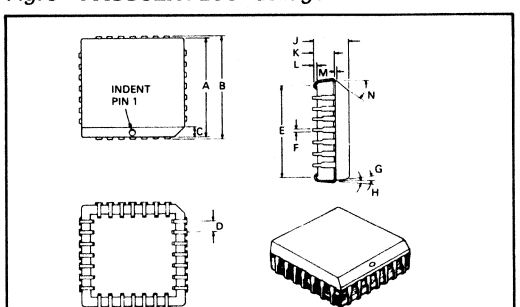
*Fig. 7* **FX336LG** *Quad Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | — |
| K | 15.65 | — |
| L | — | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 3 | TYPICAL |
| W | 0.07 | — |

*Fig. 8* **FX336LH** *PLCC Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 11.6 | 11.4 |
| B | 12.6 | 12.3 |
| C | 1.1 x 45° | TYPICAL |
| D | 1.3 | TYPICAL |
| E | 10.8 | 10.0 |
| F | 0.46 | TYPICAL |
| G | 7° | 3° |
| H | 7° | 3° |
| J | 4.5 | 4.3 |
| K | 2.5 | TYPICAL |
| L | 1.1 | 0.5 |
| M | 0.59 | TYPICAL |
| N | 45° | TYPICAL |

# CML Semiconductor Products

PRODUCT INFORMATION

# FX346 AMPS, TACS, NMT Audio Processing Array

Publication D/346/4 December 1991
Provisional Issue

## Features/Applications

- AMPS, TACS, NMT Audio + Data Processing
- Speech, SAT and Data – Full Duplex Filtering
- Speech Bandpass and Deviation Limiter Filters
- SAT 4/6kHz Bandpass Filters
- 8/10kbit Rx Wideband Data Filter and Limiter
- Filters for Speech/FFSK, Pre/De-emphasis
- Input Gain Adjustment

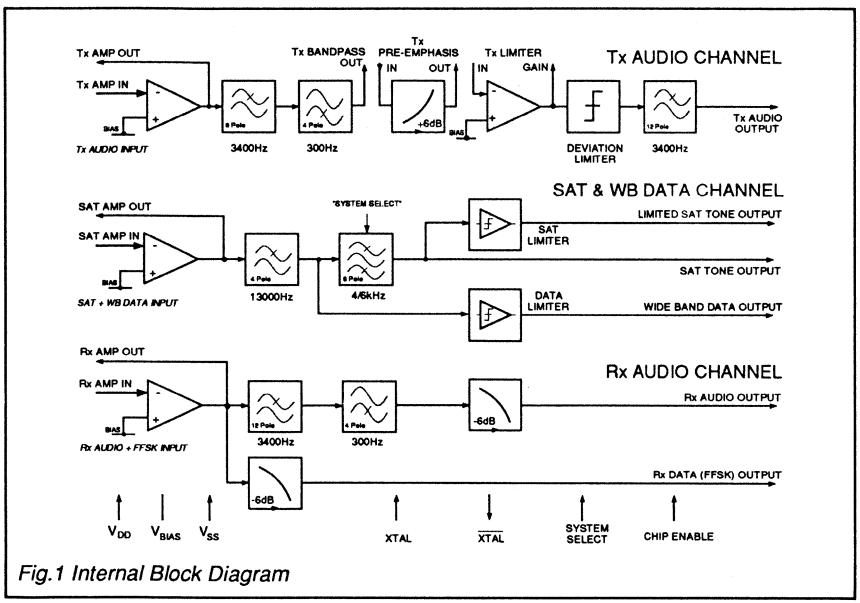



*Fig.1 Internal Block Diagram*

**FX346**

## Brief Description

The FX346 Audio Processing Array is a full-duplex Speech, SAT and Data Processor designed to meet the composite specifications of AMPS, TACS and NMT 450/900.

The product in detail :

**The Rx Audio Path** consisting:

(i) A 12th order lowpass filter.
(ii) A 4th order highpass filter.
(iii) Input gain adjustment and de-emphasis.

**The Tx Audio Path** consisting:

(i) Separate 6th and 12th order lowpass filters.
(ii) A 4th order highpass filter.
(iii) A linear deviation limiter.
(iv) Input gain adjustment and pre-emphasis.

**The Rx SAT and Data Path** consisting:

(i) A 13kHz wideband data filter and limiter.
(ii) Switchable 6th order 4/6kHz SAT bandpass filter.
(iii) 1200 baud FFSK signal data limiter on chip.

All filter stages, excluding the Rx data paths, may be de-powered for minimum current drain.
Operation in AMPS/TACS or NMT mode is controlled via a single logic input.
The FX346, in combination with the *FX009 Digitally Controlled Amplifier Array* and analogue switches offers a complete speech and processing solution for cellular radio. All filter sampling clocks are generated on-chip using an external 4.0MHz Xtal or clock pulse input. The FX346 is a low-power, single 5-volt device available in 24-pin cerdip DIL or SMD plastic packages.

| Pin Number | | Function |
|---|---|---|
| DIL FX346J | Quad FX346LG/LS | |
| 1 | 1 | **Xtal/Clock :** The input to the clock oscillator circuitry. The clock oscillator components are on-chip and require only a single 4MHz Xtal or clock pulse input. Clock oscillations are maintained in "powersave" (Chip Enable = "0"). See Figure 2. |
| 2 | 2 | **$\overline{\text{Xtal}}$ :** The output of the clock oscillator circuitry. See Figure 2. |
| 3 | 3 | **Chip Enable :** The Chip Enable logic input. When a logic "0" the chip is put into a powersave mode, with only the minimum amount of monitoring circuitry enabled, to reduce current consumption. A logic "1" will enable all circuitry. This input operates in conjunction with the System Select input, signal paths are as shown in Table 1. |
| 4 | 4 | **System Select :** A logic input to select signal paths to either the AMPS/TACS or NMT specification. This input operates in conjunction with the Chip Enable input, signal paths are as shown in Table 1. Logic "1" = AMPS/TACS, logic "0" = NMT. |
| 5 | 5 | **Tx Amp Out :** The "gain output" pin of the Transmit Audio Channel audio input amplifier. This output, together with the Tx Amp In pin is used, with external components, to set the required input gain/attenuation of this channel. See Figures 1 and 2. |
| 6 | 6 | **Tx Amp In :** The input pin to the Transmit Audio Channel. This inverting input, together with the Tx Amp Out pin is used, with external components, to set the required input gain/attenuation of the channel. See Figures 1 and 2. |
| 7 | 7 | **$V_{BIAS}$ :** The output of the on-chip analogue bias circuitry, internally set to $V_{DD}/2$ this pin requires to be decoupled to $V_{SS}$ with a capacitor, $C_1$. $V_{BIAS}$ is maintained during "powersave" (Chip Enable = "0"). See Figure 2 and Table 1. |
| 8 | 8 | **SAT Amp In :** The input to the Supervisory Audio Tone (SAT) and Wideband Data Channel. This inverting input, together with the SAT Amp Out pin is used, with external components, to set the required input gain/attenuation of the channel. See Figures 1 and 2. |
| 9 | 9 | **SAT Amp Out :** The "gain output" pin of the Supervisory Audio Tone (SAT) and Wideband Data Channel. This pin, together with the SAT Amp In pin is used, with external components, to set the required input gain/attenuation of the channel. Attention is drawn to the data circuit sensitivity (Specification page). See Figures 1 and 2. |
| 10 | 10 | **Rx Amp Out :** The "gain output" pin of the Receive Audio Channel. This pin, together with the Rx Amp In pin is used, with external components, to set the required input gain/attenuation of the channel. See Figures 1 and 2. |
| 11 | 11 | **Rx Amp In :** The input to the Receive Audio Channel. This inverting input, together with the Rx Amp Out pin is used, with external components, to set the required input gain/attenuation of the channel. See Figures 1 and 2. |

| Pin Number | | Function |
|---|---|---|
| DIL FX346J | Quad FX346LG/LS | |
| 12 | 12 | $V_{SS}$ : Negative supply rail (GND). |
| 13 | 13 | **SAT Tone Out :** The filtered Supervisory Audio Tone (SAT) output. AMPS/TACS (-6dB) = 6kHz ± 200Hz. NMT (-6dB) = 4kHz ± 200Hz. |
| 14 | 14 | **Rx Wideband Data Out :** The filtered, limited, wideband data output. This data channel produces a limited rectangular wave output. Attention is drawn to the data circuit sensitivity ( Specification page). See Figures 1 and 2. |
| 15 | 15 | **Limited SAT Tone Out :** The filtered, limited Supervisory Audio Tone (SAT). Attention is drawn to the data circuit sensitivity ( Specification page). See Figures 1 and 2. |
| 16 | 16 | **Rx Audio Out :** The bandpass filtered, de-emphasized audio output of the Rx Audio Channel. |
| 17 | 17 | **Rx Data Out :** The de-emphasized, received data output. This data process may require filtering by low group delay filters before demodulation by modems such as : *CML – FX419, FX429, FX439.* |
| 18 | 18 | **Tx Audio Out :** The processed audio to the transmission mixing and modulation circuitry. |
| 19 | 19 | **Tx Limiter Gain :** The "gain output" of the Tx Limiter Amplifier. This amplifier, using gain setting components, is used to produce the correct signal level for application to the Deviation Limiter. For limiter levels refer to the Specification page 6. Recommended circuitry is shown in Figure 2. |
| 20 | 20 | **Tx Limiter In :** The input to the Tx Limiter Amplifier. This input should be connected via external components to the Tx Pre-emphasis Out pin as shown in Figure 2. |
| 21 | 21 | **Tx Pre-emphasis Out :** The output of the on-chip +6dB/octave pre-emphasis circuitry. This output should be connected to the Tx Limiter Amplifier via external components as shown in Figure 2. |
| 22 | 22 | **Tx Pre-emphasis In :** The input to the on-chip transmitter pre-emphasis circuitry. This input would normally be connected to the output of an external audio compressor circuit. |
| 23 | 23 | **Tx Bandpass Out :** The output of the first stage of bandpass filtering in the Transmit Audio Channel. This output will normally be connected to the input of an external audio compressor circuit. See Figures 1 and 2. |
| 24 | 24 | $V_{DD}$ : Positive supply rail. A single +5-volt power supply is required. |

## External Components

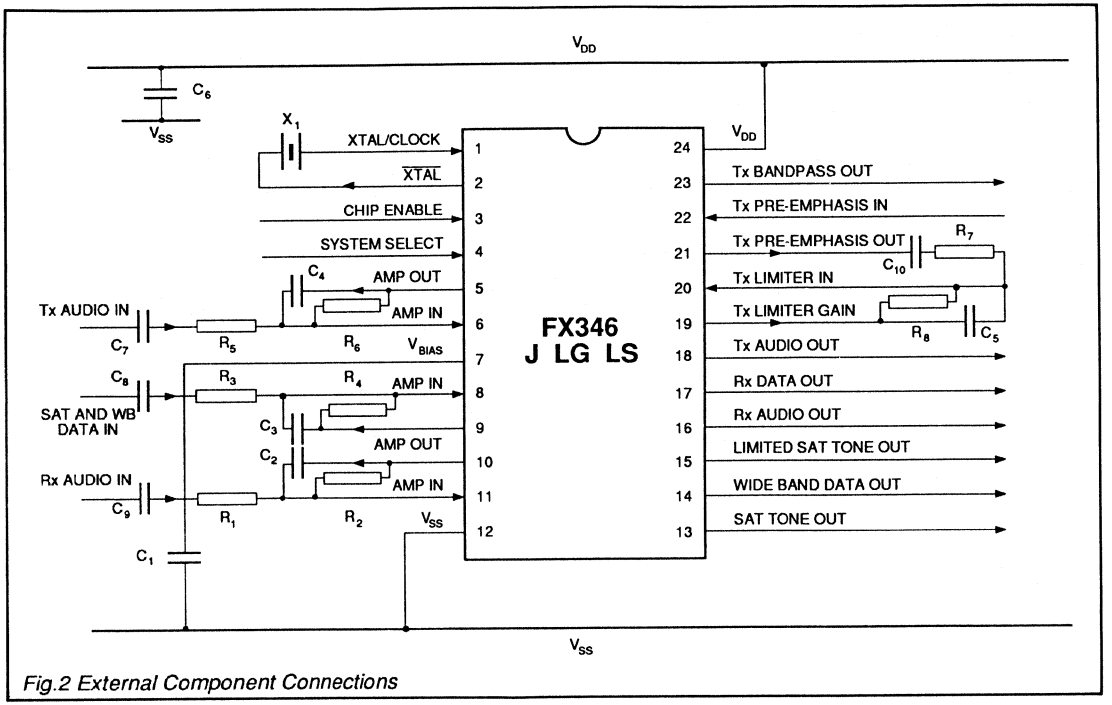



*Fig.2 External Component Connections*

### Component Value Notes

Figure 2 shows the recommended components for use with the FX346. The notes below give component values and/or calculations.

$R_2/R_1$, $R_4/R_3$, $R_6/R_5$, $R_8/R_7$.
Gain component combinations to set the gains of the *Tx Audio*, *SAT and WB Data*, *Rx Audio* and *Limiter* inputs.
Gain is calculated using the formula:

$$\text{Gain} = \frac{R_{FEEDBACK}}{R_{INPUT}}$$

– taking into account the effect of the parallel feedback capacitor.
It is recommended that all gain resistor values are kept above10kΩ.

$C_1$.
$V_{BIAS}$ decoupling capacitor = 1.0µF.

$C_2$, $C_4$ and $C_5$.
Feedback capacitor values should be calculated (taking into account gain resistors $R_1$, $R_2$, $R_5$, $R_6$, $R_7$ and $R_8$) to give a -3dB point at approximately 15kHz for Rx and Tx Channel, this for anti-alias filtering.

$C_3$.
Feedback capacitor = 10.0pF.

$C_6$.
Power supply decoupling capacitor = 1.0µF.

$C_8$.
Input coupling capacitor = 0.1µF.

$C_7$, $C_9$ and $C_{10}$.
Input coupling capacitors = 1.0µF.

**Component Tolerances**
Resistors ± 10%
Capacitors ± 20%

To maintain low current consumption, Output Buffers, anti-alias Clock Frequency Filters and input internal pullup or pulldown resistors are **not** included on-chip.

A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

## Application Information

Table 1 (below) shows the signal and data path condititons relevant to the System Select and Chip Enable inputs. Note that the oscillator circuitry and $V_{BIAS}$ line are enabled under all conditions.

| FUNCTION | | | SIGNAL PATH | | | | |
|---|---|---|---|---|---|---|---|
| System Select | 4MHz Oscillator | $V_{BIAS}$ | Tx Audio | SAT Tone | WB Data | Rx Audio | Rx Data |
| **AMPS/TACS** "1" Chip Enable = "1" | Enabled | Enabled | Enabled | 6kHz, Enabled | Enabled | Enabled | Enabled |
| Chip Enable = "0" | Enabled | Enabled | Disabled | Disabled | Enabled | Disabled | Disabled |
| **NMT** "0" Chip Enable = "1" | Enabled | Enabled | Enabled | 4kHz, Enabled | Enabled | Enabled | Enabled |
| Chip Enable = "0" | Enabled | Enabled | Disabled | Disabled | Disabled | Disabled | Enabled |

*Table1 Signal Path Selection*

Figure 3 (below) demonstrates the possible audio and data functions performed by the FX346 Audio Processing Array when employed within the audio stages of either an NMT, AMPS or TACS mobile application.

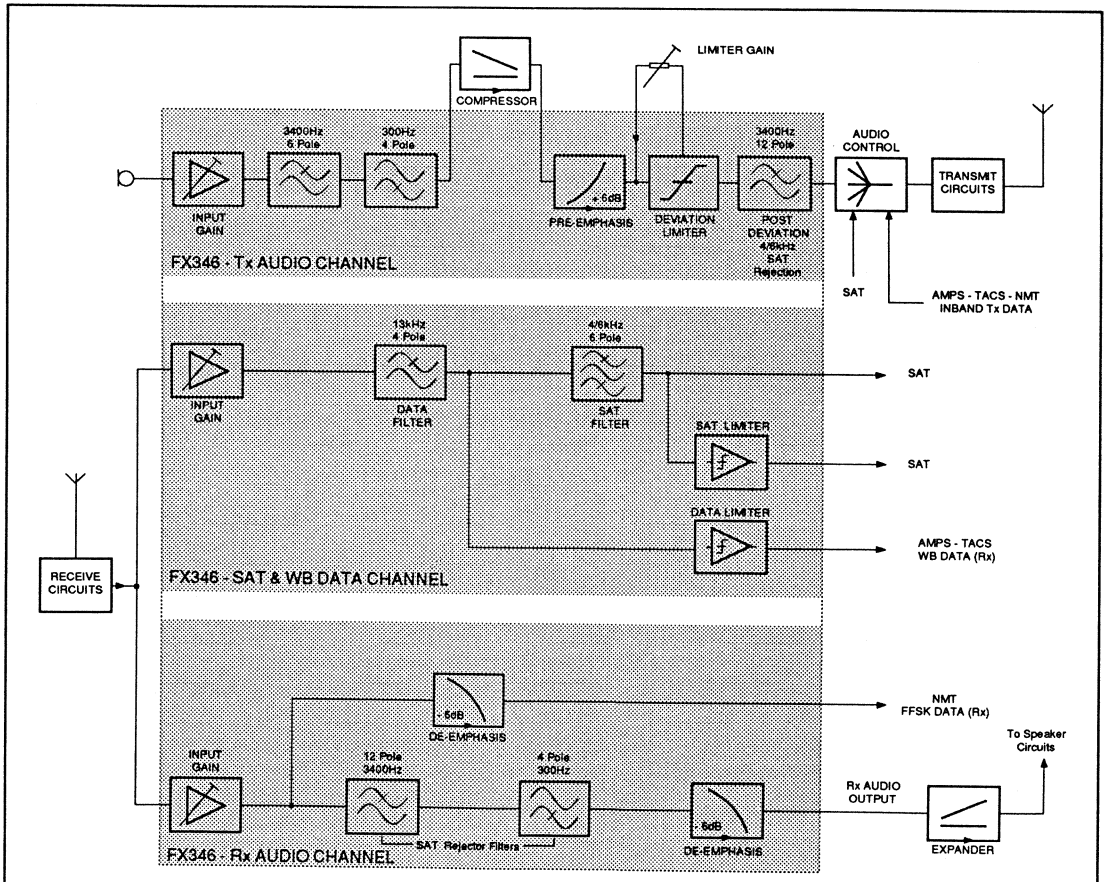



*Fig.3 Example of FX346 Employed in the Audio Stages of a Typical NMT,AMPS or TACS Mobile Application*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX346J** | -30°C to +85°C (cerdip) |
| | **FX346LG/LS** | -30°C to +70°C (plastic) |
| Storage temperature range: | **FX346J** | -55°C to +125°C (cerdip) |
| | **FX346LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.0 MHz. Audio level 0dB ref. = 300mVrms.

| Characteristics | Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage ($V_{DD}$) | | 4.5 | 5.0 | 5.5 | V |
| Input Logic '1' | 3 | 3.5 | – | – | V |
| Input Logic '0' | 3 | – | – | 1.5 | V |
| Supply Current – | 6 | | | | |
| – Enabled | | – | 12.0 | – | mA |
| – Disabled (Chip Enable = 0) – | | | | | |
| – AMPS/TACS | | – | 1.75 | – | mA |
| – NMT | | – | 1.5 | – | mA |
| **Impedance** | | | | | |
| Audio Amplifier Input/s | | 10.0 | – | – | MΩ |
| Audio Op-Amp Output/s | | – | 6.0 | 10.0 | kΩ |
| Audio Output | | – | – | 10.0 | kΩ |
| Digital Inputs | | 100 | 1000 | – | kΩ |
| Digital (data) Output/s | | – | 6.0 | 10.0 | kΩ |
| **Dynamic Values** | | | | | |
| Xtal/Clock Frequency | | – | 4.0 | – | MHz |
| Input Amplifier Gain/s | | – | – | 40.0 | dB |
| **Tx Audio Channel** | | | | | |
| Audio Input Level | 1 | – | 300 | – | mVrms |
| Overall Gain | 1, 7, 8 | – | 0 | – | dB |
| Deviation Limiter Levels | 3, 5 | 1.0 | | 4.0 | V |
| Bandpass Frequency Range (-3dB) | 8 | 300 | | 3400 | Hz |
| Pre-emphasis – | | | | | |
| – Passband | | 300 | | 3400 | Hz |
| – Response | | – | 6.0 | – | dB/octave |
| – Gain at 1kHz | | – | 0 | – | dB |
| – Passband Deviation from Ideal | | -1.0 | – | 1.0 | dB |
| Channel Stopband Attenuation – | | | | | |
| ≤ 160Hz | | – | 25 | – | dB |
| ≥ 5500Hz | | – | 40.0 | – | dB |
| Output Noise | 2 | – | 1.50 | – | mVrms |

## Specification...

| Characteristics | Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **SAT and Wideband Data Channel** | | | | | |
| Input Level | 1 | – | 300 | – | mVrms |
| Data Limiter Sensitivity | 1, 10 | | | | |
| – Limited SAT Tone (4kHz & 6kHz) | | – | 10 | – | mVrms |
| – Wideband Data | | – | 20 | – | mVrms |
| 13kHz Lowpass Filter – | | | | | |
| – Passband (-3dB) | | – | – | 15.0 | kHz |
| – Passband Gain (100Hz – 13kHz) | | -1.0 | – | +1.0 | dB |
| – Passband Ripple (100Hz – 13kHz) | | – | 2.0 | – | dB |
| – Stopband Attenuation (≥ 25kHz) | | – | 30.0 | – | dB |
| SAT Bandpass Filter – | | | | | |
| NMT 4kHz – | 4, 9 | | | | |
| – Passband Frequency Range (-6dB) | | 3800 | | 4200 | Hz |
| – Passband Gain | | – | 11.5 | – | dB |
| – Passband Ripple (4kHz ± 55Hz) | | – | – | 2.0 | dB |
| – Stopband Attenuation (<2kHz, >6kHz) | | 35.0 | 37.0 | – | dB |
| – Output Noise | 2 | – | 10.0 | – | mVrms |
| – Aliasing Frequency | | 50.0 | – | – | kHz |
| AMPS/TACS 6kHz – | 9 | | | | |
| – Passband Frequency Range (-6dB) | | 5800 | – | 6200 | Hz |
| – Passband Gain | | – | 12.0 | – | dB |
| – Passband Ripple (6kHz ± 55Hz) | | – | 2.0 | 3.0 | dB |
| – Stopband Attenuation (<4kHz, >8kHz) | | – | 35.0 | – | dB |
| – Output Noise | 2 | – | 7.5 | – | mVrms |
| **Rx Audio Channel** | | | | | |
| Input Level (Rx Audio, Rx Data) | 1 | – | 300 | – | mVrms |
| Gain | 1, 7, 8 | – | 0 | – | dB |
| Passband Frequency Range (-3dB) | 4 | 260 | | 3400 | Hz |
| Output Noise | 2 | – | 1.5 | – | mVrms |
| **Rx Data Channel** | | | | | |
| De-emphasis (Audio and Data) – | | | | | |
| – Passband | | 300 | | 3400 | Hz |
| – Response | | – | -6.0 | – | dB/octave |
| – Gain at 1kHz | | – | 0 | – | dB |
| – Passband Deviation from Ideal | | -1.0 | – | +1.0 | dB |

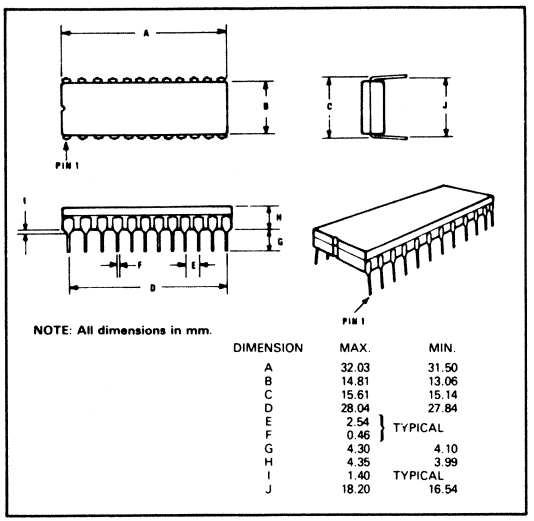
**Notes**

1. With the Input Op-Amp gain/s at unity.
2. Measured at the output with the channel input a.c. short circuit.
3. These levels are referenced to $V_{DD}$ and in this case measured with $V_{DD}$ = 5.0 volts.
4. Specified over the full operating voltage and temperature range.
5. Limiter input at $V_{BIAS}$.
6. To maintain low current consumption, buffers and clock filters are not included on-chip in series with outputs.
7. Input frequency 1.0kHz.
8. With no pre-/de-emphasis effect.
9. Shows the SAT Tone Output specification in the selected mode.
10. The minimum level at the SAT Amp Input to produce a valid logic output.

## Package Outline

The FX346J, the cerdip package is shown in Figure 4. The 'LG' version is shown in Figure 5 and the 'LS' version in Figure 6.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 4* **FX346J** *24-pin DIL Package*



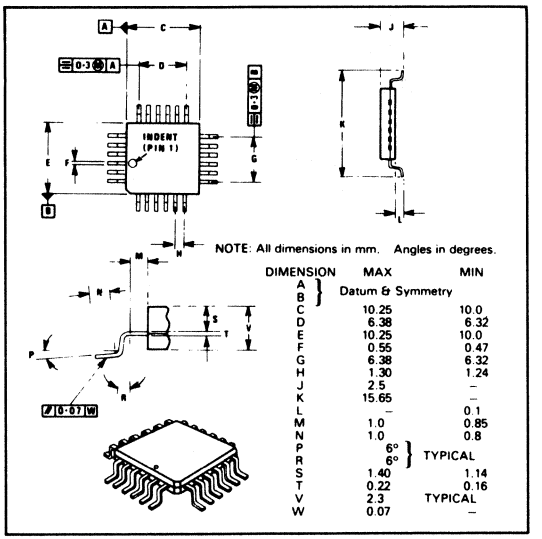

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 32.03 | 31.50 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 | TYPICAL |
| F | 0.46 | |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 | TYPICAL |
| J | 18.20 | 16.54 |

## Handling Precautions

The FX346 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

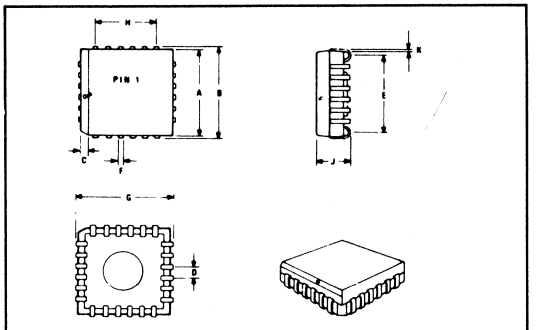
*Fig. 5* **FX346LG** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P, R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig. 6* **FX346LS** *24-pin Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.40 | | 9.70 | F | 0.55 | | 0.45 |
| B | 11.05 | | 10.60 | G | 11.05 | | 10.60 |
| C | | 1.15 x 45° | | H | | 6.35 | |
| D | | 1.27 | | J | 3.70 | | 3.25 |
| E | | 9.30 | | K | 0.27 | | 0.17 |

## Ordering Information

| | |
|---|---|
| **FX346J** | **24-pin cerdip DIL** |
| **FX346LG** | **24-pin quad plastic encapsulated bent and cropped** |
| **FX346LS** | **24-lead plastic leaded chip carrier** |

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX366 AMPS/TACS Quad Filter Array

Publication D/366/2 February 1993
Provisional Issue

## Features/Applications

- **Separate Bandpass and Lowpass Gain/Filter Blocks**
- **Global AMPS/TACS Cellular Applications**
- **Bandpass Filters**
  **4.5dB Gain (300Hz to 3000Hz)**
- **Lowpass Filters (3000Hz)**
- **Input Gain Adjustments**
- **Output Enable/Mute for Squelch Functions**
- **Small Outline Surface Mount and DIL Packages**
- **Low-Power 5V CMOS**

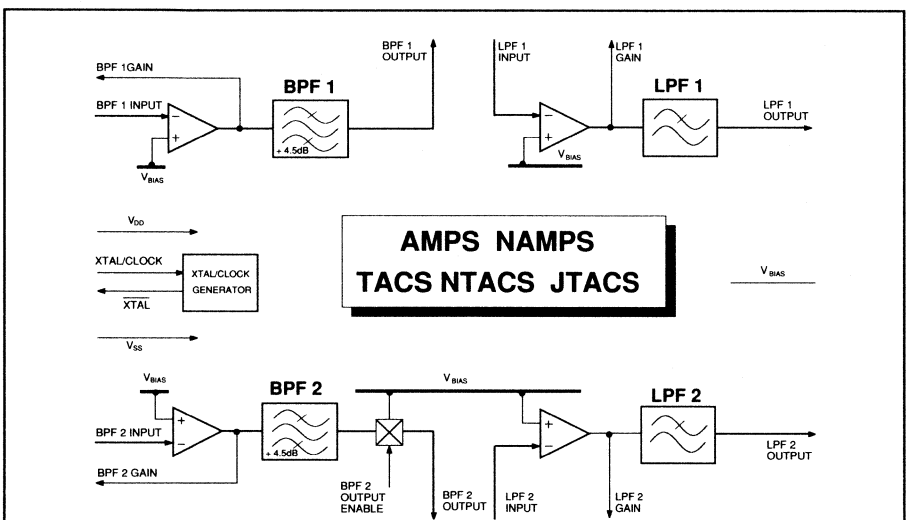



*Fig.1 The FX366 Quad Filter Array*

## Brief Description

The **FX366** AMPS/TACS Quad Filter Array comprises 4 separate individual filter/gain blocks in a single microcircuit, containing:

2 Bandpass Filters BPF 1 and BPF 2.
– 14th order 300Hz to 3000Hz –

2 Lowpass Filters LPF1 and LPF 2.
– 10th order 3100Hz –

Each filter block has an amplifier at its input for use with external components to provide functions such as, level adjustment, pre- or de-emphasis and limiting.

BPF 2 has the added facility of Output Enable which could be used as 'audio mute' in a squelch or Inband-Mixing environment.

The provision of 2 bandpass and 2 lowpass filter sections allows 2 audio channels, each of LPF and BPF pairing for use in a full-duplex Tx/Rx cellular system.

All on-chip filters meet the AMPS and TACS cellular system speechband specifications; Including NAMPS, NTACS and JTACS. Switched capacitor filter technology is employed on this chip with all switching clocks derived from an externally applied single Xtal/clock source.

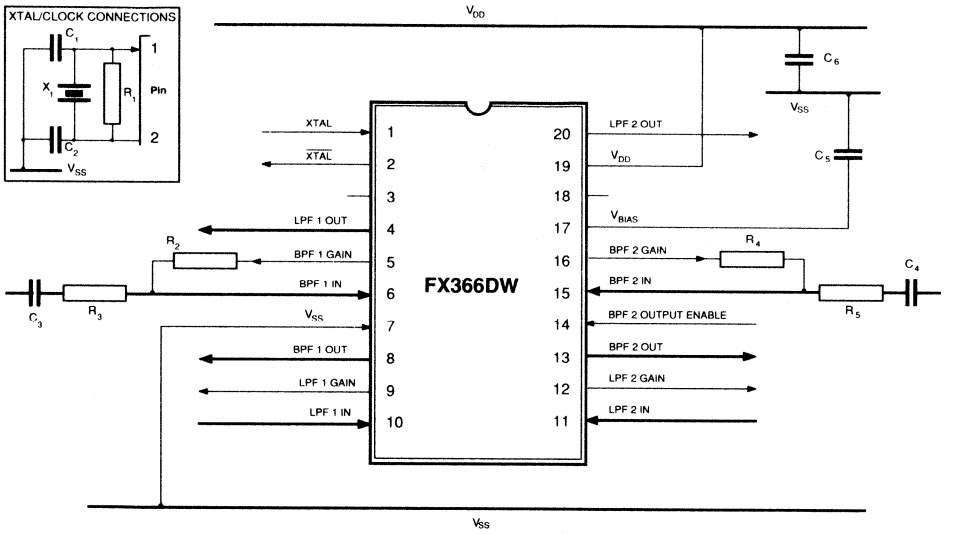
These simple, comprehensive amplifier/filter combinations eliminate the need for several separate integrated circuits therefore saving power and space.

The **FX366** is a low-power, single 5V CMOS device and is available in a 22-pin cerdip Dual-in-Line and a 20-pin plastic Small Outline (S.O.I.C.) surface mount package.

FX366

| Pin Number | | Function |
|---|---|---|
| FX366DW | FX366J | |
| 1 | 1 | **Xtal/Clock:** A 4.433619MHz Xtal or externally derived clock is injected at this pin. Operation of the FX366 without a Xtal or clock input may cause device damage. |
| 2 | 2 | **$\overline{\text{Xtal}}$:** Output of the on-chip clock oscillator inverter. |
| 4 | 4 | **LPF 1 Output:** The output of LPF 1 filter/gain block. |
| 5 | 5 | **BPF 1 Gain:** The output of BPF 1 gain-adjusting amplifier. This output is used with BPF 1 Input and external components. |
| 6 | 6 | **BPF 1 Input:** The input to BPF 1 filter/gain block. |
| 7 | 7 | **$V_{SS}$:** Negative supply (GND). |
| 8 | 8 | **BPF 1 Output:** The output of BPF 1. |
| 9 | 10 | **LPF 1 Gain:** The output of LPF 1 gain-adjusting amplifier. This output is used with LPF 1 Input and external components. |
| 10 | 11 | **LPF 1 Input:** The input to LPF 1 filter/gain block. |
| 11 | 12 | **LPF 2 Input:** The input to LPF 2 filter/gain block. |
| 12 | 13 | **LPF 2 Gain:** The output of LPF 2 gain-adjusting amplifier. This output is used with LPF 2 Input and external components. |
| 13 | 15 | **BPF 2 Output:** The output of BPF 2. This output is under the control of the BPF 2 Output Enable input. |
| 14 | 16 | **BPF 2 Output Enable:** Controls the status of BFP 2 Output. Logic "1" = Enable, Logic "0" = Muted. This pin has an internal 1.0MΩ pullup resistor. |
| 15 | 17 | **BPF 2 Input:** The input to BPF 2 filter/gain block. |
| 16 | 18 | **BPF 2 Gain:** The output of BPF 2 gain-adjusting amplifier. This output is used with BPF 2 Input and external components. |
| 17 | 19 | **$V_{BIAS}$:** The internal analogue bias line at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ by a capacitor of 1.0µF. |
| 19 | 21 | **$V_{DD}$:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this device are dependent upon this supply. |
| 20 | 22 | **LPF 2 Output:** The output of LPF 2. |
| 3, 18 | 3, 9, 14, 20 | No internal connection. Leave open circuit. |

## Application Information




| Component | | Value |
|---|---|---|
| $R_1$ | = | 1.0MΩ |

1. Configurations $R_2$, $R_3$, $C_3$ and $R_4$, $R_5$, $C_4$ should be chosen with respect to the specific application.
2. Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast-reaction fuse).

| Component | | Value |
|---|---|---|
| $C_1$ | = | 33.0pF |
| $C_2$ | | 47.0pF |
| $C_5$ | | 1.0µF |
| $C_6$ | | 0.47µF |
| $X_1$ | | 4.433619MHz |

***Tolerances***

*C = ±20%* *R = ±10%*

*Fig.2 Recommended External Components*

## The FX366 in a System

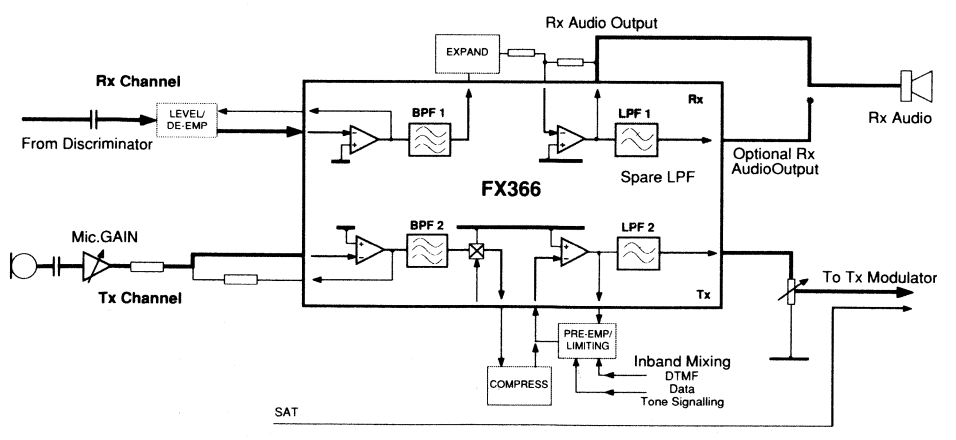



*Fig.3 Example of the FX366 Employed in the Audio Stages of a TACS Application*

# Application Information .....

## Performance

## Bandpass Sections

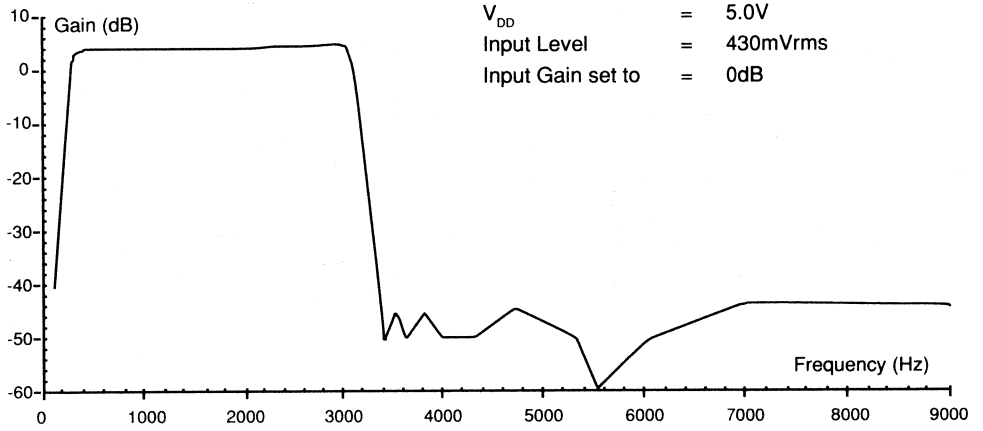



*Fig.4 Example of the FX366 Bandpass (BPF1/BPF2) Frequency Response*

When using the FX366 Quad Filter Array within a cellular system, the following points should be considered.

(1) Each bandpass filter section has a frequency range of 300Hz to 3000Hz and a typical passband gain of 4.5dB.

(2) Each lowpass filter section has a cut-off frequency of 3100Hz and a typical passband gain of 0.5dB.

(3) BPF2 Output Enable has an enable/disable operating time as shown on the Specification page.

## Lowpass Sections

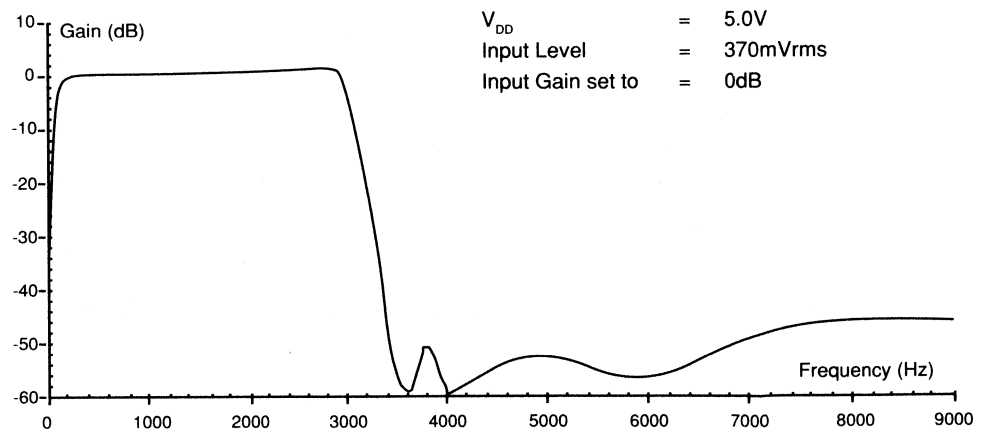



*Fig.5 Example of the FX366 Lowpass (LPF1/LPF2) Frequency Response*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX366DW** | -40°C to +85°C |
| | **FX366J** | -40°C to +85°C |
| Storage temperature range: | **FX366DW** | -40°C to +85°C |
| | **FX366J** | -55°C to +125°C |

### Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.433619MHz. Audio level 0dB ref: = 775mV rms @ 1.0kHz.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | – | 5.0 | – | mA |
| Input Impedance (Amplifiers) | | 1.0 | 10.0 | – | MΩ |
| Input Impedance (Digital) | | 100 | – | – | kΩ |
| Output Impedance (BP Filters) | | – | 2.0 | – | kΩ |
| Output Impedance (LP Filters) | | – | 2.0 | – | kΩ |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | – | – | MΩ |
| $R_{OUT}$ | | – | 10.0 | – | kΩ |
| Inverter d.c. Voltage Gain | | – | 10.0 | – | V/V |
| Gain/Bandwidth Product | | – | 10.0 | – | MHz |
| **Dynamic Values** | | | | | |
| Input Logic "1" | | 3.5 | – | – | V |
| Input Logic "0" | | – | – | 1.5 | V |
| **Analogue Levels** | | | | | |
| **LP Filters** | | | | | |
| Input | | -30.0 | – | 4.5 | dB |
| Output | | -29.5 | – | 5.0 | dB |
| **BP Filters** | | | | | |
| Input | | -30.0 | – | -1.5 | dB |
| Output | | -26.0 | – | 2.5 | dB |
| Output Noise | 2 | – | -50.0 | – | dBp |
| **Filters** | | | | | |
| **Bandpass Filter** | **1, 3** | | | | |
| Passband Frequencies | | 300 | | 3000 | Hz |
| Passband Ripple | | – | ±1.0 | – | dB |
| Low Freq. Roll-Off <200Hz | | 12.0 | – | – | dB/oct. |
| High Freq. – Attenuation at 3.4kHz | | – | 48.0 | – | dB |
| Passband Gain | | 3.5 | 4.5 | 5.5 | dB |
| Bandpass Filter 2 Output Enable | | | | | |
| Enable Time | | – | 8.0 | – | µS |
| Disable Time | | – | 20.0 | – | µS |
| **Lowpass Filter** | **1,3** | | | | |
| Cut-Off Frequency (-3dB) | | – | 3100 | – | Hz |
| Passband Ripple (300Hz - 3kHz) | | – | ±1.0 | – | dB |
| Attenuation at 3.3kHz | | – | 30.0 | – | dB |
| Attenuation at 3.6kHz | | – | 45.0 | – | dB |
| Passband Gain | | – | 0.5 | – | dB |
| Distortion | 1, 4 | – | 2.0 | – | % |

**Notes:**

1. Measured with an audio input level of –3.8dB (500mVrms).
2. With a short circuit input, at any analogue output and the measurement psophometrically weighted.
3. With Input Amplifier gain at 0dB.
4. Measured in a 30.0kHz bandwidth.

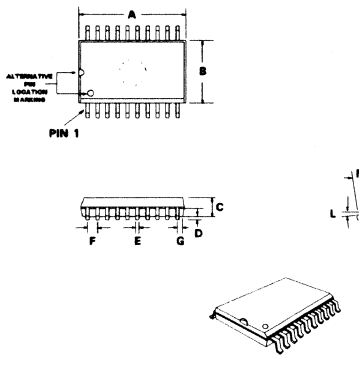
## Package Outline

The FX366DW, Small Outline Integrated Circuit package is shown in Figure 6 and the FX366J, the dual-in-line version in Figure 7.
Pin 1 identification marking is shown on the relevant diagram and pins on both package styles number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX366 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

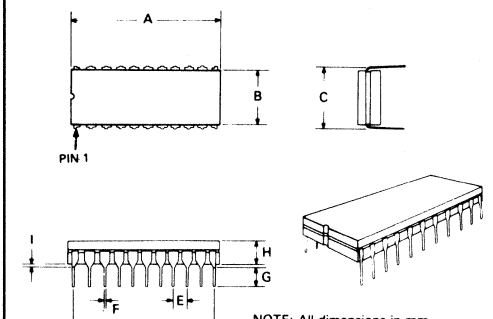
*Fig.6* ***FX366DW*** *20-pin S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 12.85 | | 12.62 | G | | 0.66 | |
| B | 7.59 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.7* ***FX366J*** *22-pin DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 | TYPICAL DIMENSION |
| F | 0.46 | |
| G | 4.35 | |
| H | 4.27 | 3.99 |
| I | – | 0.5 |

## Ordering Information

**FX366DW** 20-pin Surface Mount S.O.I.C.

**FX366J** 22-pin cerdip DIL

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX812 Voice Store and Retrieve Codec

Publication D/812/2 February 1993
Provisional Issue

## Features/Applications

- **Half-Duplex Voice Storage and Replay**
- **Serial Bus µProcessor Control**
- **On-Chip DRAM Controller**
- **Up To 2 Minutes of High-Quality Recorded Audio**
- **Answerphone and Voice-Notepad**
- **Selectable Sample Rates and "Memory Size"**
- **Small Outline (S.O.I.C.) SMD and DIL Packages**
- **Low-Power 5-Volt CMOS**

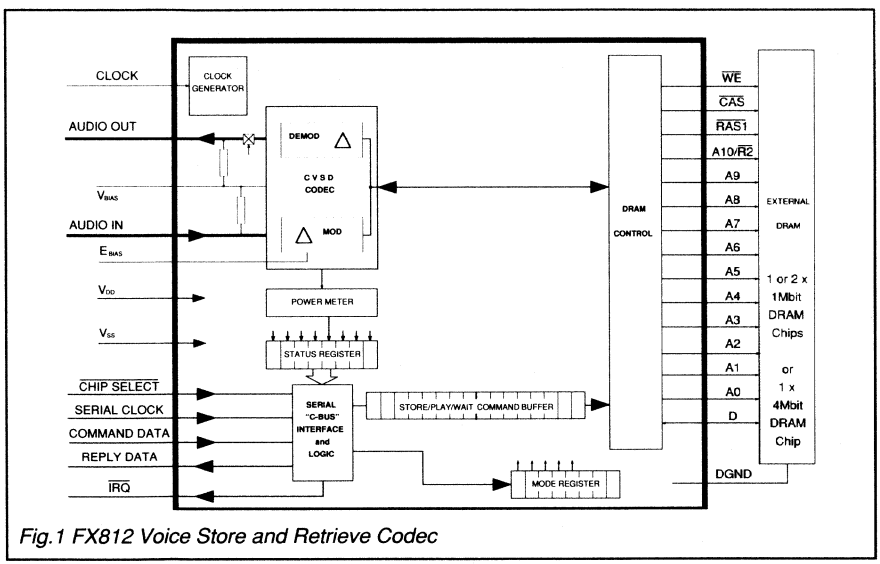



*Fig.1 FX812 Voice Store and Retrieve Codec*

**FX812**

## Brief Description

The FX812 is a half-duplex VSR Codec, which when connected to an audio processing microcircuit (such as the FX816, 826 or 836), provides the storage and recovery of speechband audio in attached Dynamic RAM. The addition of this device will enhance the communications system by providing cellular radios with "Answerphone," "Message-Notepad" and general announcement facilities.

The FX812 will enable:

- Storage of a speech message for transmission (replay) at a later time.
- Storage of a received speech message when the operator is not attending.
- The storage and subsequent replay of speech.

All VSR operating functions are controlled by a simple serial µProcessor interface which may operate from the radio's own µProcessor/Controller.

Input audio from the "Store" output of the audio processor is digitized by delta modulation and stored via the DRAM controller, in attached memory.

Audio for replay is recovered from the assigned memory locations and after demodulation made available for supply to the "Play" input of the audio processor. For use with other audio systems, the input/output audio can be connected to relevant points in circuit.

The FX812 has no on-chip input or output audio filtering, this facility must therefore be provided by the host system. Sampling rates and memory capacity are selectable to 32kb/s or 63kb/s and 1 x 4Mbit or 2 x 1Mbit respectively, which when used in conjunction allow control of audio-quality and storage-time.

This low-power CMOS device is available 28-pin plastic small outline SMD and 28-pin cerdip DIL packages.

## Pin Number Function

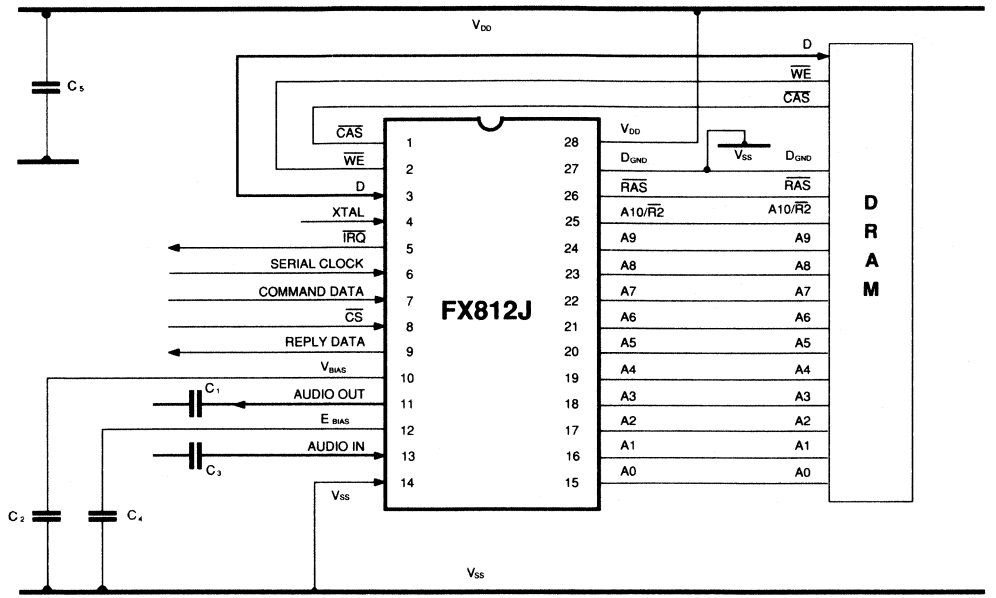
| FX812DW FX812J | |
|---|---|
| 1 | **$\overline{\text{CAS}}$:** This output should be connected to the "Column Address Strobe" input pin(s) of all DRAM devices fitted. |
| 2 | **$\overline{\text{WE}}$:** This output should be connected to the "Write Enable" input pin(s) of all DRAM devices fitted. |
| 3 | **D:** Digital (speech) data into and out of the VSR Codec. This pin should be connected to the "Data In" and "Data Out" pins ("D" and "Q") of DRAM devices. |
| 4 | **Xtal:** The nominal 4.0MHz clock input to the VSR Codec. The signal applied to this device may be derived from the attached Audio Processor on-chip Xtal Oscillator circuits (see Figures 2 and 3). **Note** that the VSR Codec will be able to function and maintain correct DRAM refresh, with Xtal input frequencies down to 2.0MHz. Compand and Local Decoder time constants will change accordingly and minimum "C-BUS" timings (Figures 6 and 7) would have to be increased pro-rata. |
| 5 | **Interrupt Request ($\overline{\text{IRQ}}$):** This Interrupt Request output from the FX812 is 'wire-OR able' allowing the Interrupt Outputs of other peripherals to be commoned and connected to the Interrupt input of the µProcessor (see the CML Serial µProcessor Data Interface publication D/µINT/1 June 1991). This output has a low-impedance pulldown to $V_{SS}$ when active, and a high-impedance when inactive. |
| 6 | **Serial Clock:** The "C-BUS" serial clock input. This clock produced by the µController, is used for transfer timing of commands and data to and from the VSR Codec. See Timing Diagrams. |
| 7 | **Command Data:** The "C-BUS" serial (command) data input from the µController. Data is loaded to this device in 8-bit bytes MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. |
| 8 | **Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data transfer control function. This input is provided by the µController. Transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams. |
| 9 | **Reply Data:** The "C-BUS" serial data output to the µController. The transmission of reply bytes is synchronized to the Serial Clock under the control of the Chip Select input. This is a 3-state output which is held at a high-impedance when not sending data to the µController. |
| 10 | **$V_{BIAS}$:** The output of the internal analogue circuitry bias line, held internally at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ by capacitor $C_2$ (see Figure 2). |
| 11 | **Audio Out:** The analogue output to the Audio Processor "Play" input when the VSR Codec is configured as a Decoder. When configured as an active Decoder but with no Play Page commands ($62_H$) active, the VSR Codec will play-out an idle pattern of "101010.....10$^s$". When not configured as a Decoder, or Powersaved (Mode Register), this output will be held at $V_{BIAS}$ via an internal 500kΩ resistor. The output at this pin is unfiltered; An external speechband filter – such as that included on the FX816/826/836 Audio Processors – will be required. As this output is centred about $V_{DD}/2$ a coupling capacitor is required. |
| 12 | **$E_{BIAS}$:** The Encoder d.c. internal balancing circuitry line. This pin should be decoupled to $V_{SS}$ by a capacitor $C_4$, (see Figure 2). **Note** that in the 'Encode' mode (Mode Register DE and PS both "0") the Codec drives this pin to approximately $V_{DD}/2$ through a very high impedance; It can take more than one second for the $E_{BIAS}$ voltage to stabilize when power is first applied to this device. A faster start--up can be achieved by setting Bit DE or PS to "1" for 250mS (approx) during power-up. This will cause the $E_{BIAS}$ pin to be connected to $V_{BIAS}$ through a resistance of approximately 100kΩ. |
| 13 | **Audio In:** The analogue input to the VSR Codec in the Encode mode. When not configured as an Encoder, or Powersaved (Mode Register), this input will be held at $V_{BIAS}$ via an internal 500kΩ resistor. This pin should be coupled via a capacitor, see Figure 2. As this input does not contain an internal audio filter, the audio to this pin should be limited to a 3400Hz "speechband" by an external audio filter – such as included in the FX816/826/836 Audio Processors. |
| 14 | **$V_{SS}$:** The "analogue" ground connection. See $D_{GND}$ description. |

## Pin Number Function

| FX812DW FX812J | Function |
|---|---|
| 15 | **A0:** DRAM address line outputs from the FX812. These pins should be connected to the corresponding address inputs of the associated DRAM. |
| 16 | **A1:** |
| 17 | **A2:** |
| 18 | **A3:** |
| 19 | **A4:** |
| 20 | **A5:** |
| 21 | **A6:** |
| 22 | **A7:** |
| 23 | **A8:** |
| 24 | **A9:** |
| 25 | **A10/$\overline{R2}$:** A dual function output pin selected by the memory size (MS) bit (Mode Register), as detailed in the table below: |
| 26 | **$\overline{RAS}$:** An output from the VSR Codec which should be connected to the "Row Address Strobe" pin of the 4Mbit DRAM or the first 1Mbit DRAM, see Figure 4, Example DRAM connections. |
| 27 | **$D_{GND}$:** The digital signal ground connection to the VSR Codec. Both $D_{GND}$ and $V_{SS}$ pins should be connected to the negative side of the d.c. power supply, however the printed circuit board should be laid out so that $D_{GND}$ is connected as closely as possible to the DRAM section ground pins. |
| 28 | **$V_{DD}$:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the VSR Codec are dependent upon this supply. This pin should be decoupled to $V_{SS}$ via capacitor $C_5$, located close to the FX812 pins. |

| MS bit | DRAMs | Connected To | This Output |
|---|---|---|---|
| "0" | 1Mbits' | DRAM No 2 $\overline{RAS}$ | RAS2 |
| "1" | 4Mbit | DRAM A10 | A10 Signal |

# Application Information




| Component | Value |
|---|---|
| $C_1$ | Dependant upon the input impedance of the driven stage |
| $C_2$ | 1.0µF |
| $C_3$ | 100nF |
| $C_4$ | 1.0µF non-electrolytic |

Tolerance: Capacitors = -50/+100%

*Fig.2 Recommended External Components*

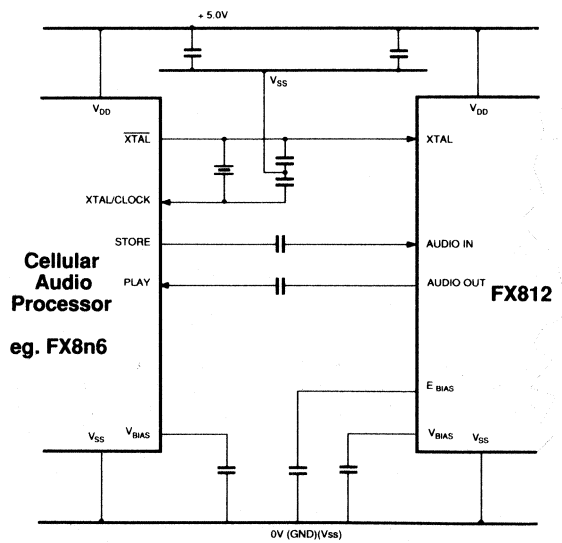



*Fig.3 Interfacing to an Audio Processor*

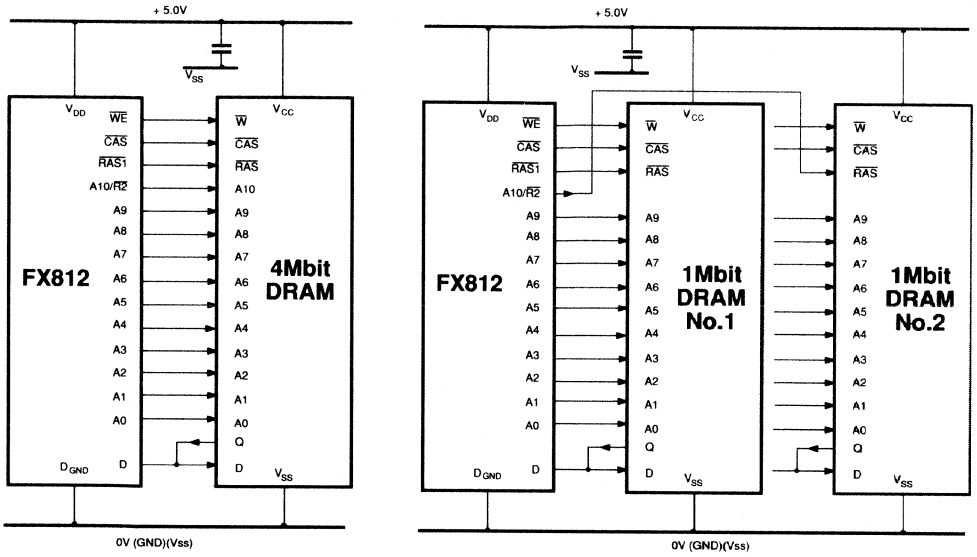



*Fig.4 Example DRAM Connections*

### Choice of DRAM Devices

DRAM devices chosen should be standard 1,048,576 x 1 or 4,194,304 x 1 Dynamic Random Access memories, with 'CAS before RAS' refresh, and a Row Address access time of 200 nano-seconds or less.

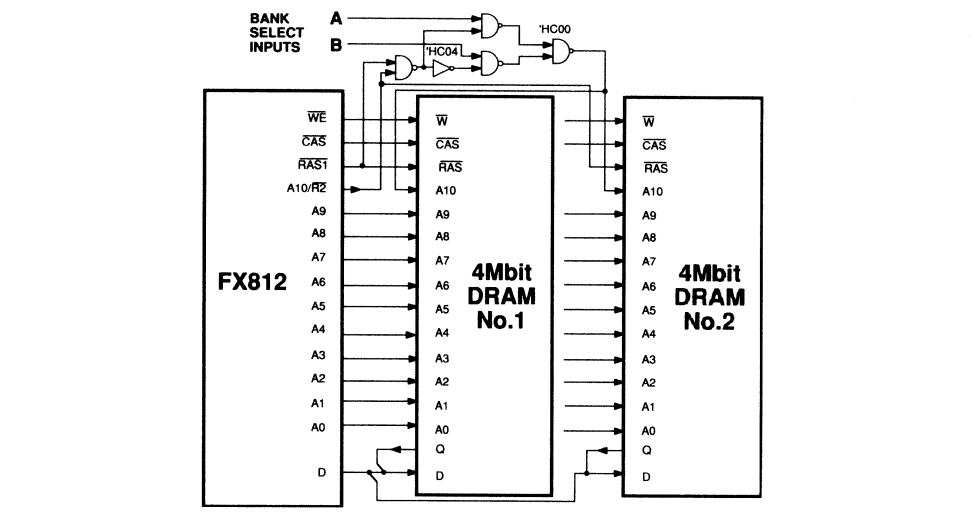



*Fig.5 Employment of External Elements to Drive Two 4-MBit DRAM Chips*

## Driving Two 4-MBit DRAM Sections

By the addition of external logic circuitry, the FX812 can be configured to drive two 4-MBit DRAM sections. This will have the effect of doubling the available storage time. i.e. 4 minutes at 32kb/s.

With reference to the circuitry shown in Figure 5:

With the Mode Register **MS** Bit set to "0" the FX812 treats the DRAM sections as two 1-Mbit devices. The external logic makes each 4-MBit DRAM appear as four 1-MBit banks selected by the Bank Select lines '**A**' and '**B**.'

| Bank Select Inputs | | DRAM No 1 Pages | DRAM No 2 Pages |
|---|---|---|---|
| A | B | 0 – 1023 | 1024 – 2047 |
| 0 | 0 | ■ | ■ |
| 1 | 0 | ■ | ■ |
| 0 | 1 | ■ | ■ |
| 1 | 1 | ■ | ■ |

# The Controlling System

## "C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

---

Control of the functions and levels within the FX812 VSR Codec is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the FX812.
The use of these instructions is detailed in the following paragraphs and tables.

| Command Assignment | Address/Command (A/C) Byte Hex. | Binary MSB LSB | + | Data Byte/s |
|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | |
| Write to Mode Register | 60 | 0 1 1 0 0 0 0 0 | + | 1 byte Instruction to Mode Register |
| Read Status Register | 61 | 0 1 1 0 0 0 0 1 | + | 1 byte Reply from Status Register |
| Store/Play Page | 62 | 0 1 1 0 0 0 1 0 | + | 2 bytes Command |
| Wait | 63 | 0 1 1 0 0 0 1 1 | | |

*Table 1 – "C-Bus" Address/Commands*

## "Write to Mode Register" – A/C $60_H$, followed by 1 byte of Command Data.

**Interrupt Output – IE**
Controls the FX812 IRQ output driver.

**Sampling Rates – SR**
The CVSD Codec sampling rates. Accurate rates depend upon the applied Xtal/clock frequency (see Table 5).

**Memory Size – MS**
The FX812 can operate with 1 x 1Mbit, 2 x 1Mbit or 1 x 4Mbit of DRAM (see Figure 4).

**Powersave – PS**
Powersaves the CVSD Codec only. Logic functions and DRAM refresh are maintained.

**Decode/Encode – DE**
The Codec and DRAM operational mode."
"Play" or "Store"

| *Setting* | *Mode Bits* |
|---|---|
| ***MSB*** | ***Transmitted to 812 First*** |
| ***7*** | **Interrupt Output** |
| 1 | Enable |
| 0 | Disable |
| ***6*** | **Sampling Rate** |
| 1 | 63kb/s |
| 0 | 32kb/s |
| ***5*** | **Memory (DRAM) Size** |
| 1 | Single 4Mbit |
| 0 | 1 or 2 x 1Mbit |
| ***4*** | **Powersave** |
| 1 | CVSD Codec Powersaved |
| 0 | CVSD Codec Powered |
| ***3*** | **Decode/Encode** |
| 1 | Decode – Play Mode |
| 0 | Encode – Store Mode |
| ***2 1 0*** | **Not Used** |
| 0 0 0 | Set to 'zeros' |

*Table 2 Control Register*

## Interrupts

The FX812's Interrupt Output is driven by the Status Bit 7 (IF) when the Mode Register Bit7 (IE) is set to a "1."

The IF bit and the Interrupt Output (If enabled) are set when the Store/Play/Wait command Buffer is emptied (MT bit) by transferring from the buffer to the DRAM control circuits.

and/or

The IF bit and the Interrupt Output (if enabled) are set when a Store, Play or Wait command has finished **and** the Command Buffer is empty.

The notes below illustrate the $\overline{IRQ}$ pin conditions:

| IF Bit | IE Bit | $\overline{IRQ}$ |
|---|---|---|
| "0" cleared | "0" disable | High Z |
| "0" cleared | "1" enable | High Z |
| "1" Interrupt | "0" disable | High Z |
| "1" Interrupt | "1" enable | $V_{SS}$ (logic "0") |

## "General Reset" – A/C $01_H$

Upon Power-Up the "bits" in the FX812 registers will be random (either "0" or "1"). A General Reset Command ($01_H$) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX812.

*Clear all Mode Register bits to "0"*
*Status Register Bit 7 (IF) to "0"*
*Bits 5 and 6 (MT and I) to "1"*
*Halt any current Store, Play or Wait execution*
*Clear the Store/Play/Wait Command Buffer*

## "Read Status Register" – A/C $61_H$, followed by 1 byte of Reply Data.

| *Reading* | *Status Bits* |
|---|---|
| ***MSB*** | ***Received from 812 First*** |
| ***7*** | **Interrupt Condition (Flag)** |
| 1 | Bit 6 or 5 set to a "1" |
| 0 | Cleared condition |
| ***6*** | **Command Buffer** |
| 1 | Buffer Empty |
| 0 | Cleared condition |
| ***5*** | **Device Condition** |
| 1 | Idle |
| 0 | Storing, Playing or Waiting |
| ***4 3 2 1 0*** | **Input Power Level** |

*Table 3 Status Register*

**Interrupt Condition (Flag) – IF**

**Set** to a logic "1" whenever Bit 6 or Bit 5 goes from "0" to "1" (unless the transition is caused by a "General Reset" command $01_H$). This indication allows monitoring by 'poll' whilst Interrupts are disabled.
**Cleared** to a logic "0" by a General Reset command or immediately following a read of the Status Register.

**Command Buffer Status – MT**

**Set** to a logic "1" when the Command Buffer is empty or by a General Reset command.
**Cleared** to a logic "0" by loading a new Store, Play, Wait commands.

**Device Condition – I**

**Set** to a logic "1" when **NO** Store, Play or Wait command is being executed or by a General Reset command.
**Set** to a logic "0" whilst a Store, Play or Wait command is being executed.

**Encode Input Power Level – POWER**

Available in the Encode mode, a 5-bit representation of the analogue signal input level, updated at the end of every Store or Wait command.

## Store/Play/Wait Command Buffer

A buffer used to accept and hold the latest Store, Play or Wait command received over the "C-BUS" while the FX812 is executing the previous command. The Status Register, bit 6, indicates the condition of this buffer.

When a command is received it is first loaded into this buffer. If the FX812 is already executing a previously loaded Store, Play or Wait command the new command will be stored temporarily in the Command Buffer from where it will be taken on completion of the previous command.

This permits the FX812 to perform a continuous sequence of Store, Play or Wait commands, without gaps and without requiring an unduly fast response from the µController.

Note that this Command Buffer can only hold one Store, Play or Wait instruction, each new command received into this buffer will overwrite any previously loaded contents.

To Store or Play a sequence of pages the relevant commands should be loaded with sequential page numbers whilst observing the Status Register – Bit 6.

## "Store/Play Page" – A/C $62_H$, followed by 2 bytes of Command Data.

For the purposes of storage and replay, the attatched DRAM is divided into 'data-pages' of 1024 bits (1kbit).
One Store/Play command (loaded MSB first) will instruct the FX812 to store or play (depending upon the setting of the Mode Register, Bit-3) to or from 1 x 1024 "page" of DRAM. The Store/Play/Wait command buffer will allow continuity of operation.

The particular page selected is identified by the 12 lowest bits of the 2 x Store/Play bytes as shown below.
If a Store command is loaded and executed whilst the Codec is "Powersaved" in the Encode mode, the selected DRAM page will be filled with an idle pattern ("101010.....").

| | Bit Number | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ***MSB – Loaded to FX812 First*** | | | | | | | | | | | | | | | ***Loaded Last – LSB*** | |
| **Bit** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **Bit** |
| **Value** | **x** | **x** | **x** | **x** | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ | **Value** |
| **Page** | "0" | "0" | "0" | "0" | DRAM Page Number | | | | | | | | | | | | Page |

| DRAM Size | Valid Page Nos | Bit Nos |
|---|---|---|
| 4Mbit | 0 – 4095 | 0 – 11 |
| 1 + 1Mbit | 0 – 2047 | 0 – 10 |
| 1Mbit | 0 – 1023 | 0 – 9 |

## "Wait" – A/C $63_H$, — Wait for 1024 bit periods

Causes the FX812 to wait for 1024 bit periods (approximately 16 0r 32msec).
If the Codec is set to the Encode mode, a new "Power" reading that is relevant to the input audio level, will be loaded into the Status Register at the end of the Wait period.
If the Codec is set to the Decode mode it will 'Play' a perfect idle pattern ("101010.....") during the Wait period.

# Control Timing Information

## Control Timing

Figure 6 shows the timing parameters for two-way communication between the µController and Cellular peripherals on the "C-BUS." Figure 7 shows the timing relationships between the Serial Clock and Data.

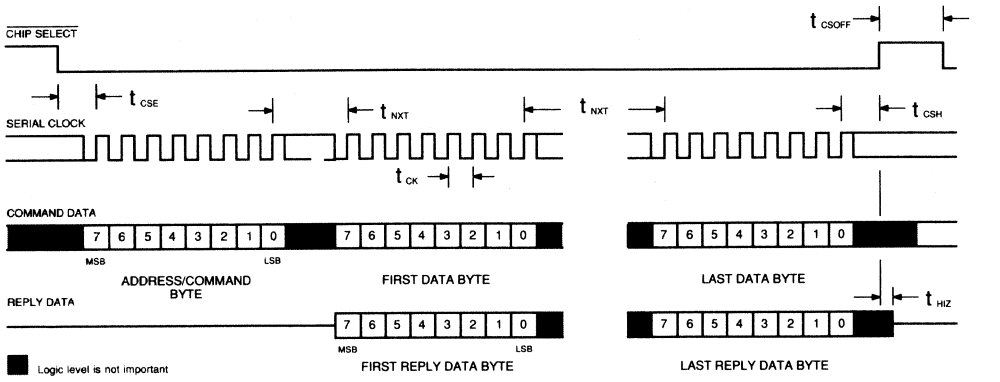



*Fig.6 Control Timing Information*

*NOT TO SCALE*

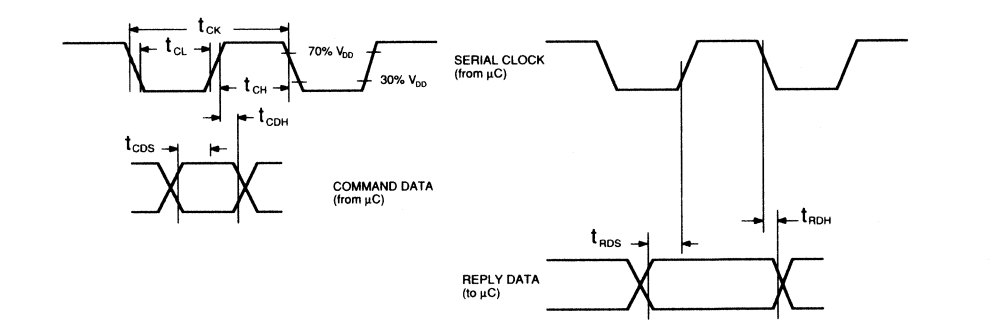



*Fig.7 Control Timing Relationships*

*NOT TO SCALE*

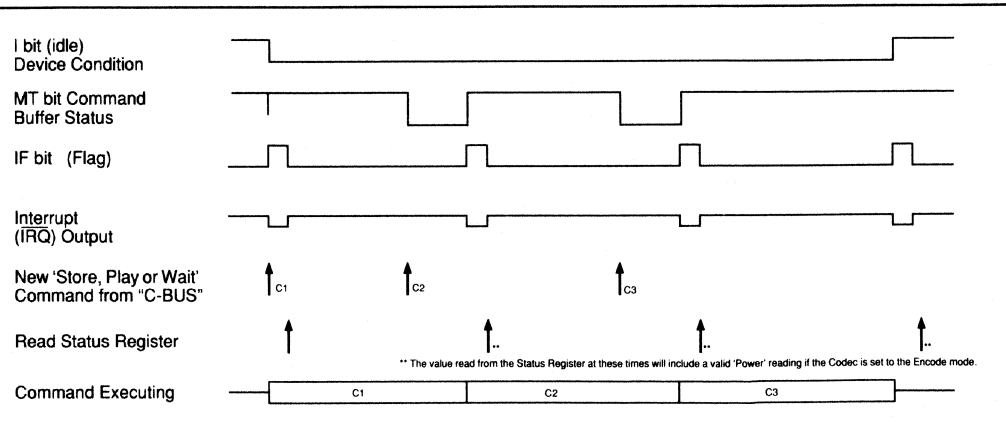



*Fig.8 Typical Command Sequences*

## Control Timing Information .....

Timing Specification – Figures 6 and 7

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CSE}$ | "CS-Enable to Clock-High" | | 2.0 | – | – | µs |
| $t_{CSH}$ | Last "Clock-High to CS-High" | | 4.0 | – | – | µs |
| $t_{HIZ}$ | "CS-High to Reply Output Tri-state" | | – | – | 2.0 | µs |
| $t_{CSOFF}$ | "CS-High" Time between transactions | | 2.0 | – | – | µs |
| $t_{CK}$ | "Clock-Cycle" Time | | 2.0 | – | – | µs |
| $t_{NXT}$ | "Inter-Byte" Time | | 4.0 | – | – | µs |
| $t_{CH}$ | "Serial Clock-High" Period | | 500 | – | – | ns |
| $t_{CL}$ | "Serial Clock-Low" Period | | 500 | – | – | ns |
| $t_{CDS}$ | "Command Data Set-Up" Time | | 250 | – | – | ns |
| $t_{CDH}$ | "Command Data Hold" Time | | 0 | – | – | ns |
| $t_{RDS}$ | "Reply Data Set-Up" Time | | 250 | – | – | ns |
| $t_{RDH}$ | "Repy Data Hold" Time | | 50.0 | – | – | ns |

## Address Line Decoding

MA0 to MA21 are the outputs of the internal 22-bit DRAM address counter, which are time multiplexed as 'Row' and 'Column' addresses onto the DRAM address lines A0 to A10 etc., as shown below.

**Memory Size (MS) Bit = "1" – 4Mbit DRAM**

| Pin | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10/R2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Row Address | MA0 | MA2 | MA4 | MA6 | MA8 | MA10 | MA12 | MA14 | MA16 | MA18 | MA20 |
| Column Address | MA1 | MA3 | MA5 | MA7 | MA9 | MA11 | MA13 | MA15 | MA17 | MA19 | MA21 |

**Memory Size (MS) Bit = "0" – 1Mbit DRAM(s)**

| Pin | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 |
|---|---|---|---|---|---|---|---|---|---|---|
| Row Address | MA0 | MA2 | MA4 | MA6 | MA8 | MA10 | MA12 | MA14 | MA16 | MA18 |
| Column Address | MA1 | MA3 | MA5 | MA7 | MA9 | MA11 | MA13 | MA15 | MA17 | MA19 |

| MA20 | MA21 | RAS1 | A10/R2 | DRAM Selected |
|---|---|---|---|---|
| 0 | x | active | | "first" |
| 1 | x | | active | "second" |

*x = don't care*

*Table 4 Address Line Decoding*

| | | Xtal/clock Frequency (MHz) | | |
|---|---|---|---|---|
| | | 4.0 | 4.032 | 4.096 |
| Sample Rate (SR) Bit | Division Ratio | Sampling Rate (kbits/s) | | |
| SR = "1" | 64 | 62.50 | 63.00 | 64.00 |
| SR = "0" | 128 | 31.25 | 31.50 | 32.00 |
| | | Internal Clock Rate (kHz) | | |
| Local Decoder Clock | | 125.0 | 126.0 | 128.0 |

*Table 5 Sampling Clock Rates Available*

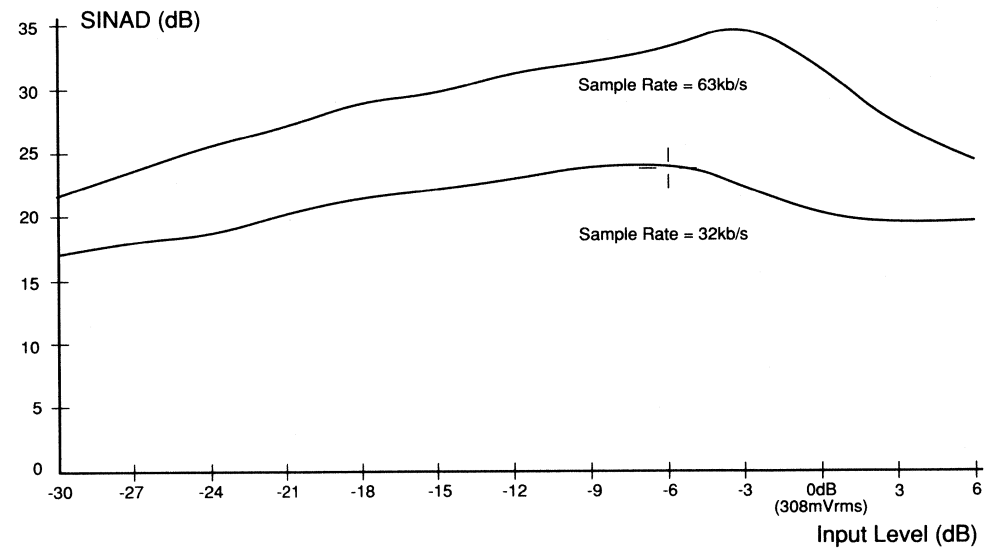



*Fig.9 Typical "SINAD vs Input Level" Plot*

**Performance**

Figure 9 Shows a typical graph of SINAD vs Input Level produced for both 32kb/s and 63kb/s sample rates at an input frequency of 1.0kHz.

Figure 10 shows a typical graph of the "Power" reading for increasing input signal levels. The "Power" figure (0 to 31) is the binary figure obtained from the 5-bit representation in the Status Register - Bits 0, 1, 2, 3 and 4 whilst the Codec is selected to the Encode mode.

This reading is updated at the end of every Store or Wait command; Excessive input signal levels will record "$11111_2$" ($31_{10}$).

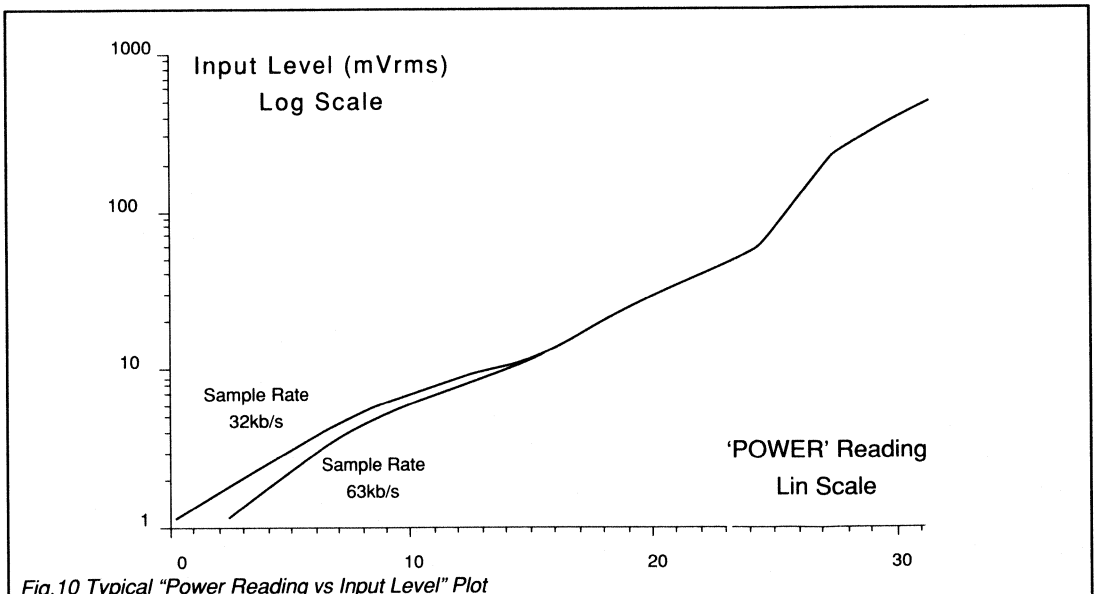



*Fig.10 Typical "Power Reading vs Input Level" Plot*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref. $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX812DW** | -40°C to +85°C (plastic) |
| | **FX812J** | -40°C to +85°C (cerdip) |
| Storage temperature range: | **FX812DW** | -40°C to +85°C (plastic) |
| | **FX812J** | -55°C to +125°C (cerdip) |

### Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.00MHz. Audio level 0dB ref: = 308mV rms @ 1.0kHz.
Reply Data Line loaded with 50pF//200kΩ to $V_{SS}$.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | | | | |
| Enabled | 1 | – | 3.0 | – | mA |
| Powersaved | 1 | – | 1.0 | – | mA |
| Analogue Input Impedance | | – | 100 | – | kΩ |
| Analogue Output Impedance (Decode) | | – | 1.0 | – | kΩ |
| Analogue Output Impedance (Encode or Powersave) | | – | 500 | – | kΩ |
| **DRAM Interface** | | | | | |
| Input Logic "1" | 2 | 3.5 | – | – | V |
| Input Logic "0" | 2 | – | – | 1.5 | V |
| Output Logic "1" (at $I_o$ = -120µA) | 3 | 2.7 | – | – | V |
| Output Logic "0" (at $I_o$ = 120µA) | 3 | – | – | 0.4 | V |
| Input Leakage Current (at $V_{IN}$ = 0 to $V_{DD}$) | 4 | -1.0 | – | 1.0 | µA |
| Input Capacitance | 2 | – | 10.0 | – | pF |
| **Digital Interface** | | | | | |
| Input Logic "1" | 5 | 3.5 | – | – | V |
| Input Logic "0" | 5 | – | – | 1.5 | V |
| $I_{IN}$ (logic "1" or "0") | 5 | -1.0 | – | 1.0 | µA |
| Output Logic Levels | | | | | |
| Output Logic "1" (-120µA) | 6 | 4.6 | – | – | V |
| Output Logic "0" (360µA) | 7 | – | – | 0.4 | V |
| $I_{Out}$ Tri-state (logic "1" or "0") | 6 | -4.0 | – | 4.0 | µA |
| Input Capacitance | 5 | – | – | 7.5 | pF |
| IOX ($V_{Out}$ = 5V) | 8 | – | – | 4.0 | µA |
| **Dynamic Values** | | | | | |
| "Xtal" Pin Input Frequency Range | 12 | 4.0 | | 4.1 | MHz |
| **Store Mode** | | | | | |
| Analogue Input Signal Levels | 9 | -24.0 | – | 4.0 | dB |
| Analogue Input Signal Frequency Range | 9, 10 | 300 | | 3400 | Hz |
| Recommended Signal Source Impedance | 9 | – | – | 2.0 | kΩ |
| **Play Mode** | | | | | |
| Analogue Output Signal Levels | 13 | -7.0 | – | -5.0 | dB |
| Output Noise (idle) | 11 | – | -55.0 | – | dBp |
| **Overall 'Store to Play' Performance** | | | | | |
| Output Noise (Input Short Circuit) | 11 | – | -50.0 | – | dBp |
| SINAD (**SR** = 32kb/s) (Input = 1.0kHz @ -6.0dB) | 11 | – | 23.0 | – | dB |

### Notes

1. Not including DRAM current.
2. D input from DRAM
3. Outputs to DRAM.
4. All digital inputs.
5. Serial Clock, Command Data and Chip Select inputs.
6. Reply Data output.
7. Reply Data and Interrupt ($\overline{IRQ}$) outputs.
8. Leakage current into the "Off" Interrupt ($\overline{IRQ}$) output.
9. For optimum performance.
10. Input filtering must be performed at the source.
11. Measured in conjunction with the FX836 R2000 system Audio Processor.
12. For full "C-BUS" compatibility.
13. Playback of a stored "-6.0dB 1.0kHz Test Signal."

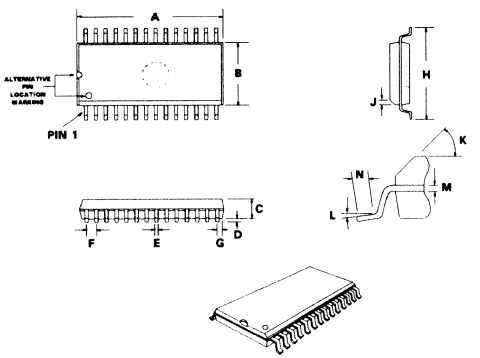
## Package Outline

The FX812DW Small Outline Integrated Circuit is shown in Figure 11 and the "J" version in Figure 12. Pin 1 identification marking is shown on the relevant diagram.
Pins on both package styles number anti-clockwise when viewed from the top (marked side).

## Handling Precautions

The FX812 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

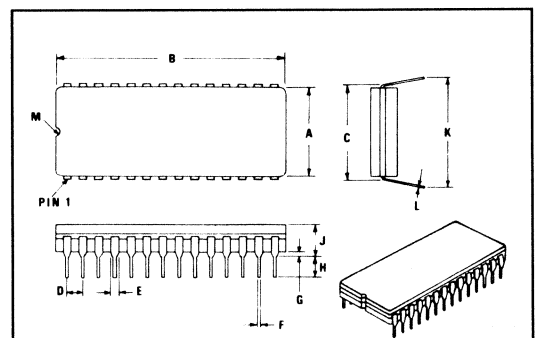
*Fig.11* ***FX812DW*** *28-pin S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 18.05 | | 17.70 | G | | 0.66 | |
| B | 7.65 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.12* ***FX812J*** *28-pin DIL Package*




All dimensions in mm Angles in degrees

| DIMENSION | MAX | MIN | DIMENSION | MAX | MIN |
|---|---|---|---|---|---|
| A | 13.36 | 13.06 | G | 1.40 | TYPICAL |
| B | 37.05 | 36.58 | H | 4.30 | 4.10 |
| C | 15.70 | 15.50 | J | 5.57 | 4.49 |
| D | 2.54 | TYPICAL | K | 17.00 | TYPICAL |
| E | 1.39 | TYPICAL | L | 0.25 | TYPICAL |
| F | 0.45 | TYPICAL | M | 0.64R | TYPICAL |

## Ordering Information

**FX812DW** 28-pin plastic S.O.I.C.

**FX812J** 28-pin cerdip DIL

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX816 NMT System Audio Processor

Publication D/816/2 February 1993
Provisional Issue

## Features/Applications

- **Full-Duplex Audio Processing for NMT Cellular System**
- **On-Chip Speech and SAT Facilities**
  ***– Tx/Rx/SAT Filtering & Gain – VOGAD – Pre-/De-Emphasis – Deviation Limiter –***
- **Serial µProcessor Interface**
- **Separate SAT Channel**
- **"Sidetone" Output Available**
- **HandsFree Compatibility**
- **Access to External Processes**
  ***– Compression – Expansion – Signalling/Data Mixing – VSR Codec (Store/Play) –***
- **Powersave (Low-Current) Settings**

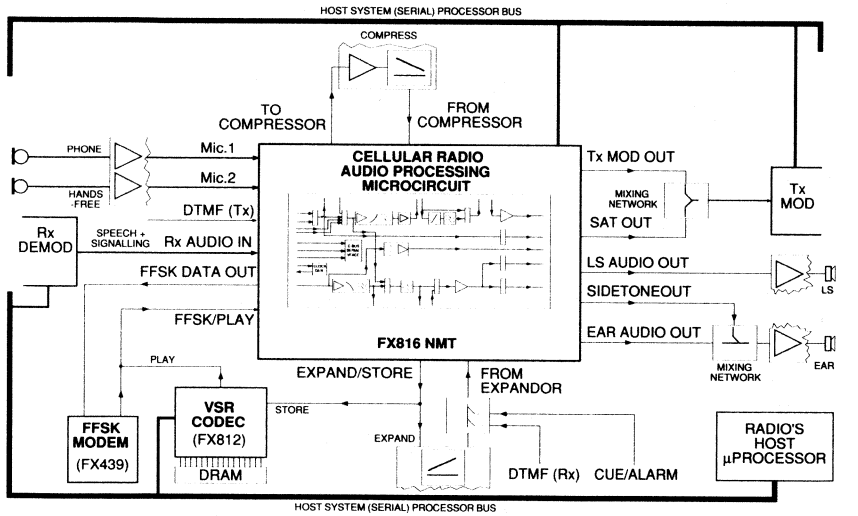



*Fig.1 The FX816 NMT Audio Processor Installed within a Cellular System*

FX816

## Brief Description

The FX816 is a µProcessor controlled full-duplex audio processor on a single-chip with separate Tx and Rx paths to provide all the filter/gain/limiting functions necessary to pre-process audio, data and signalling in the Nordic Mobile Telephone (NMT) cellular communications system.

Selectable inputs available to the transmit path are: a choice of two microphones, DTMF/signalling or FFSK/data, with access, in this path, to external compression circuitry. Operationally the Tx path provides input gain/filtering, VOGAD, a deviation limiter and Tx Modulation Drive controls.

In the Rx path the SAT signal is separated from the incoming audio via a gain/filter block and made available at a separate pin for mixing externally with the Tx Modulation Drive.

The Rx path consists of an input gain/filter block for voice and data, inputs from an external audio expansion system and an output gain control driving either a loudspeaker system or earpiece.

Unique to the FX816/826/836 cellular audio processors is the ability to route audio (Tx or Rx) to an external Voice Store and Retrieve (VSR) device such as the FX802 or FX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

The FX816, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

## Pin Number Function

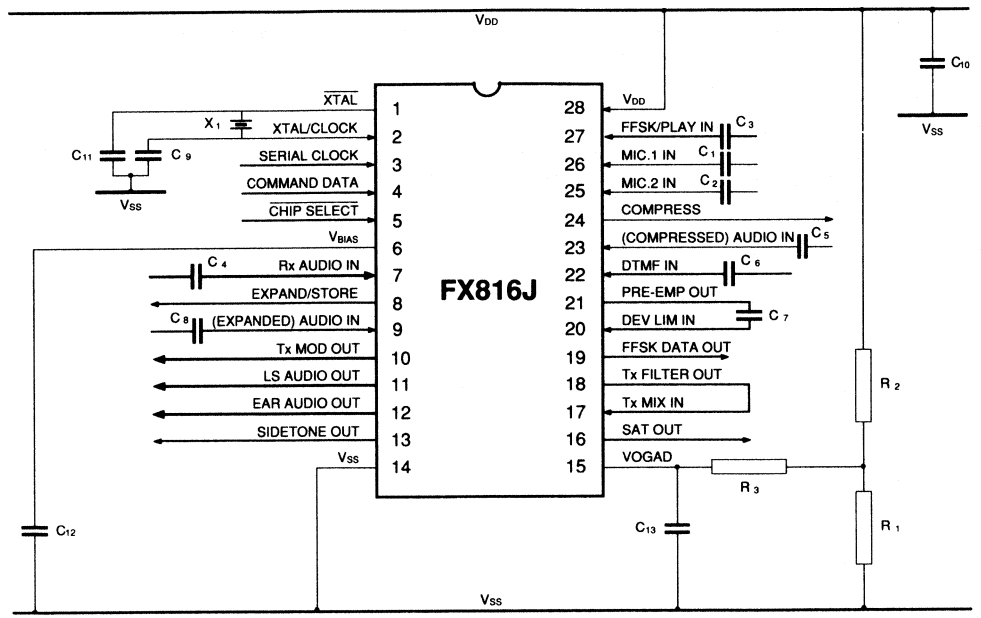
| FX816DW | FX816J | |
|---|---|---|
| 1 | 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. |
| 2 | 2 | **Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock ($f_{XTAL}$) should be connected here. Note that operation of the FX816 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes). |
| 3 | 3 | **Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the FX816. See Timing Diagrams. |
| 4 | 4 | **Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the FX816 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams. |
| 5 | 5 | **Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams. |
| 6 | 6 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$. See Figure 2. |
| 7 | 7 | **Rx Audio In:** Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to $V_{BIAS}$ and requires to be connected via a capacitor. |
| 8 | 8 | **Expand/Store:** A common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the FX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3. |
| 9 | 9 | **(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to $V_{BIAS}$ and requires to be connected via a capacitor. See Figures 2 and 3. |
| 10 | 10 | **Tx Mod Out:** The composite Tx audio output to the transmitter modulator from a variable attenuation stage ($11_H$). This output is set to $V_{BIAS}$ via an internal 1MΩ resistor when set to Powersave or OFF. |
| 11 | 11 | **LS Audio Out:** An audio output of the Rx path (or selected audios, see Figures 3 and 4) for a loudspeaker system. This is available for handsfree operation. This output can be connected to $V_{BIAS}$ when not required, by SW6 (Configuration Command ($10_H$)). A driver amplifier may be required. |
| 12 | 12 | **Ear Audio Out:** An audio output of the Rx path (or selected audios, see Figures 3 and 4), available as an output for a handset earpiece. This output in parallel with the LS Audio Out function, can be connected to $V_{BIAS}$ when not required, by SW7 (Configuration Command ($10_H$)). A driver amplifier may be required. |
| 13 | 13 | **Sidetone:** A switched "sidetone" from the microphone inputs made available for mixing externally with the "Ear" audio. See Figure 3. |
| 14 | 14 | **$V_{SS}$:** Negative supply rail. Signal ground. |
| | | ***Notes on Inputs:*** *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.* |

## Pin Number Function

| FX816DW | FX816J | |
|---|---|---|
| 15 | 15 | **VOGAD:** External components (R and C) at this pin control the attack and decay time constants of the on-chip VOGAD function. |
| 16 | 16 | **SAT Out:** The output of the SAT bandpass filter. This level, which is recovered from the input Rx audio. This tone level can be modified by the SAT and Powersave Command ($13_H$) and is available for mixing externally with the transmitter modulation. See Figures 3 and 4. |
| 17 | 17 | **Tx Mix In:** An input and output available, with external components, to introduce signalling tones into the Tx Path prior to the final level adjustment. |
| 18 | 18 | **Tx Filter Out:** |
| 19 | 19 | **FFSK Out:** The de-emphasized Rx audio output available for access to the received FFSK data. This output could be directed to an FFSK Modem such as the FX439. |
| 20 | 20 | **Deviation Limiter In:** Input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve the best possible symmetry of limiting as this input has a 1MΩ internal resistor to $V_{BIAS}$. See Figure 2. |
| 21 | 21 | **Pre-Emphasis Out:** Audio output from the VOGAD circuitry in the Tx Input Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figure 2. |
| 22 | 22 | **DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the Tx Path, controlled by SW2 (Configuration Command ($10_H$)). This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 23 | 23 | **Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 24 | 24 | **Compression:** The output to an external audio compression system. Currently available compressor/ expanders have Op-Amps incorporated. The compressor can be by-passed by SW2. |
| 25 | 25 | **Mic.2 In:** Tx voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any Tx audio input. Pre-amplification may be required at these inputs. These inputs each have an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 26 | 26 | **Mic.1 In:** |
| 27 | 27 | **FFSK/Play In:** The Tx FFSK data input via SW2. This can also be used to input (replay) from a voice storage device such as the FX812. This "replayed" audio can be sent to Rx or Tx paths allowing a Messaging/Voice Notepad/Answering facility. Both FX439 FFSK Modem and FX812 VSR Codec outputs can be wired directly to this pin if the functions are activated one-at-a-time. This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 28 | 28 | **$V_{DD}$:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this Audio Processor are dependent upon this supply. |

***"C-BUS"** is CML's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController. For further details refer to CML Publication No. D/µINT/1 June 1991.*

## Application Information




| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $R_1$ | = | 100kΩ | $C_2$ | = | 100nF | $C_6$ | = | 100nF | $C_{10}$ | = | 100nF |
| $R_2$ | | 100kΩ | $C_3$ | | 100nF | $C_7$ | | 100nF | $C_{11}$ | | 33pF |
| $R_3$ | | 2.2MΩ | $C_4$ | | 100nF | $C_8$ | | 100nF | $C_{12}$ | | 1.0µF |
| $C_1$ | | 100nF | $C_5$ | | 100nF | $C_9$ | | 33pF | $C_{13}$ | | 0.1µF |
| | | | | | | | | | $X_1$ | | 4.032MHz |

**Tolerances** – Resistors ±10% Capacitors ±20%

*Fig.2 Recommended External Components*

## Notes

1. **Xtal/clock operation**
Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast-reaction fuse).

2. **VOGAD components**
$R_1$, $R_2$, $R_3$ and $C_{13}$ with the VOGAD Pin internal impedance, form the VOGAD timing circuitry.
Control-Voltage Attack Time is set by
$C_{13}$ x Internal Impedance.
Control-Voltage Decay Time is set by
$C_{13}$ x $R_3$ – *assuming* $R_3 >> R_1$ *and* $R_2$.

3. **FFSK Modem**
The FX439, a general purpose FFSK Modem could be employed with this NMT system Audio Processor. The FX439 is a non-formatted modem, which with due regard to Xtal/clock frequencies and µProcessor interface, is compatible with both Mobile/Portable and Base Station applications.

4. **SAT Output**
It is possible, due to the high output impedance of this output, that an external buffer amplifier is required at this output when interfacing or mixing with other system sections.

## NMT Cellular System Interfaces

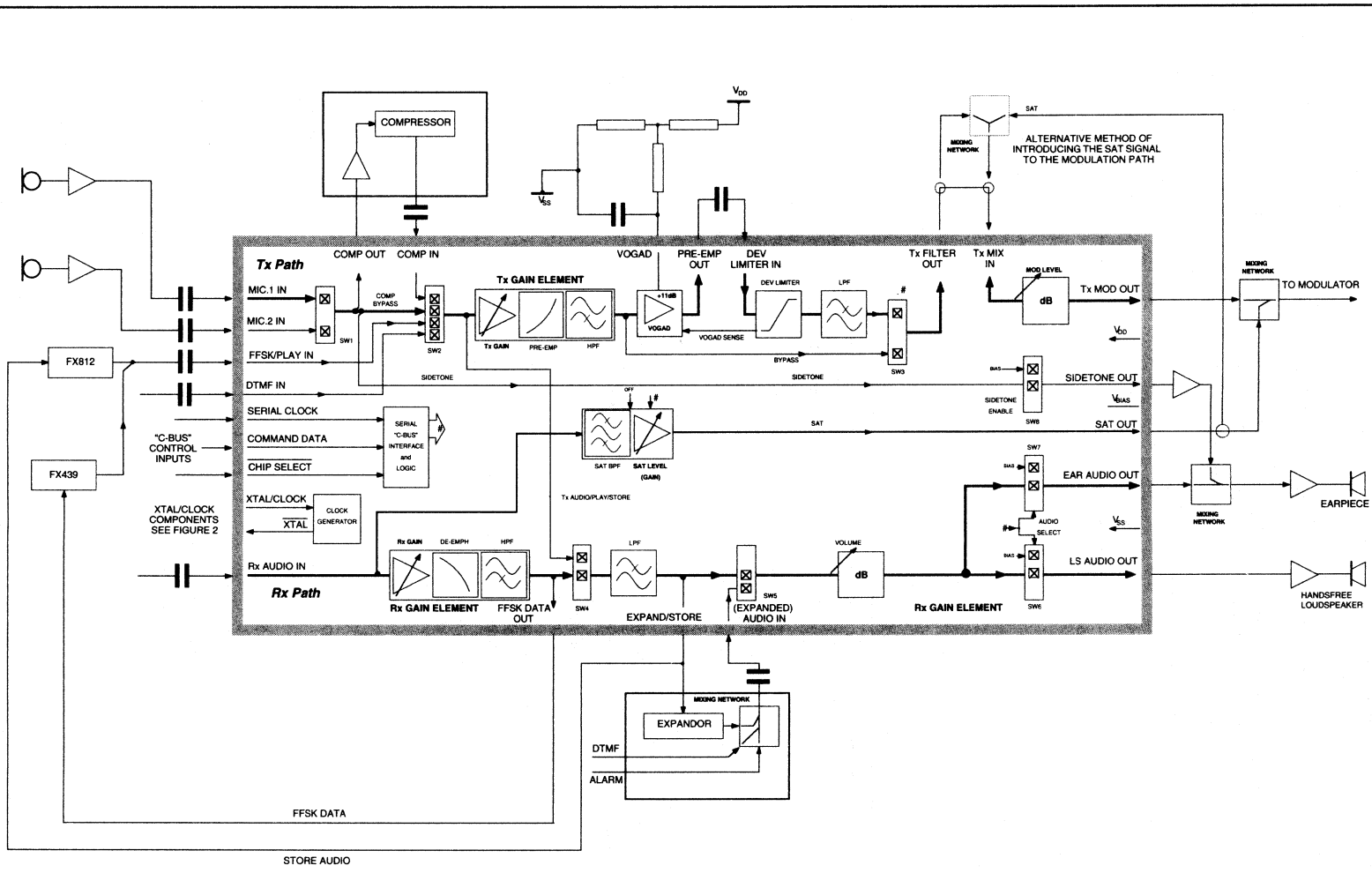



*Fig.3 The FX816 within an NMT Cellular Radio System*

# The Controlling System

## "C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

---

Control of the functions and levels within the FX816 NMT Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device.
The use of these instructions is detailed in the following paragraphs and tables.

| Command Assignment | Address/Command (A/C) Byte Hex | Binary MSB LSB | | Command Data | Table |
|---|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | | |
| Configuration Command | 10 | 0 0 0 1 0 0 0 0 | + | 1 byte | 2 |
| Tx Gain & Mod. Command | 11 | 0 0 0 1 0 0 0 1 | + | 1 byte | 3 |
| Rx Gain & Vol. Command | 12 | 0 0 0 1 0 0 1 0 | + | 1 byte | 4 |
| SAT & P/Save Command | 13 | 0 0 0 1 0 0 1 1 | + | 1 byte | 5 |

*Table 1 "C-Bus" Address/Commands*

In "C-BUS" protocol the audio processor is allocated Address/Command (A/C) values $10_H$ to $13_H$. Configuration, Tx/Rx Gains and SAT/Powersave assignments and data requirements are given in Table 1.
Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams–Figures 5 and 6.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A **General Reset Command ($01_H$)** will be required to set all FX816 registers to $00_H$.

## Configuration Command *(Preceded by A/C $10_H$)*

| *Setting* | | *Control Bits* |
|---|---|---|
| ***MSB*** | | ***Transmitted First*** |
| ***Bit 7*** | | **Sw8 Sidetone** |
| 0 | | Sidetone Bias |
| 1 | | Sidetone Enabled |
| ***6*** | | **Sw6/7 Rx Audio** |
| 0 | | Ear Enabled, LS Bias |
| 1 | | LS Enabled, Ear Bias |
| ***5*** | | **Sw5 Expander** |
| 0 | | Expander By-Pass |
| 1 | | Expander Route |
| ***4*** | | **Sw4 Tx/Rx Audio** |
| 0 | | Tx Store/Audio |
| 1 | | Rx Store/Audio |
| ***3*** | | **Sw3 Dev. Limiter** |
| 0 | | Dev. Limiter By-Pass |
| 1 | | Dev. Limiter Route |
| ***2*** | | **Sw1 Mic. Inputs** |
| 0 | | Mic. 1 Input |
| 1 | | Mic.2 Input |
| ***1*** | ***0*** | **Sw2 Tx Function** |
| 0 | 0 | DTMF In |
| 0 | 1 | Compressor In |
| 1 | 0 | Compressor By-Pass |
| 1 | 1 | FFSK/Play In |

*Table 2 Configuration Commands*

## Tx Gain & Mod. Command *(Preceded by A/C $11_H$)*

| *Setting* | | | | *Gain (dBs)* |
|---|---|---|---|---|
| ***MSB*** | | | | ***Transmitted First*** |
| ***7*** | ***6*** | ***5*** | ***4*** | **Tx Mod. Level** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -5.6 |
| 0 | 0 | 1 | 0 | -5.2 |
| 0 | 0 | 1 | 1 | -4.8 |
| 0 | 1 | 0 | 0 | -4.4 |
| 0 | 1 | 0 | 1 | -4.0 |
| 0 | 1 | 1 | 0 | -3.6 |
| 0 | 1 | 1 | 1 | -3.2 |
| 1 | 0 | 0 | 0 | -2.8 |
| 1 | 0 | 0 | 1 | -2.4 |
| 1 | 0 | 1 | 0 | -2.0 |
| 1 | 0 | 1 | 1 | -1.6 |
| 1 | 1 | 0 | 0 | -1.2 |
| 1 | 1 | 0 | 1 | -0.8 |
| 1 | 1 | 1 | 0 | -0.4 |
| 1 | 1 | 1 | 1 | 0 |
| ***3*** | ***2*** | ***1*** | ***0*** | **Tx Input Gain** |
| 0 | 0 | 0 | 0 | -2.65 |
| 0 | 0 | 0 | 1 | -2.05 |
| 0 | 0 | 1 | 0 | -1.50 |
| 0 | 0 | 1 | 1 | -0.95 |
| 0 | 1 | 0 | 0 | -0.45 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0.45 |
| 0 | 1 | 1 | 1 | 0.85 |
| 1 | 0 | 0 | 0 | 1.25 |
| 1 | 0 | 0 | 1 | 1.65 |
| 1 | 0 | 1 | 0 | 2.05 |
| 1 | 0 | 1 | 1 | 2.40 |
| 1 | 1 | 0 | 0 | 2.70 |
| 1 | 1 | 0 | 1 | 3.05 |
| 1 | 1 | 1 | 0 | 3.35 |
| 1 | 1 | 1 | 1 | 3.65 |

*Table 3 Tx Gain & Mod. Commands*

# The Controlling System .....

## Rx Gain & Vol. Command *(Preceded by A/C $12_H$)*

| *Setting* | | | | *Gain (dBs)* |
|---|---|---|---|---|
| ***MSB*** | | | | ***Transmitted First*** |
| ***7*** | ***6*** | ***5*** | ***4*** | **Rx LS Volume** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -28.0 |
| 0 | 0 | 1 | 0 | -26.0 |
| 0 | 0 | 1 | 1 | -24.0 |
| 0 | 1 | 0 | 0 | -22.0 |
| 0 | 1 | 0 | 1 | -20.0 |
| 0 | 1 | 1 | 0 | -18.0 |
| 0 | 1 | 1 | 1 | -16.0 |
| 1 | 0 | 0 | 0 | -14.0 |
| 1 | 0 | 0 | 1 | -12.0 |
| 1 | 0 | 1 | 0 | -10.0 |
| 1 | 0 | 1 | 1 | -8.0 |
| 1 | 1 | 0 | 0 | -6.0 |
| 1 | 1 | 0 | 1 | -4.0 |
| 1 | 1 | 1 | 0 | -2.0 |
| 1 | 1 | 1 | 1 | 0 |
| ***3*** | ***2*** | ***1*** | ***0*** | **Rx Input Gain** |
| 0 | 0 | 0 | 0 | 3.75 |
| 0 | 0 | 0 | 1 | 4.30 |
| 0 | 0 | 1 | 0 | 4.80 |
| 0 | 0 | 1 | 1 | 5.30 |
| 0 | 1 | 0 | 0 | 5.80 |
| 0 | 1 | 0 | 1 | 6.20 |
| 0 | 1 | 1 | 0 | 6.55 |
| 0 | 1 | 1 | 1 | 7.05 |
| 1 | 0 | 0 | 0 | 7.40 |
| 1 | 0 | 0 | 1 | 7.80 |
| 1 | 0 | 1 | 0 | 8.15 |
| 1 | 0 | 1 | 1 | 8.50 |
| 1 | 1 | 0 | 0 | 8.80 |
| 1 | 1 | 0 | 1 | 9.10 |
| 1 | 1 | 1 | 0 | 9.40 |
| 1 | 1 | 1 | 1 | 9.70 |

*Table 4 Rx Gain and Vol. Commands*

## SAT & P/Save Command *(Preceded by A/C $13_H$)*

| *Setting* | | | | *Control Bits* |
|---|---|---|---|---|
| ***MSB*** | | | | ***Transmitted First*** |
| ***Bit 7*** | | | | |
| 0 | | | | Must be a logic "0" |
| ***6*** | | | | |
| 0 | | | | Must be a logic "0" |
| ***5*** | ***4*** | ***3*** | ***2*** | **SAT Tone Level** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -1.95 |
| 0 | 0 | 1 | 0 | -1.40 |
| 0 | 0 | 1 | 1 | -0.90 |
| 0 | 1 | 0 | 0 | -0.45 |
| 0 | 1 | 0 | 1 | -0 |
| 0 | 1 | 1 | 0 | 0.40 |
| 0 | 1 | 1 | 1 | 0.85 |
| 1 | 0 | 0 | 0 | 1.20 |
| 1 | 0 | 0 | 1 | 1.60 |
| 1 | 0 | 1 | 0 | 1.95 |
| 1 | 0 | 1 | 1 | 2.30 |
| 1 | 1 | 0 | 0 | 2.60 |
| 1 | 1 | 0 | 1 | 2.90 |
| 1 | 1 | 1 | 0 | 3.25 |
| 1 | 1 | 1 | 1 | 3.50 |
| ***1*** | | | | **Powersave Rx Gain Element** |
| 0 | | | | Powersave Element |
| 1 | | | | Enable Element |
| ***0*** | | | | **Powersave FX816** (except Rx Gain Element) |
| 0 | | | | Powersave FX816 |
| 1 | | | | Enable FX816 |

*Table 5 SAT and Powersave Commands*

## Reference Signal Levels

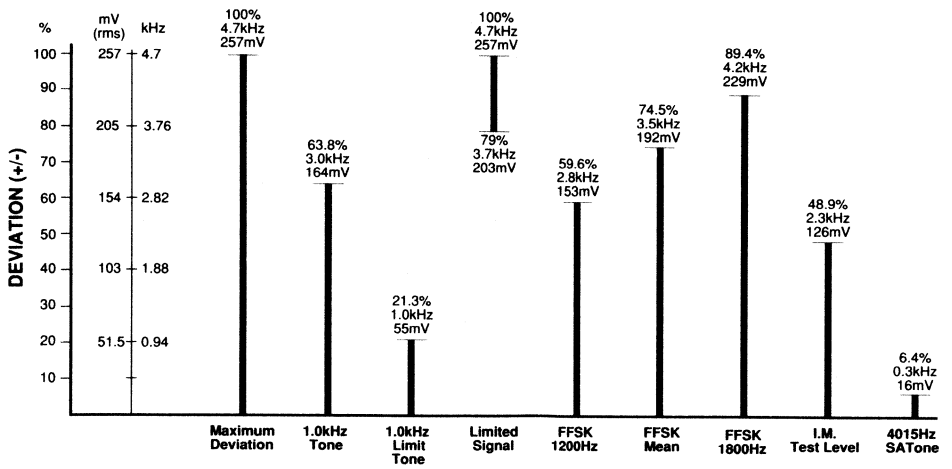



*Fig.4 NMT Signal Deviation Levels and corresponding **Tx Mod Outputs** with the Mod Level set to 0dB*

# Control Timing Information

Timing Specification – Figures 5 and 6.

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CSE}$ | "CS-Enable to Clock-High" | 1 | 2.0 | – | – | µs |
| $t_{CSH}$ | Last "Clock-High to CS-High" | 1 | 4.0 | – | – | µs |
| $t_{CSOFF}$ | "CS-High" Time between transactions | 1, 2 | 2.0 | – | – | µs |
| $t_{CK}$ | "Clock-Cycle" Time | 1 | 2.0 | – | – | µs |
| $t_{NXT}$ | "Inter-Byte" Time | 1 | 4.0 | – | – | µs |
| $t_{CH}$ | "Serial Clock-High" Period | | 500 | – | – | ns |
| $t_{CL}$ | "Serial Clock-Low" Period | | 500 | – | – | ns |
| $t_{CDS}$ | "Command Data Set-Up" Time | | 250 | – | – | ns |
| $t_{CDH}$ | "Command Data Hold" Time | | 0 | – | – | ns |

**Notes**

1. These Minimum Timing values are altered during operation of the FX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

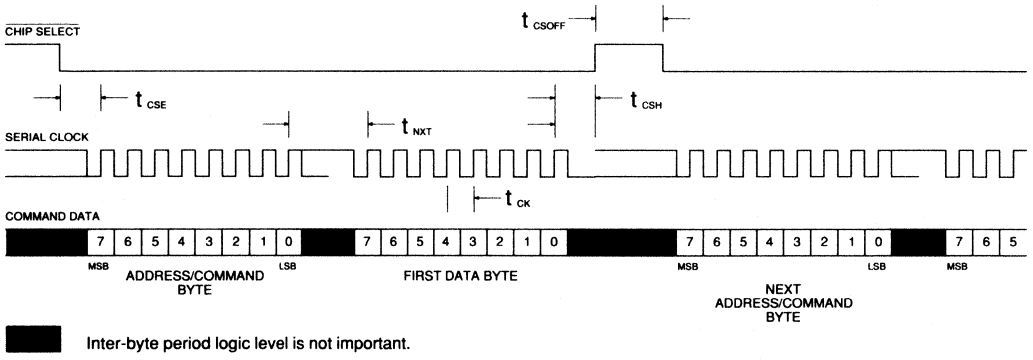



*Fig.5 Control Timing Information*

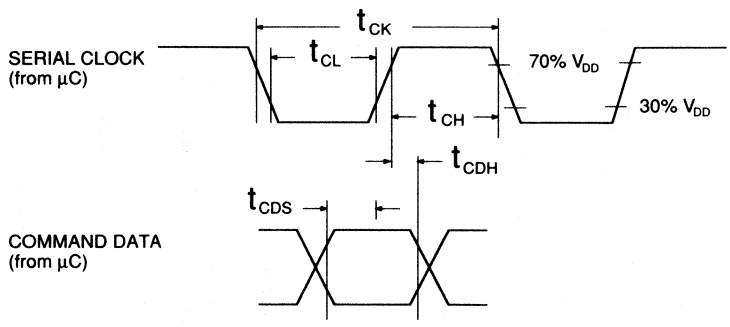



*Fig.6 Control Timing Relationships*

## System Performance

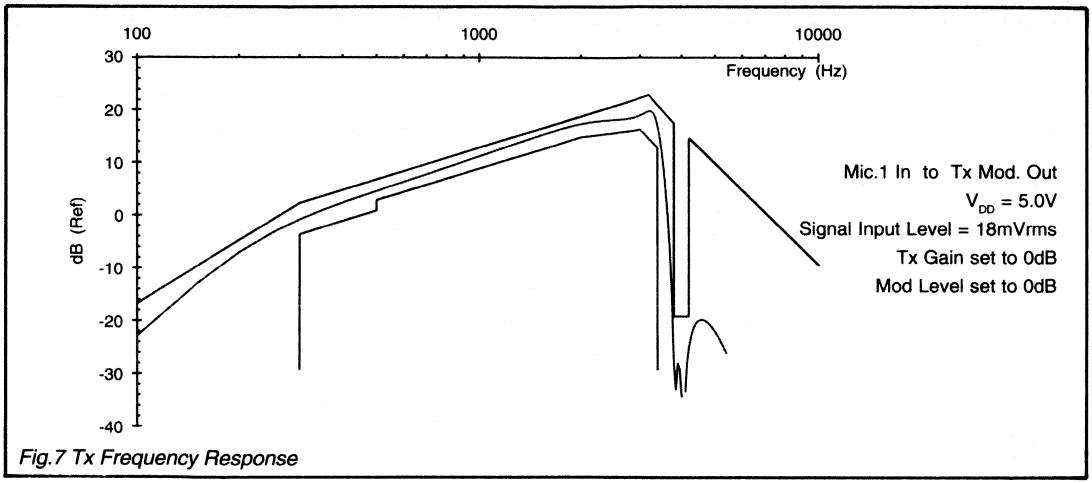



*Fig.7 Tx Frequency Response*

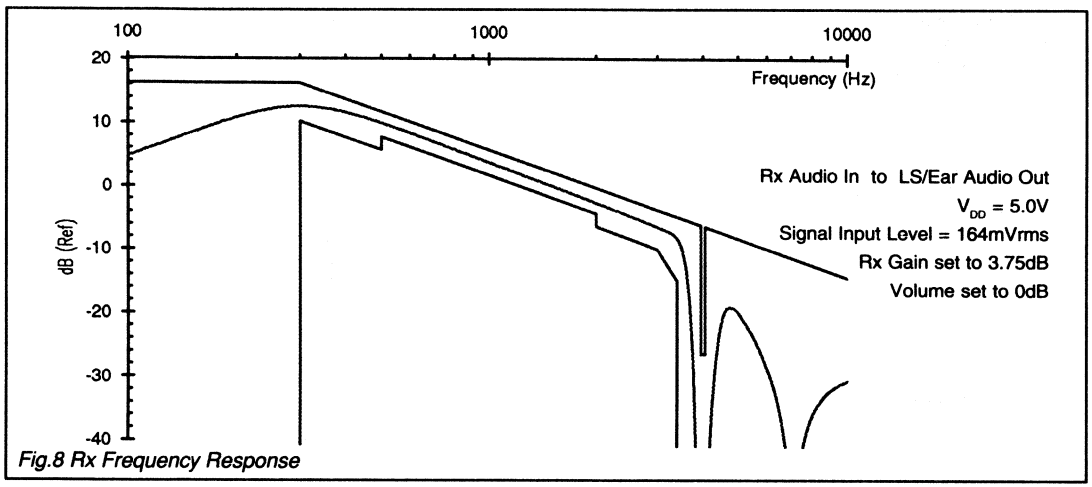



*Fig.8 Rx Frequency Response*

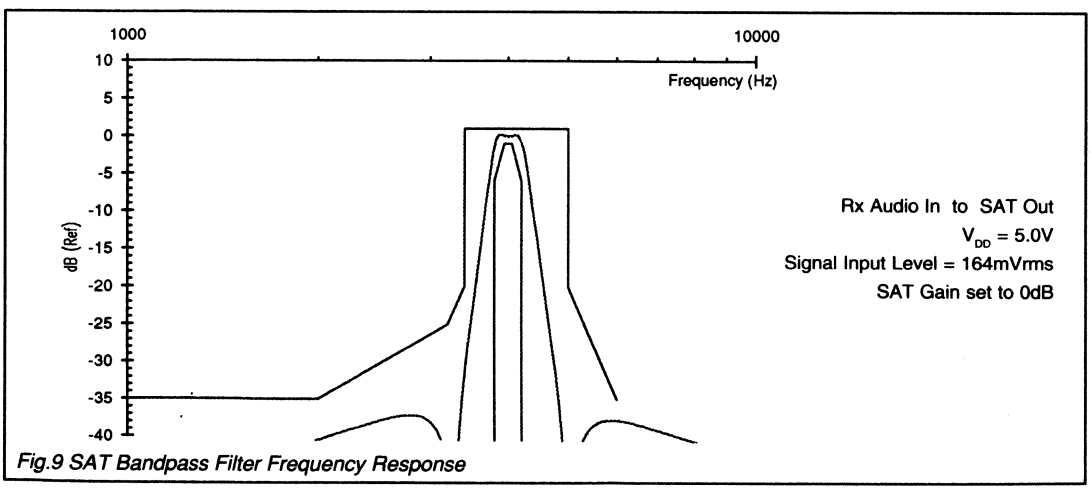



*Fig.9 SAT Bandpass Filter Frequency Response*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref. $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX816DW** | -40°C to +85°C (plastic) |
| | **FX816J** | -40°C to +85°C (cerdip) |
| Storage temperature range: | **FX816DW** | -40°C to +85°C (plastic) |
| | **FX816J** | -55°C to +125°C (cerdip) |

**Operating Limits**

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.032MHz. Audio level 0dB ref. = 164mV rms @ 1.0kHz.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | | | | |
| All Operating | | – | 6.0 | – | mA |
| Rx Data Mode | 1 | – | 1.0 | – | mA |
| Powersave All | | – | 0.6 | – | mA |
| Alias Frequency | | – | 63.0 | – | kHz |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | – | – | MΩ |
| $R_{OUT}$ | | – | 10.0 | – | kΩ |
| Inverter d.c. Voltage Gain | | – | 10.0 | – | V/V |
| Gain/Bandwidth Product | | – | 10.0 | – | MHz |
| **Analogue Input Impedances** | | | | | |
| Mic.1 & 2 | | – | 500 | – | kΩ |
| FFSK/Play | | – | 500 | – | kΩ |
| Comp In | | – | 500 | – | kΩ |
| DTMF In | | – | 500 | – | kΩ |
| Dev. Limiter In | | – | 100 | – | kΩ |
| (Expanded) Audio In | | – | 47.0 | – | kΩ |
| Tx Mix In | | – | 100 | – | kΩ |
| Rx Audio In | | – | 100 | – | kΩ |
| **Analogue Output Impedances** | | | | | |
| Pre-Emp Out | | – | 1.4 | – | kΩ |
| Tx Mod Out | | – | 600 | – | Ω |
| Expand/Store | | – | 600 | – | Ω |
| LS and Ear Audio | | – | 1.0 | – | kΩ |
| FFSK Data Out | | – | 600 | – | Ω |
| SAT Out | | – | 10.0 | – | kΩ |
| Tx Filter Out | | – | 600 | – | Ω |
| VOGAD | | – | 500 | – | Ω |
| Switches – ON | | – | 1.0 | – | kΩ |
| – OFF | | 10.0 | – | – | MΩ |
| **Control Interface Parameters** | | | | | |
| Input Logic Levels | | | | | |
| Logic "1" | 2 | 3.5 | – | – | V |
| Logic "0" | 2 | – | – | 1.5 | V |
| $I_{IN}$ (logic "1" or "0") | 2 | -1.0 | – | 1.0 | µA |
| Input Capacitance | 2 | – | – | 7.5 | pF |
| **Channel Performances** | | | | | |
| **Tx Path** | | | | | |
| **Analogue Signal Input Levels** | | | | | |
| Mic. 1 and 2 | 3 | – | -11.0 | – | dB |
| FFSK/Play | 3 | – | -11.0 | – | dB |
| DTMF | 3 | – | -11.0 | – | dB |
| Comp. In | 3 | – | -11.0 | – | dB |
| Tx Mix In | 3 | – | 0 | – | dB |

# Specification .....

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Analogue Signal Output Levels** | | | | | |
| Pre-Emp Out | 3 | – | 0 | – | dB |
| Tx Filter Out | 3 | – | 0 | – | dB |
| Tx Mod Out | 3 | – | 0 | – | dB |
| Sidetone Out | 3 | – | -11.0 | – | dB |
| **Path Gains/Levels** | | | | | |
| **Tx Gain – $11_H$** | | | | | |
| Nominal Adjustment Range | | -2.65 | – | 3.65 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |
| **VOGAD** | | | | | |
| Gain (Non-Compressing) | | – | 11.0 | – | dB |
| (Full Compressing) | | – | -34.0 | – | dB |
| Attack Time | 4 | – | 3.0 | – | ms |
| **Dev Limiter** | | | | | |
| Threshold | | – | 713 | – | mVp-p |
| Symmetry | | – | 7.0 | – | % |
| **Mod Level Attenuation – $11_H$** | | | | | |
| Nominal Adjustment Range | | -5.6 | | 0 | dB |
| Step Size | | 0.2 | 0.4 | 0.6 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| **Overall** | | | | | |
| Tx Distortion | | – | -40.0 | -32.0 | dBp |
| Tx Hum and Noise | | – | -40.0 | -20.0 | dB |
| **Rx Signal Path** | | | | | |
| Rx Audio Input Level | 3 | – | -7.0 | – | dB |
| LS/Ear Audio Output Level | 3 | – | 0 | – | dB |
| **Path Gains/Levels** | | | | | |
| **Rx Gain – $12_H$** | | | | | |
| Nominal Adjustment Range | | 3.75 | | 9.70 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |
| **FFSK Output** | | | | | |
| Frequency Range | | 900 | – | 2100 | Hz |
| Gain at 1kHz | | -1.0 | 0 | 1.0 | dB |
| Response | | – | 6.0 | – | db/oct |
| **Volume – $12_H$** | | | | | |
| Nominal Adjustment Range | | -28.0 | | 0 | dB |
| Step Size | | 1.5 | 2.0 | 2.5 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| **Overall** | | | | | |
| Rx Distortion | | – | -40.0 | -32.0 | dBp |
| Rx Hum and Noise | | – | -40.0 | -34.0 | dB |
| **SAT Signal Path** | | | | | |
| **Bandpass Filter** | | | | | |
| Frequency Range | | 3945 | | 4055 | Hz |
| Gain | | -0.5 | – | 1.5 | dB |
| SAT Level – $13_H$ | | | | | |
| Nominal Adjustment Range | | -1.95 | | 3.50 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |

**Notes**

1. With reference to the Powersave Command and Figure 3, all functions with the exception of the Rx Gain Element may be powersaved. This will still allow signalling data through the FX816 to activate the system via the µProcessor.
2. Serial Clock, Command Data and Chip Select inputs.
3. Levels equivalent to ±3.0kHz deviation with the settings below:

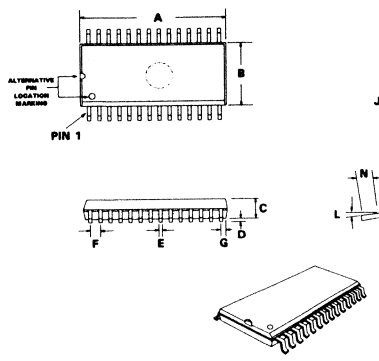
   *Tx Gain = 0dB* *Mod Level = 0dB*
   *Rx Gain = 7.05dB* *Volume = 0dB*
   *SAT Level = 0dB*

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.
4. Using the components shown in Figure 2.

## Package Outline

The FX816DW Small Outline Integrated Circuit is shown in Figure 10 and the "J" version in Figure 11. Pin 1 identification marking is shown on the relevant diagram.
Pins on both package styles number anti-clockwise when viewed from the top (marked side).

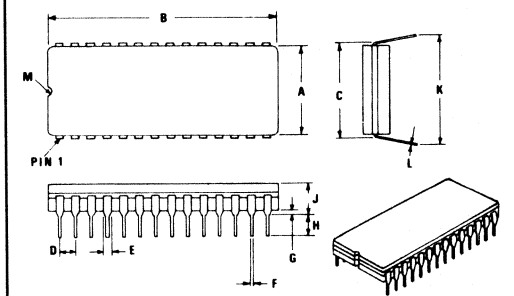
*Fig.10* ***FX816DW*** *28-pin S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 18.05 | | 17.70 | G | | 0.66 | |
| B | 7.65 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.11* ***FX816J*** *28-pin DIL Package*




All dimensions in mm Angles in degrees

| DIMENSION | MAX | MIN | DIMENSION | MAX | MIN |
|---|---|---|---|---|---|
| A | 13.36 | 13.06 | G | 1.40 | TYPICAL |
| B | 37.05 | 36.58 | H | 4.30 | 4.10 |
| C | 15.70 | 15.50 | J | 5.57 | 4.49 |
| D | 2.54 | TYPICAL | K | 17.00 | TYPICAL |
| E | 1.39 | TYPICAL | L | 0.25 | TYPICAL |
| F | 0.45 | TYPICAL | M | 0.64R | TYPICAL |

## Handling Precautions

The FX816 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

## Ordering Information

**FX816DW** 28-pin plastic S.O.I.C.

**FX816J** 28-pin cerdip DIL

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX826 AMPS/TACS System Audio Processor

Publication D/826/2 February 1993
Provisional Issue

## Features

- **Full-Duplex Audio Processing for AMPS & TACS Cellular Systems**
- **On-Chip Speech and SAT Facilities**
  **– Tx/Rx Filtering & Gain – SAT Channel Pre-/De-Emphasis – Deviation Limiter –**
- **Serial µProcessor Interface**
- **Separate SAT Channel**
- **"Sidetone" Output Available**
- **HandsFree Compatibility**
- **Access to External Processes**
  ***– Compression – Expansion – Signalling – VSR Codec (Store/Play) –***
- **Powersave (Low-Current) Settings**

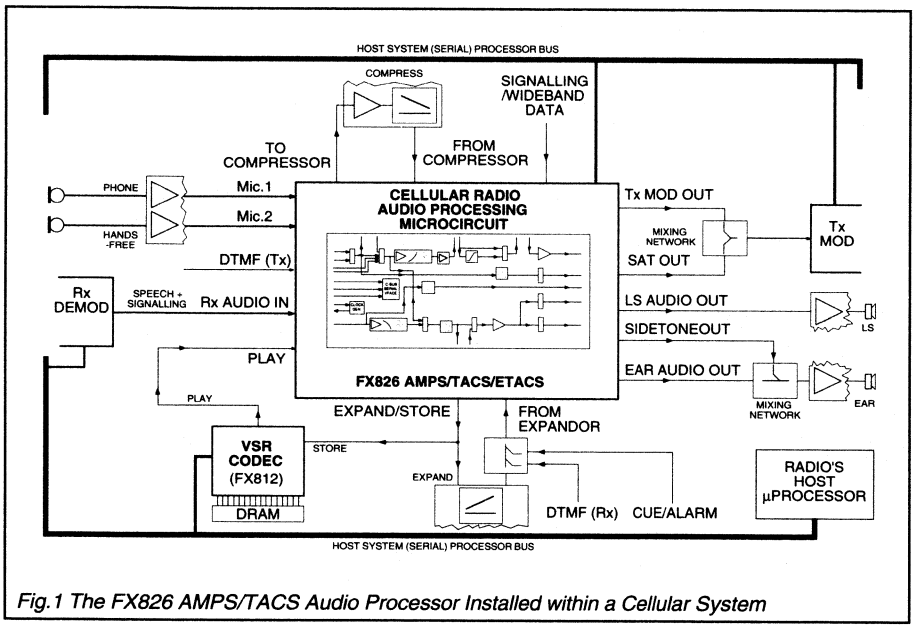



*Fig.1 The FX826 AMPS/TACS Audio Processor Installed within a Cellular System*

**FX826**

## Brief Description

The FX826 is a µProcessor controlled full-duplex audio processor on a single-chip with separate Tx and Rx paths to provide all the filter/gain/limiting functions necessary to pre-process audio, wideband-data and signalling in cellular communications systems using the AMPS or TACS/ETACS/JTACS specifications.

Selectable inputs available to the transmit path are: a choice of two microphones and DTMF/signalling, with access, in this path, to external compression circuitry. Operationally the Tx path provides input gain/filtering, a deviation limiter and Tx Modulation Drive controls.

In the Rx path the SAT signal is separated from the incoming audio via a filter block and made available at a separate pin for mixing externally with the Tx Modulation Drive.

The Rx path consists of an input gain/filter block for voice, inputs from an external audio expansion system and an output gain control driving either a loudspeaker system or earpiece.

Unique to the FX816/826/836 cellular audio processors is the ability to route audio (Tx or Rx) to an external Voice Store and Retrieve (VSR) device such as the FX802 or FX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

The FX826, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

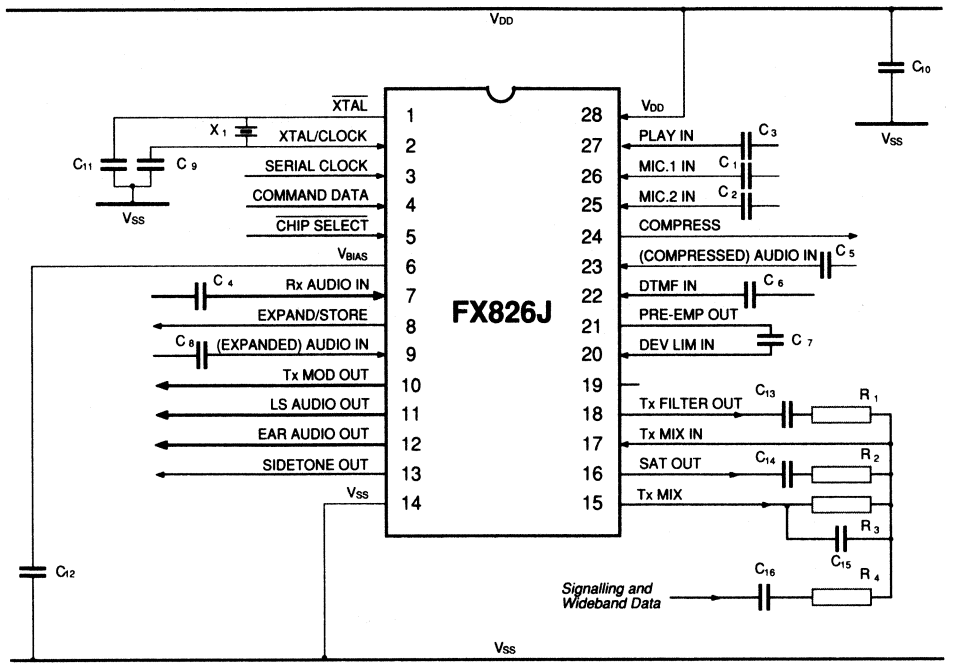
## Pin Number Function

| FX826DW | FX826J | |
|---|---|---|
| 1 | 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. |
| 2 | 2 | **Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock ($f_{XTAL}$) should be connected here. Note that operation of the FX826 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes). |
| 3 | 3 | **Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the FX826. See Timing Diagrams. |
| 4 | 4 | **Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the FX826 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams. |
| 5 | 5 | **Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams. |
| 6 | 6 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$. See Figure 2. |
| 7 | 7 | **Rx Audio In:** Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to $V_{BIAS}$ and requires to be connected via a capacitor. |
| 8 | 8 | **Expand/Store:** A common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the FX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3. |
| 9 | 9 | **(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to $V_{BIAS}$ and requires to be connected via a capacitor. See Figures 2 and 3. |
| 10 | 10 | **Tx Mod Out:** The composite Tx audio output to the transmitter modulator from a variable attenuation stage ($11_H$). This output is set to $V_{BIAS}$ via an internal 1MΩ resistor when set to Powersave or OFF. |
| 11 | 11 | **LS Audio Out:** An audio output of the Rx path (or selected audios, see Figure 3) for a loudspeaker system. This is available for handsfree operation. This output can be connected to $V_{BIAS}$ when not required, by SW6 (Configuration Command ($10_H$)). A driver amplifier may be required. |
| 12 | 12 | **Ear Audio Out:** An audio output of the Rx path (or selected audios), available as an output for a handset earpiece. This output, in parallel with the LS Audio Out function, can be connected to $V_{BIAS}$ when not required, by SW7 (Configuration Command ($10_H$)). A driver amplifier may be required. |
| 13 | 13 | **Sidetone:** A switched "sidetone" from the microphone inputs made available for mixing externally with the "Ear" audio. See Figure 3. |
| 14 | 14 | **$V_{SS}$:** Negative supply rail. Signal ground. |
| | | ***Notes on Inputs:*** *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.* |

## Pin Number Function

| FX826DW | FX826J | |
|---|---|---|
| 15 | 15 | **Tx Mix:** The output of the Tx Mix Amplifier. Used with external components, it allows the Tx Filter Out output to mix with externally generated signalling tones prior to the final level adjustment. |
| 16 | 16 | **SAT Out:** The output of the SAT Bandpass filter. This level is recovered from the input Rx audio and is available for mixing externally with the transmitter modulation. See Figure 3. |
| 17 | 17 | **Tx Mix In:** The input to the Tx Mix Amplifier. Used with external components, it allows the Tx Filter Out output to mix with externally generated signalling tones prior to the final level adjustment. The recovered SAT signal may be introduced at this point. See Figures 2 and 3. |
| 18 | 18 | **Tx Filter Out:** The output of the Deviation Limiter/Lowpass Filter stage. This stage can be by-passed using SW3 (Configuration Command). See Figure 3. |
| 19 | 19 | No internal connection – Leave open circuit. |
| 20 | 20 | **Deviation Limiter In:** Input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve maximum possible symmetry of limiting as this input has a 1MΩ internal resistor to $V_{BIAS}$. See Figure 2. |
| 21 | 21 | **Pre-Emphasis Out:** Audio output from the Tx Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 & 3. |
| 22 | 22 | **DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the Tx Path, controlled by SW2 (Configuration Command ($10_H$)). This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 23 | 23 | **Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 24 | 24 | **Compression:** The output to an external audio compression system. Currently available compressor/ expanders have Op-Amps incorporated. The compressor can be by-passed by SW2. |
| 25 | 25 | **Mic.2 In:** Tx voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any Tx audio input. Pre-amplification may be required at these inputs. These inputs each have an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 26 | 26 | **Mic.1 In:** |
| 27 | 27 | **Play In:** The input via SW2 from a voice storage device such as the FX812. This "replayed" audio can be sent to Rx or Tx paths allowing a Messaging/Voice Notepad/Answering facility. This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 28 | 28 | $V_{DD}$: Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this Audio Processor are dependent upon this supply. |
| | | ***"C-BUS"** is CML's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController. For further details refer to CML Publication No. D/µINT/1 June 1991.* |

# Application Information




| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $R_1$ | = | 100kΩ | $C_3$ | = | 100nF | $C_8$ | = | 100nF | $C_{13}$ | = | 100nF |
| $R_2$ | | as required | $C_4$ | | 100nF | $C_9$ | | 33pF | $C_{14}$ | | 100nF |
| $R_3$ | | 100kΩ | $C_5$ | | 100nF | $C_{10}$ | | 100nF | $C_{15}$ | | 100pF |
| $R_4$ | | as required | $C_6$ | | 100nF | $C_{11}$ | | 33pF | $C_{16}$ | | 100nF |
| $C_1$ | | 100nF | $C_7$ | | 100nF | $C_{12}$ | | 1.0µF | $X_1$ | | 4.000MHz |
| $C_2$ | | 100nF | | | | | | | | | |

**Tolerances** – Capacitors ±20%

*Fig.2 Recommended External Components*

## Notes

1. **Xtal/clock operation**
Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast-reaction fuse).

2. **SAT Output**
It is possible, due to the impedance of this output, that an external buffer amplifier is required when interfacing or mixing with other cellular system sections.

3. **Tx Mix Gain**
The value of $R_4$ should be chosen with $R_3/C_{15}$ so as to provide the required gain.

## AMPS/TACS Cellular System Interfaces

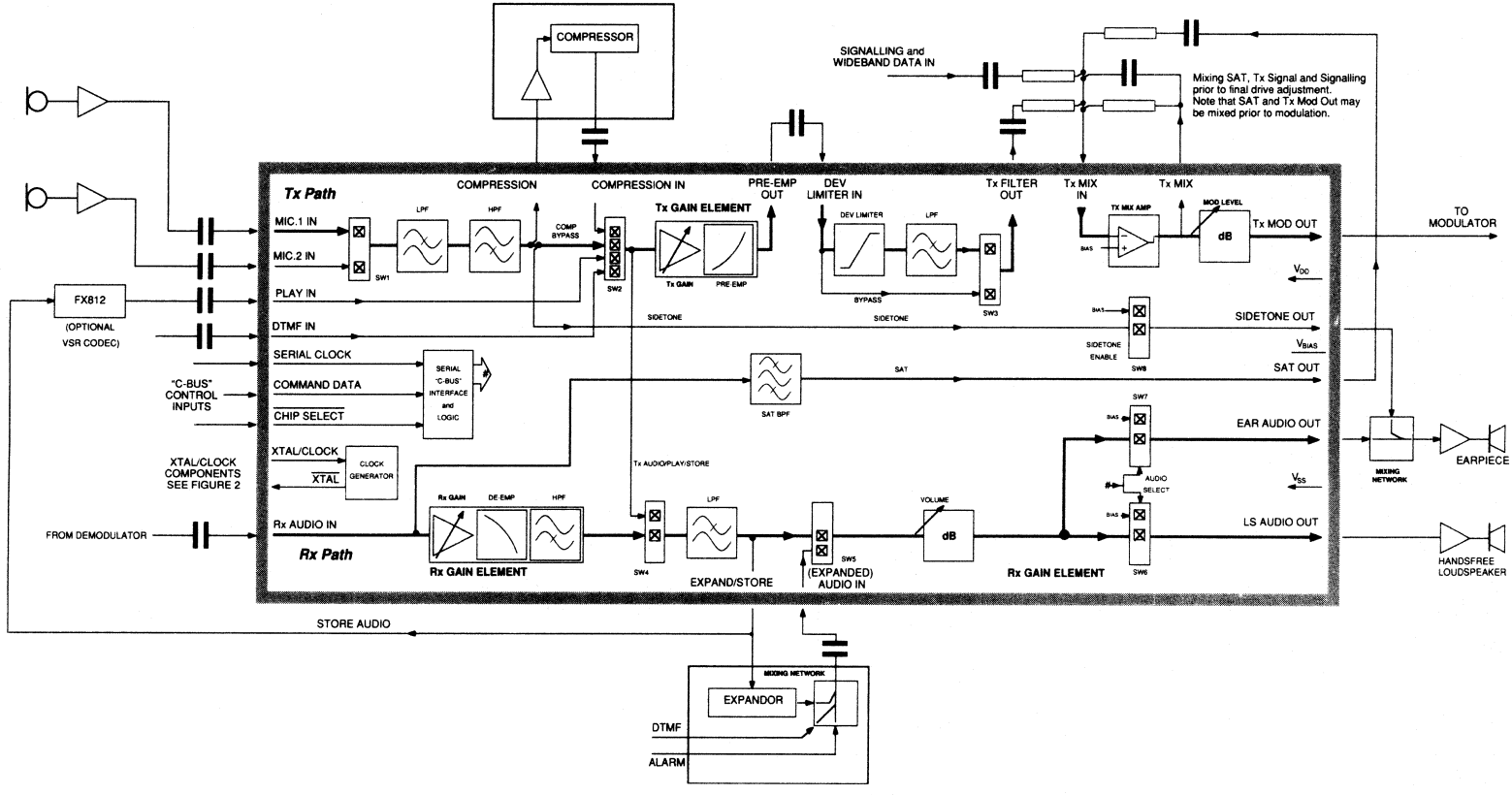



*Fig.3 The FX826 Internal and External Signal Paths within a TACS Cellular Radio System*

# The Controlling System

## "C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

---

Control of the functions and levels within the FX826 AMPS and TACS Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device. The use of these instructions is detailed in the following paragraphs and tables.

| Command Assignment | Address/Command (A/C) Byte Hex | Binary MSB LSB | | Command Data | Table |
|---|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | | |
| Configuration Command | 10 | 0 0 0 1 0 0 0 0 | + | 1 byte | 2 |
| Tx Gain & Mod. Command | 11 | 0 0 0 1 0 0 0 1 | + | 1 byte | 3 |
| Rx Gain & Vol. Command | 12 | 0 0 0 1 0 0 1 0 | + | 1 byte | 4 |
| Powersave Command | 13 | 0 0 0 1 0 0 1 1 | + | 1 byte | 5 |

*Table 1 "C-Bus" Address/Commands*

In "C-BUS" protocol the audio processor is allocated Address/Command (A/C) values $10_H$ to $13_H$. Configuration, Tx/Rx Gains and Powersave assignments and data requirements are given in Table 1.
Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams Figures 5 and 6.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A **General Reset Command ($01_H$)** will be required to set all FX826 registers to $00_H$.

## Configuration Command *(Preceded by A/C $10_H$)*

| Setting | | Control Bits |
|---|---|---|
| ***MSB*** | | ***Transmitted First*** |
| ***Bit 7*** | | **Sw8 Sidetone** |
| 0 | | Sidetone Bias |
| 1 | | Sidetone Enabled |
| ***6*** | | **Sw6/7 Rx Audio** |
| 0 | | Ear Enabled, LS Bias |
| 1 | | LS Enabled, Ear Bias |
| ***5*** | | **Sw5 Expandor** |
| 0 | | Expandor By-Pass |
| 1 | | Expandor Route |
| ***4*** | | **Sw4 Tx/Rx Audio** |
| 0 | | Tx Store/Audio |
| 1 | | Rx Store/Audio |
| ***3*** | | **Sw3 Dev. Limiter** |
| 0 | | Dev. Limiter By-Pass |
| 1 | | Dev. Limiter Route |
| ***2*** | | **Sw1 Mic. Inputs** |
| 0 | | Mic. 1 Input |
| 1 | | Mic.2 Input |
| ***1*** | ***0*** | **Sw2 Tx Function** |
| 0 | 0 | DTMF In |
| 0 | 1 | Compressor By-Pass |
| 1 | 0 | Compressor In |
| 1 | 1 | Play In |

*Table 2 Configuration Commands*

## Tx Gain & Mod. Command *(Preceded by A/C $11_H$)*

| Setting | | | | Gain (dBs) |
|---|---|---|---|---|
| ***MSB*** | | | | ***Transmitted First*** |
| ***7*** | ***6*** | ***5*** | ***4*** | **Tx Mod. Level** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -5.6 |
| 0 | 0 | 1 | 0 | -5.2 |
| 0 | 0 | 1 | 1 | -4.8 |
| 0 | 1 | 0 | 0 | -4.4 |
| 0 | 1 | 0 | 1 | -4.0 |
| 0 | 1 | 1 | 0 | -3.6 |
| 0 | 1 | 1 | 1 | -3.2 |
| 1 | 0 | 0 | 0 | -2.8 |
| 1 | 0 | 0 | 1 | -2.4 |
| 1 | 0 | 1 | 0 | -2.0 |
| 1 | 0 | 1 | 1 | -1.6 |
| 1 | 1 | 0 | 0 | -1.2 |
| 1 | 1 | 0 | 1 | -0.8 |
| 1 | 1 | 1 | 0 | -0.4 |
| 1 | 1 | 1 | 1 | 0 |
| ***3*** | ***2*** | ***1*** | ***0*** | **Tx Input Gain** |
| 0 | 0 | 0 | 0 | -2.65 |
| 0 | 0 | 0 | 1 | -2.05 |
| 0 | 0 | 1 | 0 | -1.50 |
| 0 | 0 | 1 | 1 | -0.95 |
| 0 | 1 | 0 | 0 | -0.45 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0.45 |
| 0 | 1 | 1 | 1 | 0.85 |
| 1 | 0 | 0 | 0 | 1.25 |
| 1 | 0 | 0 | 1 | 1.65 |
| 1 | 0 | 1 | 0 | 2.05 |
| 1 | 0 | 1 | 1 | 2.40 |
| 1 | 1 | 0 | 0 | 2.70 |
| 1 | 1 | 0 | 1 | 3.05 |
| 1 | 1 | 1 | 0 | 3.35 |
| 1 | 1 | 1 | 1 | 3.65 |

*Table 3 Tx Gain & Mod. Commands*

# The Controlling System .....

## Rx Gain & Vol. Command *(Preceded by A/C $12_H$)*

| Setting | | | | Gain (dBs) |
|---|---|---|---|---|
| *MSB* | | | | |
| *7* | *6* | *5* | *4* | ***Transmitted First*** |
| | | | | **Rx Volume** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -28.0 |
| 0 | 0 | 1 | 0 | -26.0 |
| 0 | 0 | 1 | 1 | -24.0 |
| 0 | 1 | 0 | 0 | -22.0 |
| 0 | 1 | 0 | 1 | -20.0 |
| 0 | 1 | 1 | 0 | -18.0 |
| 0 | 1 | 1 | 1 | -16.0 |
| 1 | 0 | 0 | 0 | -14.0 |
| 1 | 0 | 0 | 1 | -12.0 |
| 1 | 0 | 1 | 0 | -10.0 |
| 1 | 0 | 1 | 1 | -8.0 |
| 1 | 1 | 0 | 0 | -6.0 |
| 1 | 1 | 0 | 1 | -4.0 |
| 1 | 1 | 1 | 0 | -2.0 |
| 1 | 1 | 1 | 1 | 0 |
| ***3*** | ***2*** | ***1*** | ***0*** | **Rx Input Gain** |
| 0 | 0 | 0 | 0 | 3.75 |
| 0 | 0 | 0 | 1 | 4.30 |
| 0 | 0 | 1 | 0 | 4.80 |
| 0 | 0 | 1 | 1 | 5.30 |
| 0 | 1 | 0 | 0 | 5.80 |
| 0 | 1 | 0 | 1 | 6.20 |
| 0 | 1 | 1 | 0 | 6.55 |
| 0 | 1 | 1 | 1 | 7.05 |
| 1 | 0 | 0 | 0 | 7.40 |
| 1 | 0 | 0 | 1 | 7.80 |
| 1 | 0 | 1 | 0 | 8.15 |
| 1 | 0 | 1 | 1 | 8.50 |
| 1 | 1 | 0 | 0 | 8.80 |
| 1 | 1 | 0 | 1 | 9.10 |
| 1 | 1 | 1 | 0 | 9.40 |
| 1 | 1 | 1 | 1 | 9.70 |

*Table 4 Rx Gain and Vol. Commands*

## Powersave Command *(Preceded by A/C $13_H$)*

| Setting | | | | | | | Control Bits |
|---|---|---|---|---|---|---|---|
| *MSB* | | | | | | | |
| *Bit 7* | | | | | | | ***Transmitted First*** |
| *7* | *6* | *5* | *4* | *3* | *2* | *1* | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | All must be a logic "0" |
| | | | ***0*** | | | | **Powersave Setting** |
| | | | 0 | | | | Powersave FX826 |
| | | | 1 | | | | Enable FX826 |

*Table 5 Powersave Command*

## Reference Signal Levels

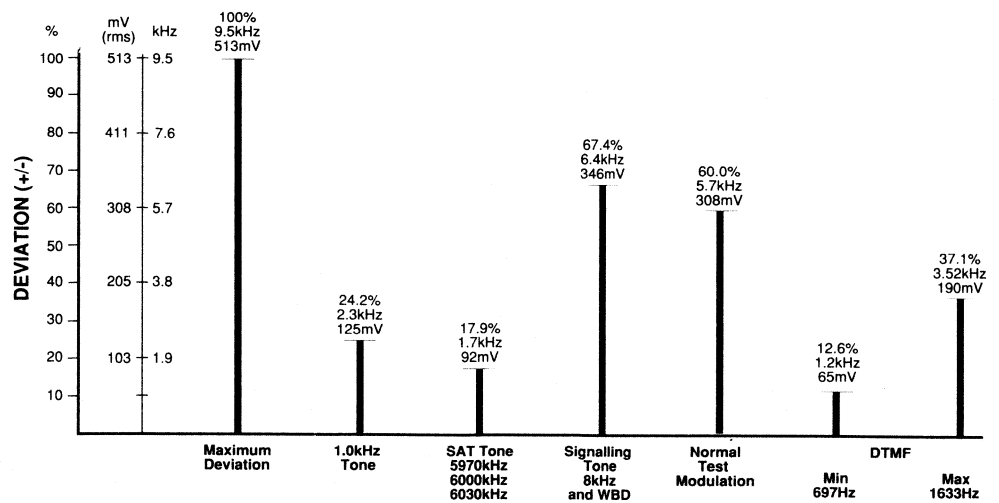



*Fig.4 TACS Signal Deviation Levels and corresponding **Tx Mod Outputs** with the Mod Level set to 0dB*

# Control Timing Information

Timing Specification – Figures 5 and 6.

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CSE}$ | "CS-Enable to Clock-High" | 1 | 2.0 | – | – | µs |
| $t_{CSH}$ | Last "Clock-High to CS-High" | 1 | 4.0 | – | – | µs |
| $t_{CSOFF}$ | "CS-High" Time between transactions | 1, 2 | 2.0 | – | – | µs |
| $t_{CK}$ | "Clock-Cycle" Time | 1 | 2.0 | – | – | µs |
| $t_{NXT}$ | "Inter-Byte" Time | 1 | 4.0 | – | – | µs |
| $t_{CH}$ | "Serial Clock-High" Period | | 500 | – | – | ns |
| $t_{CL}$ | "Serial Clock-Low" Period | | 500 | – | – | ns |
| $t_{CDS}$ | "Command Data Set-Up" Time | | 250 | – | – | ns |
| $t_{CDH}$ | "Command Data Hold" Time | | 0 | – | – | ns |

**Notes**

1. These Minimum Timing values are altered during operation of the FX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

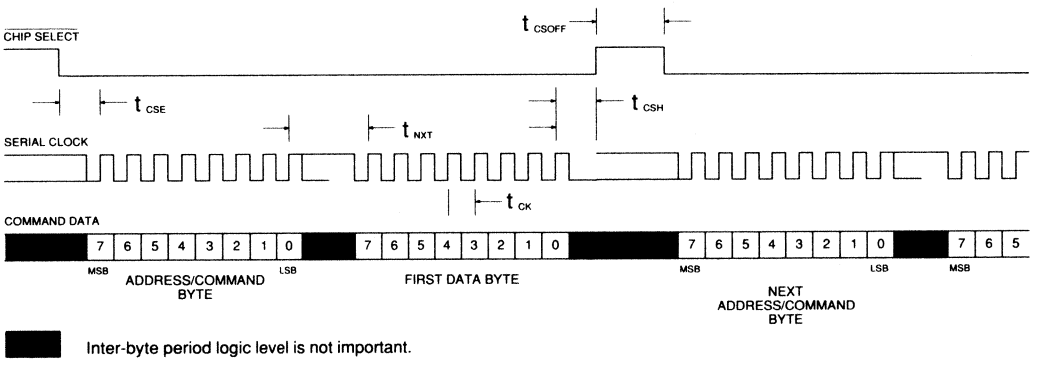



*Fig.5 Control Timing Information*

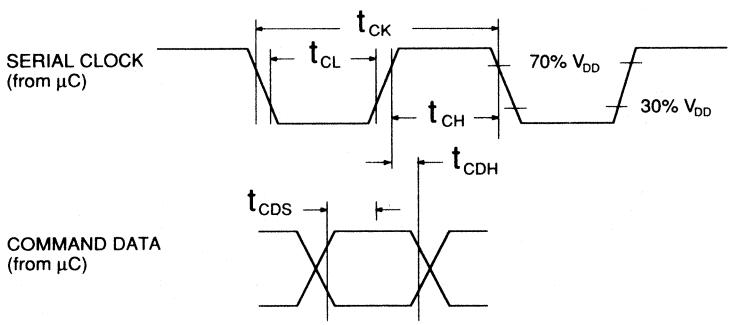



*Fig.6 Control Timing Relationships*

# Frequency Responses

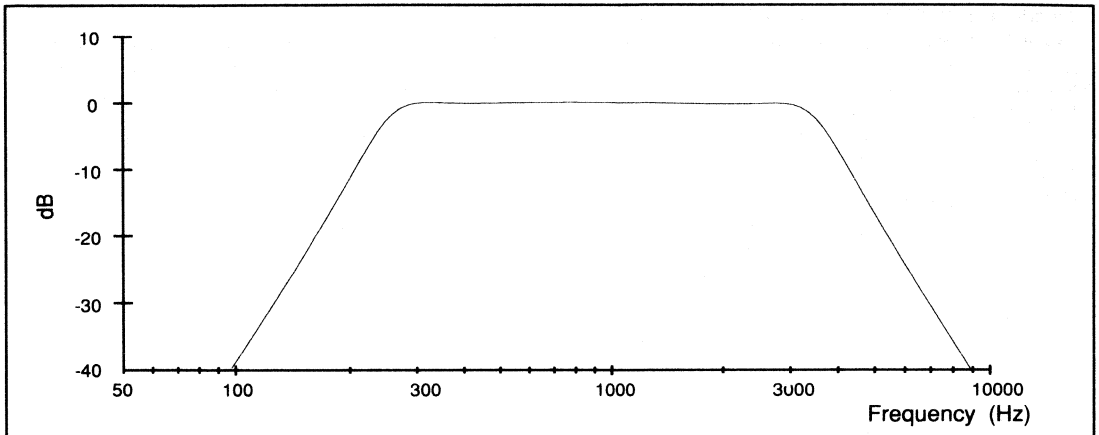



*Fig.7 Microphone Input Stages -Combined Low and Highpass Filter Frequency Response*

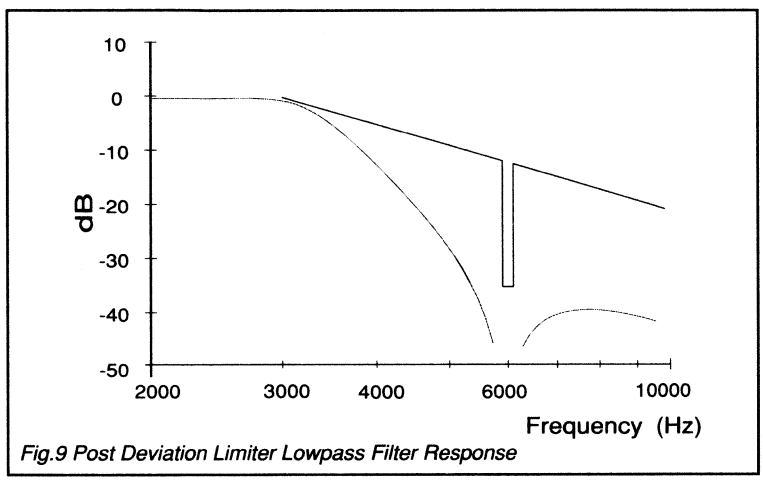



*Fig.9 Post Deviation Limiter Lowpass Filter Response*

**Figure 7**
**Mic.1/2 In to Compression Out**

$V_{DD}$ = 5.0V

Signal Input Level = 55.0mVrms

**Figure 8**
**Dev Limiter In to Tx Filter Out**

$V_{DD}$ = 5.0V

Signal Input Level = 55.0mVrms

**Figure 9**

**Rx Audio In to SAT out**

$V_{DD}$ = 5.0V

Signal Input Level = 100mVrms

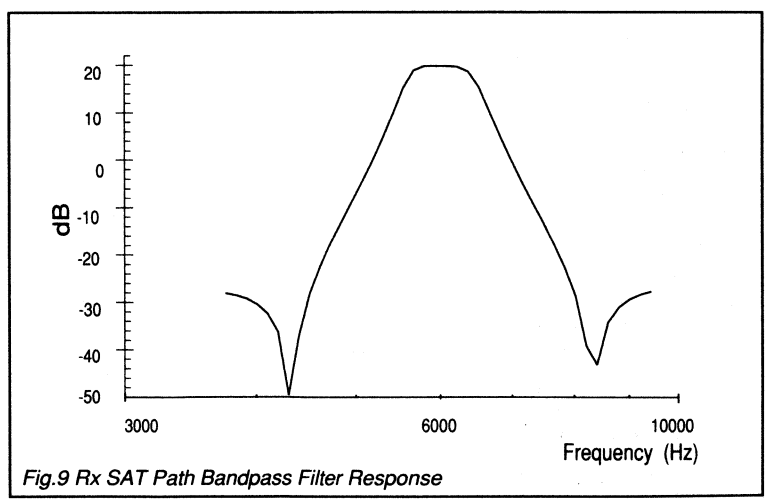



*Fig.9 Rx SAT Path Bandpass Filter Response*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref. $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX826DW** | -40°C to +85°C (plastic) |
| | **FX826J** | -40°C to +85°C (cerdip) |
| Storage temperature range: | **FX826DW** | -40°C to +85°C (plastic) |
| | **FX826J** | -55°C to +125°C (cerdip) |

**Operating Limits**

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.000MHz. Audio level 0dB ref. = 308mV rms @ 1.0kHz.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | | | | |
| Operating | | – | 6.5 | – | mA |
| Powersave | | – | 0.5 | – | mA |
| Alias Frequency | | – | 63.0 | – | kHz |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | – | – | MΩ |
| $R_{OUT}$ | | – | 10.0 | – | kΩ |
| Inverter d.c. Voltage Gain | | – | 10.0 | – | V/V |
| Gain/Bandwidth Product | | – | 10.0 | – | MHz |
| Tx Mix Amp (Open Loop Gain) | | – | 50.0 | – | dB |
| (Bandwidth) | | 20.0 | – | – | kHz |
| **Analogue Input Impedances** | | | | | |
| Mic.1 & 2 | | – | 500 | – | kΩ |
| Play | | – | 500 | – | kΩ |
| Comp In | | – | 500 | – | kΩ |
| DTMF In | | – | 500 | – | kΩ |
| Dev. Limiter In | | – | 100 | – | kΩ |
| (Expanded) Audio In | | – | 47.0 | – | kΩ |
| Tx Mix In | | 10.0 | – | – | MΩ |
| Rx Audio In | | – | 100 | – | kΩ |
| **Analogue Output Impedances** | | | | | |
| Pre-Emp Out | | – | 600 | – | Ω |
| Tx Mod Out | | – | 600 | – | Ω |
| Expand/Store | | – | 600 | – | Ω |
| LS and Ear Audio | | – | 1.0 | – | kΩ |
| SAT Out | 3 | – | 1.0 | – | kΩ |
| Tx Filter Out | | – | 600 | – | Ω |
| Comp Out | | – | 600 | – | Ω |
| Sidetone Out | | – | 2.0 | – | kΩ |
| Tx Mix (Open Loop) | | – | 6.0 | – | kΩ |
| (Closed Loop) | | – | 600 | – | Ω |
| Switches – ON | | – | 1.0 | – | kΩ |
| – OFF | | 10.0 | – | – | MΩ |
| **Control Interface Parameters** | | | | | |
| Input Logic Levels | | | | | |
| Logic "1" | 1 | 3.5 | – | – | V |
| Logic "0" | 1 | – | – | 1.5 | V |
| $I_{IN}$ (logic "1" or "0") | 1 | -1.0 | – | 1.0 | µA |
| Input Capacitance | 1 | – | – | 7.5 | pF |
| **Channel Performances** | | | | | |
| **Tx Path** | | | | | |
| **Filter Specifications** | | | | | |
| **Pre-Compression L/HPF Combination** | | | | | |
| Passband | | 300 | | 3000 | Hz |
| Slope - below 300Hz | | +24.0 | – | – | dB/oct. |
| above 3000Hz | | -24.0 | – | – | dB/oct. |
| **Tx Gain Pre-Emphasis** | | | | | |
| Gain at 1.0kHz | | – | 0 | – | dB |
| Slope (300Hz - 3000Hz) | | – | 6.0 | – | dB/oct. |

# Specification .....

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Post Deviation Limiter LPF** | | | | | |
| Attenuation Relative to 1.0kHz | 3.0kHz - 5.9kHz | | 40 log(f/3000) | | dB |
| | 5.9kHz - 6.1kHz | | 35.0 | | dB |
| | 6.1kHz - 15kHz | | 40 log(f/3000) | | dB |
| | >15kHz | | 28.0 | | dB |
| **Analogue Signal Input Levels** | | | | | |
| Mic. 1 and 2 | 2 | – | 0 | – | dB |
| Play | 2 | – | 0 | – | dB |
| DTMF | 2 | – | 0 | – | dB |
| Comp. In | 2 | – | 0 | – | dB |
| Tx Mix In | 2 | – | 0 | – | dB |
| **Analogue Signal Output Levels** | | | | | |
| Pre-Emp Out | 2 | – | 0 | – | dB |
| Tx Filter Out | 2 | – | 0 | – | dB |
| Tx Mod Out | 2 | – | 0 | – | dB |
| Sidetone Out | 2 | – | 0 | – | dB |
| **Path Gains/Levels** | | | | | |
| **Tx Gain – $11_H$** | | | | | |
| Nominal Adjustment Range | | -2.65 | – | 3.65 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |
| **Dev Limiter** | | | | | |
| Threshold | | – | 1086 | – | mVp-p |
| Symmetry | | – | 7.0 | – | % |
| **Mod Level Attenuation – $11_H$** | | | | | |
| Nominal Adjustment Range | | -5.6 | | 0 | dB |
| Step Size | | 0.2 | 0.4 | 0.6 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| **Overall** | | | | | |
| Tx Distortion | | – | -40.0 | -32.0 | dBp |
| Tx Hum and Noise | | – | -40.0 | -20.0 | dB |
| **Rx Signal Path** | | | | | |
| **Filter Specifications** | | | | | |
| **Rx Gain De-Emphasis** | | | | | |
| Gain at 1.0kHz | | – | 3.75 | – | dB |
| Slope (300Hz - 3000Hz) | | – | -6.0 | – | dB/oct. |
| **Rx Channel Bandpass** | | 300 | | 3000 | Hz |
| Slope - below 300Hz | | +24.0 | – | – | dB/oct. |
| above 3000Hz | | -36.0 | – | – | dB/oct. |
| **Analogue Signal Levels** | | | | | |
| Rx Audio Input Level | 2 | – | -7.0 | – | dB |
| LS/Ear Audio Output Level | 2 | – | 0 | – | dB |
| **Path Gains/Levels** | | | | | |
| **Rx Gain – $12_H$** | | | | | |
| Nominal Adjustment Range | | 3.75 | | 9.70 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |
| **Volume – $12_H$** | | | | | |
| Nominal Adjustment Range | | -28.0 | | 0 | dB |
| Step Size | | 1.5 | 2.0 | 2.5 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| **Overall** | | | | | |
| Rx Distortion | | – | -40.0 | -32.0 | dBp |
| Rx Hum and Noise | | – | -40.0 | -34.0 | dB |
| **SAT Signal Path** | | | | | |
| **Bandpass Filter** | | | | | |
| Frequency Range | | 5970 | | 6030 | Hz |
| Gain | | 19.0 | 20.0 | 21.0 | dB |

**Notes**

1. Serial Clock, Command Data and Chip Select inputs.
2. Levels equivalent to ±3.0kHz deviation with the settings below:

   *Tx Gain = 0dB* *Mod Level = 0dB*

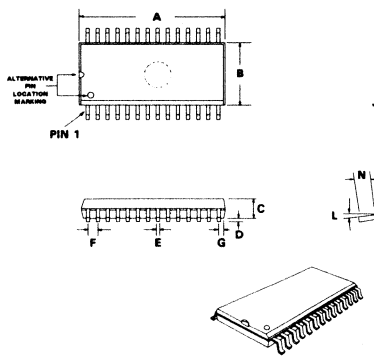
   *Rx Gain = 7.05dB* *Volume = 0dB*

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.
3. Recommended load >10.0kΩ.

## Package Outline

The FX826DW Small Outline Integrated Circuit is shown in Figure 10 and the "J" version in Figure 11. Pin 1 identification marking is shown on the relevant diagram.
Pins on both package styles number anti-clockwise when viewed from the top (marked side).

*Fig.10* ***FX826DW*** *28-pin S.O.I.C. Package*



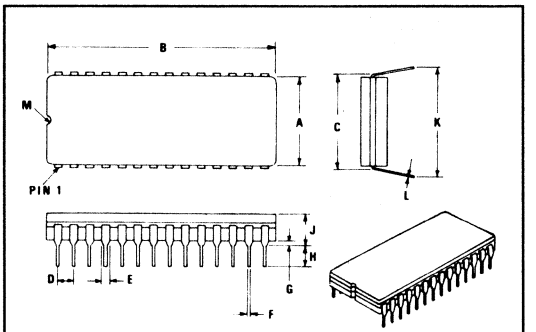

All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 18.05 | | 17.70 | G | | 0.66 | |
| B | 7.65 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

## Handling Precautions

The FX826 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

*Fig.11* ***FX826J*** *28-pin DIL Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX | MIN | DIMENSION | MAX | MIN |
|---|---|---|---|---|---|
| A | 13.36 | 13.06 | G | 1.40 | TYPICAL |
| B | 37.05 | 36.58 | H | 4.30 | 4.10 |
| C | 15.70 | 15.50 | J | 5.57 | 4.49 |
| D | 2.54 | TYPICAL | K | 17.00 | TYPICAL |
| E | 1.39 | TYPICAL | L | 0.25 | TYPICAL |
| F | 0.45 | TYPICAL | M | 0.64R | TYPICAL |

## Ordering Information

**FX826DW** 28-pin plastic S.O.I.C.

**FX826J** 28-pin cerdip DIL

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX836 Radiocom 2000 System Audio Processor

Publication D/836/2 February 1993
Provisional Issue

## Features/Applications

- **Full-Duplex Audio Processing for R2000 Cellular System**
- **On-Chip Speech and Data Facilities**
  - **Tx/Rx/Data Filtering & Gain**
  - **Pre-/De-Emphasis – Deviation Limiter**
- **Serial μProcessor Interface**
- **Tx and Rx LF-Data Paths**
- **FFSK and (50 Baud) LF-Data Facilities**
- **Hands-Free Compatibility**
- **Access to External Processes**
  - ***Compression – Expansion***
  - ***Signalling/Data Mixing***
  - ***VSR Codec (Store/Play)***
- **Powersave (Low-Current) Settings**

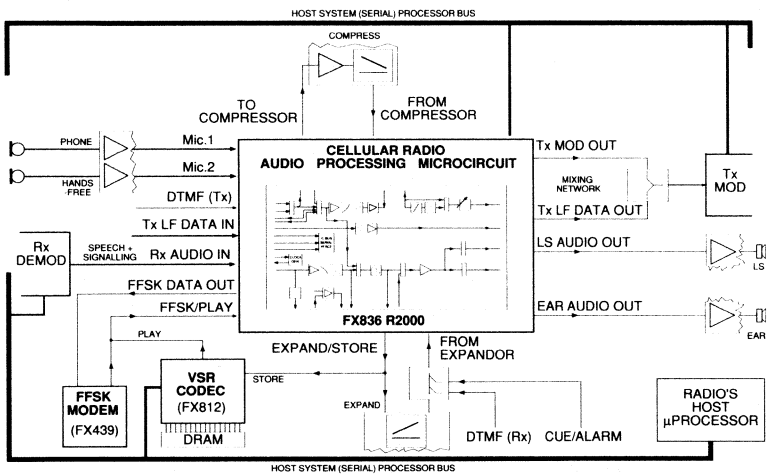



*Fig.1 The FX836 R2000 Audio Processor within a Cellular System*

FX836

## Brief Description

The FX836 is a μProcessor controlled full-duplex audio processor on a single-chip with separate Tx, Rx and LF (50 baud) data paths to provide all the filter/gain/limiting functions necessary to pre-process audio, data and signalling in the Radiocom 2000 (R2000) Cellular communications system.

Selectable inputs available for transmission are: a choice of two microphones, DTMF/signalling or FFSK/data, with access, in this path, to external voice compression circuitry. Operationally the Tx path provides input gain/ filtering, pre-emphasis, a deviation limiter and Tx Modulation Drive controls. Available to the transmit function is a separate path to process LF system control data for amalgamation externally with Tx voiceband audio.

The Rx path consists of an input gain/de-emphasis/filter block for voice and data, inputs from an external audio expansion system and output gain controls driving loudspeaker and earpiece circuitry.

In the Rx path LF data signals are separated from the incoming audio via an LF filter and made available at a separate pin for use by the system μProcessor

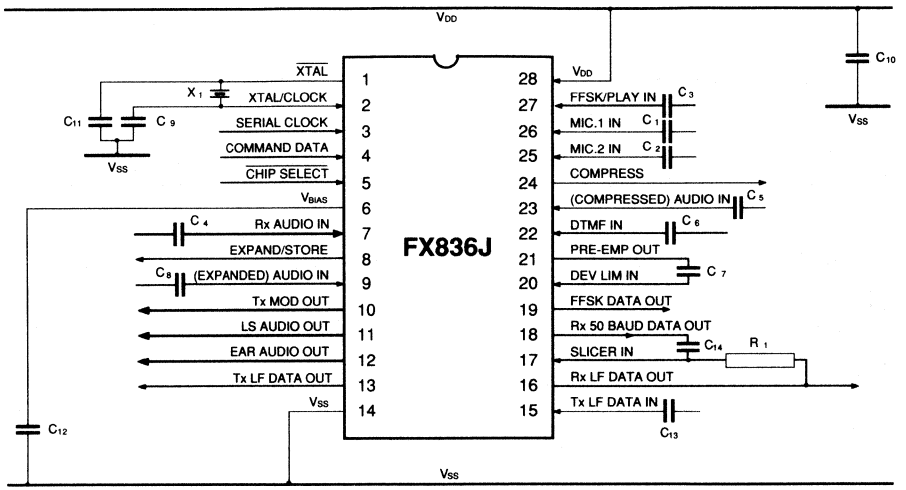
Unique to the FX816/826/836 cellular audio processors is the ability to route audio (Tx or Rx) to an external Voice Store and Retrieve (VSR) device such as the FX802 or FX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

The FX836, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

| Pin Number FX836DW FX836J | Function |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. |
| 2 | **Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock ($f_{XTAL}$) should be connected here. Note that operation of the FX836 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes). |
| 3 | **Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the FX836. See Timing Diagrams. |
| 4 | **Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the FX836 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams. |
| 5 | **Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Timing Diagrams. |
| 6 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$. See Figure 2. |
| 7 | **Rx Audio In:** Normally taken from the radio's discriminator output. This input has a 1MΩ internal resistor to $V_{BIAS}$ and requires to be connected via a capacitor. |
| 8 | **Expand/Store:** A common output that can be used as either an input to an external audio expandor or the input to a voice storage medium such as the FX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 4. |
| 9 | **(Expanded) Audio In:** The audio input, via SW5, from an external expandor or audio mixing function. This input has a 1MΩ internal resistor to $V_{BIAS}$ and requires to be connected via a capacitor. See Figures 2 and 4. |
| 10 | **Tx Mod Out:** The composite Tx audio output to the transmitter modulator from a variable attenuation stage ($11_H$). This output is set to $V_{BIAS}$ via an internal 1MΩ resistor when set to Powersave or OFF. |
| 11 | **LS Audio Out:** An audio output of the Rx Path (or audio selected by SW2 and SW4 Figure 4) for a loudspeaker system. Available for handsfree operation this output is controlled by the Rx Gain and LS Volume Command ($12_H$) and is internally connected to $V_{BIAS}$ when not required. A driver amplifier may be required at this output. |
| 12 | **Ear Audio Out:** An audio output of the Rx Path (or audio selected by SW2 and SW4–Figure 4), available as an output for a handset earpiece. Separate from the LS Audio Out function, this output is controlled by the LF Data Gain and Ear Volume Command ($13_H$) and is internally connected to $V_{BIAS}$ when not required. A driver amplifier may be required at this output. |
| 13 | **Tx LF Data Out:** The output, if required, to the Tx Modulator, of LF (50 baud) filtered and level-adjusted digital data. |
| 14 | **$V_{SS}$:** Negative supply rail. Signal ground. |
| | ***Notes on Inputs:*** *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.* |

| Pin Number<br>FX836DW<br>FX836J | Function |
|---|---|
| 15 | **Tx LF Data In:** The input of LF (50 baud) digital data for transmission, from an external modem. This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 16 | **Rx LF Data Out:** The output, to a 50 baud modem, of the received, filtered, LF data. This pin is used with the 50 Baud Data, Slicer In pins and external components to filter and limit the received LF data. See Figure 4. |
| 17 | **Slicer In:** The input to the data slicer. Employed as shown in Figure 4 to filter and limit the received LF data. |
| 18 | **Rx 50 Baud Data Out:** The output of the received 50 baud data. See Figures 2 and 4. |
| 19 | **FFSK Out:** The de-emphasized Rx audio output available for access to the received FFSK data. This output could be directed to an FFSK Modem such as the FX439. |
| 20 | **Deviation Limiter In:** Input to the on-chip deviation Limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling is required to achieve the best possible symmetry of limiting as this input has a 1MΩ internal resistor to $V_{BIAS}$. See Figure 2. |
| 21 | **Pre-Emphasis Out:** Audio output from the Tx Input Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 and 4. |
| 22 | **DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the Tx Path, controlled by SW2 (Configuration Command ($10_H$)). This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 23 | **Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 24 | **Compression:** The output to an external audio compression system. Currently available compressor/ expandors have Op-Amps incorporated. The compressor can be by-passed by SW2. |
| 25<br>26 | **Mic.2 In:**<br>**Mic.1 In:** Tx voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any Tx audio input. Pre-amplification may be required prior to these inputs. Each input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 27 | **FFSK/Play In:** The Tx FFSK data input via SW2. This can also be used to input (replay) from a voice storage device such as the FX812. This "replayed" audio can be sent to Rx or Tx paths allowing a Messaging/Voice Notepad/Answering facility. Both FX439 FFSK Modem and FX812 VSR Codec outputs can be wired together at this pin (OR'd) if the functions are activated one-at-a-time. This input has an internal 1MΩ resistor to $V_{BIAS}$ and should be connected via a capacitor. |
| 28 | **$V_{DD}$:** Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this audio processor are dependent upon this supply.<br>***"C-BUS"** is CML's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController.*<br>*For further details refer to CML Publication No. DµINT/1 June 1991 or DBS 800 System Information Document.* |

# Application Information




| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $R_1$ | = | 1.0MΩ | $C_4$ | = | 100nF | $C_8$ | = | 100nF | $C_{12}$ | = | 1.0µF |
| $C_1$ | | 100nF | $C_5$ | | 100nF | $C_9$ | | 33pF | $C_{13}$ | | 100nF |
| $C_2$ | | 100nF | $C_6$ | | 100nF | $C_{10}$ | | 100nF | $C_{14}$ | | 100nF |
| $C_3$ | | 100nF | $C_7$ | | 100nF | $C_{11}$ | | 33pF | $X_1$ | | 4.032MHz |

**Tolerances** – Resistors ±10% Capacitors ±20%

*Fig.2 Recommended External Components*

1. **Xtal/clock operation**
   Operation of any CML microcircuit without a Xtal or clock input may cause device damage.
   To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast-reaction fuse).

2. **FFSK Modem**
   The FX439, a general purpose FFSK Modem could be employed with this R2000 system Audio Processor. The FX439 is a non-formatted modem, which with due regard to Xtal/clock frequencies and µProcessor interface, is compatible with both Mobile/Portable and Base Station applications.

## Reference Signal Levels

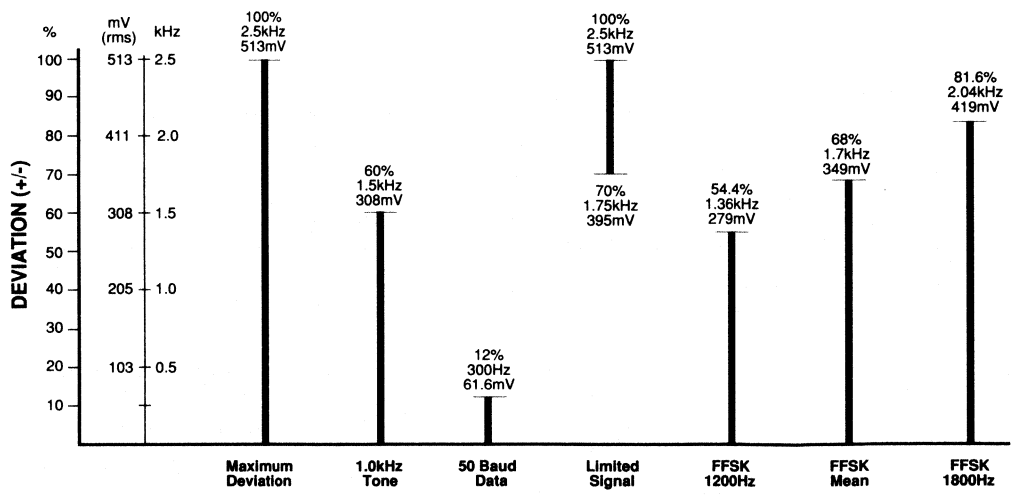



*Fig.3 R2000 Signal Deviation Levels and corresponding **Tx Mod Outputs** with the Mod Level set to 0dB*

## R2000 Cellular System Interfaces

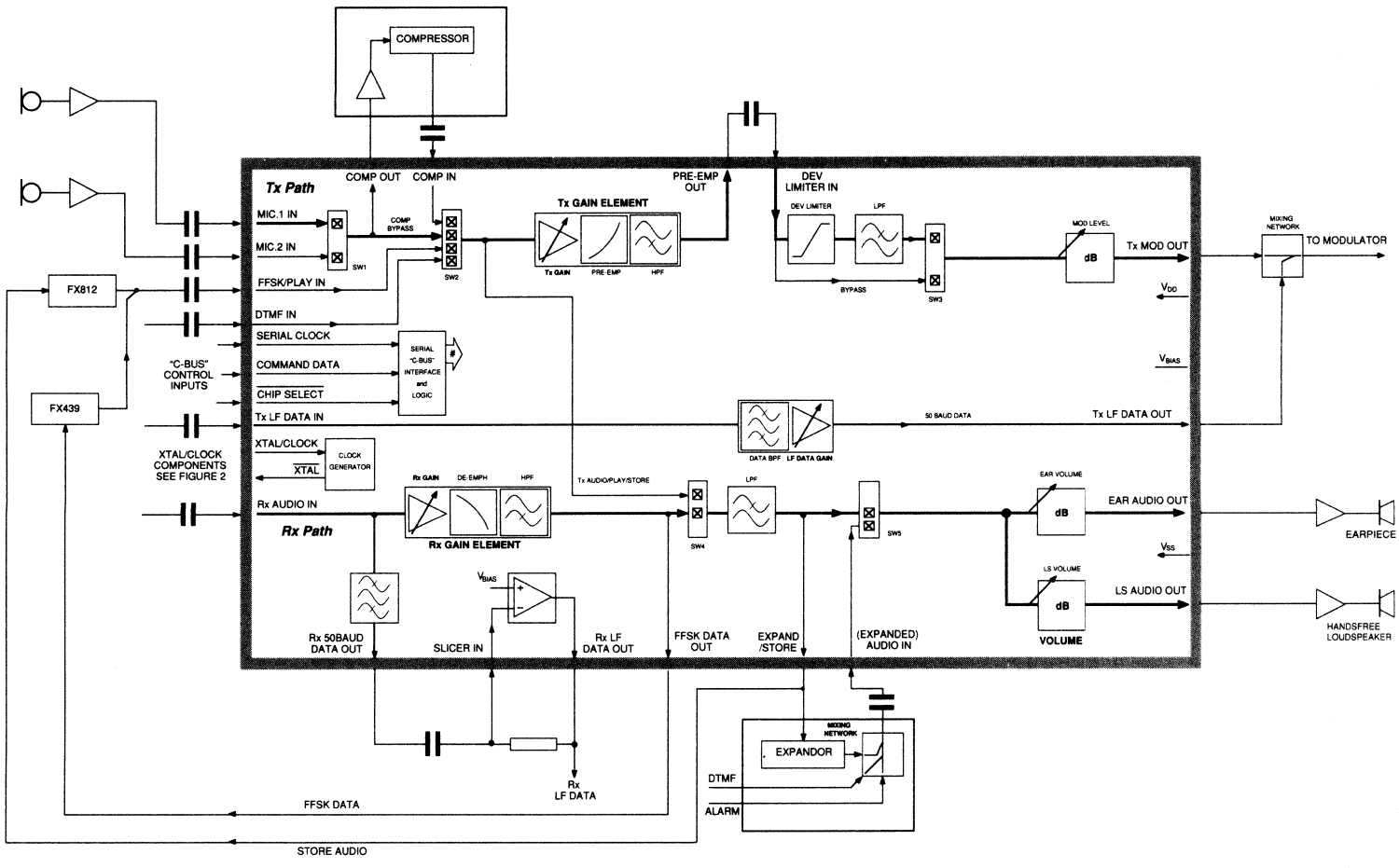



*Fig.4 The FX836 within an R2000 Cellular Radio System*

# The Controlling System

## "C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

---

Control of the functions and levels within the FX836 R2000 Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device. The use of these instructions is detailed in the following paragraphs and tables.

| Command Assignment | Address/Command (A/C) Byte Hex | Binary MSB LSB | | Command Data | Table |
|---|---|---|---|---|---|
| General Reset | 01 | 0 0 0 0 0 0 0 1 | | | |
| Configuration Command | 10 | 0 0 0 1 0 0 0 0 | + | 1 byte | 2 |
| Tx Gain & Mod. Level | 11 | 0 0 0 1 0 0 0 1 | + | 1 byte | 3 |
| Rx Gain & LS Vol. | 12 | 0 0 0 1 0 0 1 0 | + | 1 byte | 4 |
| LF Data Gain & Ear Vol. | 13 | 0 0 0 1 0 0 1 1 | + | 1 byte | 5 |

*Table 1 "C-Bus" Address/Commands*

In "C-BUS" protocol the audio processor is allocated Address/Command (A/C) values $10_H$ to $13_H$. Configuration, Tx/Rx Gains and SAT/Powersave assignments and data requirements are given in Table 1. Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2,3,4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). Therefore a **General Reset Command ($01_H$)** will be required initially to set all FX836 registers to $00_H$.

## Configuration Command *(Preceded by A/C $10_H$)*

| Setting | Control Bits |
|---|---|
| ***MSB*** | ***Transmitted First*** |
| ***Bit 7*** | **Rx Gain Element** |
| 0 | Powersave |
| 1 | Enable |
| ***6*** | **All Functions** (except Rx Gain Element) |
| 0 | Powersave |
| 1 | Enable |
| ***5*** | **Sw5 Expandor** |
| 0 | Expandor By-Pass |
| 1 | Expandor Route |
| ***4*** | **Sw4 Tx/Rx Audio** |
| 0 | Tx Store/Audio |
| 1 | Rx Store/Audio |
| ***3*** | **Sw3 Dev. Limiter** |
| 0 | Dev. Limiter By-Pass |
| 1 | Dev. Limiter Route |
| ***2*** | **Sw1 Mic. Inputs** |
| 0 | Mic. 1 Input |
| 1 | Mic.2 Input |
| ***1*** ***0*** | **Sw2 Tx Function** |
| 0 0 | DTMF In |
| 0 1 | Compressor In |
| 1 0 | Compressor By-Pass |
| 1 1 | FFSK/Play In |

**Note** that Bits 6 and 7 can be configured to allow the Rx to "listen for data" whilst powersaved. See Figure 4.

*Table 2 Configuration Commands*

## Tx Gain & Mod. Level *(Preceded by A/C $11_H$)*

| Setting | | | | Gain (dBs) |
|---|---|---|---|---|
| ***MSB*** | | | | ***Transmitted First*** |
| ***7*** | ***6*** | ***5*** | ***4*** | **Tx Mod. Level** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -5.6 |
| 0 | 0 | 1 | 0 | -5.2 |
| 0 | 0 | 1 | 1 | -4.8 |
| 0 | 1 | 0 | 0 | -4.4 |
| 0 | 1 | 0 | 1 | -4.0 |
| 0 | 1 | 1 | 0 | -3.6 |
| 0 | 1 | 1 | 1 | -3.2 |
| 1 | 0 | 0 | 0 | -2.8 |
| 1 | 0 | 0 | 1 | -2.4 |
| 1 | 0 | 1 | 0 | -2.0 |
| 1 | 0 | 1 | 1 | -1.6 |
| 1 | 1 | 0 | 0 | -1.2 |
| 1 | 1 | 0 | 1 | -0.8 |
| 1 | 1 | 1 | 0 | -0.4 |
| 1 | 1 | 1 | 1 | 0 |
| ***3*** | ***2*** | ***1*** | ***0*** | **Tx Input Gain** |
| 0 | 0 | 0 | 0 | -2.65 |
| 0 | 0 | 0 | 1 | -2.05 |
| 0 | 0 | 1 | 0 | -1.50 |
| 0 | 0 | 1 | 1 | -0.95 |
| 0 | 1 | 0 | 0 | -0.45 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0.45 |
| 0 | 1 | 1 | 1 | 0.85 |
| 1 | 0 | 0 | 0 | 1.25 |
| 1 | 0 | 0 | 1 | 1.65 |
| 1 | 0 | 1 | 0 | 2.05 |
| 1 | 0 | 1 | 1 | 2.40 |
| 1 | 1 | 0 | 0 | 2.70 |
| 1 | 1 | 0 | 1 | 3.05 |
| 1 | 1 | 1 | 0 | 3.35 |
| 1 | 1 | 1 | 1 | 3.65 |

*Table 3 Tx Gain & Mod. Commands*

## The Controlling System .....

### Rx Gain & LS Vol.

*(Preceded by A/C $12_H$)*

| Setting | | | | Gain (dBs) |
|---|---|---|---|---|
| MSB | | | | |
| 7 | 6 | 5 | 4 | **Transmitted First** **Rx LS Volume** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -28.0 |
| 0 | 0 | 1 | 0 | -26.0 |
| 0 | 0 | 1 | 1 | -24.0 |
| 0 | 1 | 0 | 0 | -22.0 |
| 0 | 1 | 0 | 1 | -20.0 |
| 0 | 1 | 1 | 0 | -18.0 |
| 0 | 1 | 1 | 1 | -16.0 |
| 1 | 0 | 0 | 0 | -14.0 |
| 1 | 0 | 0 | 1 | -12.0 |
| 1 | 0 | 1 | 0 | -10.0 |
| 1 | 0 | 1 | 1 | -8.0 |
| 1 | 1 | 0 | 0 | -6.0 |
| 1 | 1 | 0 | 1 | -4.0 |
| 1 | 1 | 1 | 0 | -2.0 |
| 1 | 1 | 1 | 1 | 0 |
| 3 | 2 | 1 | 0 | **Rx Input Gain** |
| 0 | 0 | 0 | 0 | 3.75 |
| 0 | 0 | 0 | 1 | 4.30 |
| 0 | 0 | 1 | 0 | 4.80 |
| 0 | 0 | 1 | 1 | 5.30 |
| 0 | 1 | 0 | 0 | 5.80 |
| 0 | 1 | 0 | 1 | 6.20 |
| 0 | 1 | 1 | 0 | 6.65 |
| 0 | 1 | 1 | 1 | 7.05 |
| 1 | 0 | 0 | 0 | 7.40 |
| 1 | 0 | 0 | 1 | 7.80 |
| 1 | 0 | 1 | 0 | 8.15 |
| 1 | 0 | 1 | 1 | 8.50 |
| 1 | 1 | 0 | 0 | 8.80 |
| 1 | 1 | 0 | 1 | 9.10 |
| 1 | 1 | 1 | 0 | 9.40 |
| 1 | 1 | 1 | 1 | 9.70 |

*Table 4 Rx Gain and LS Vol. Command*

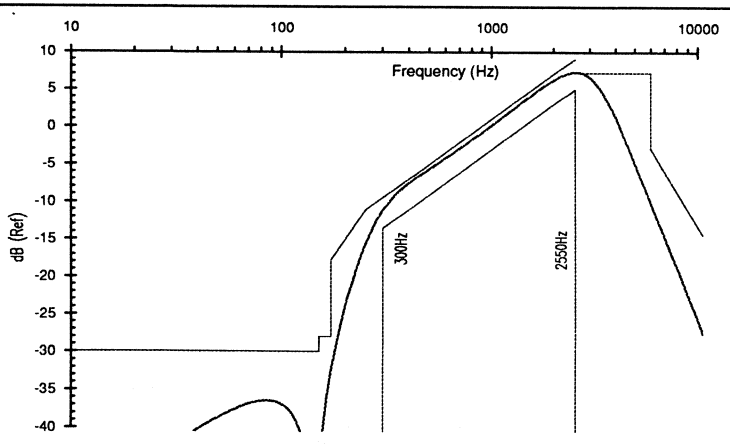
### LF Data Gain & Ear Vol.

*(Preceded by A/C $13_H$)*

| Setting | | | | Gain (dBs) |
|---|---|---|---|---|
| MSB | | | | |
| 7 | 6 | 5 | 4 | **Transmitted First** **Rx Ear Volume** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -28.0 |
| 0 | 0 | 1 | 0 | -26.0 |
| 0 | 0 | 1 | 1 | -24.0 |
| 0 | 1 | 0 | 0 | -22.0 |
| 0 | 1 | 0 | 1 | -20.0 |
| 0 | 1 | 1 | 0 | -18.0 |
| 0 | 1 | 1 | 1 | -16.0 |
| 1 | 0 | 0 | 0 | -14.0 |
| 1 | 0 | 0 | 1 | -12.0 |
| 1 | 0 | 1 | 0 | -10.0 |
| 1 | 0 | 1 | 1 | -8.0 |
| 1 | 1 | 0 | 0 | -6.0 |
| 1 | 1 | 0 | 1 | -4.0 |
| 1 | 1 | 1 | 0 | -2.0 |
| 1 | 1 | 1 | 1 | 0 |
| 3 | 2 | 1 | 0 | **LF** (50 Baud) **Data Gain** |
| 0 | 0 | 0 | 0 | OFF (Low Z to $V_{BIAS}$) |
| 0 | 0 | 0 | 1 | -2.60 |
| 0 | 0 | 1 | 0 | -2.20 |
| 0 | 0 | 1 | 1 | -1.80 |
| 0 | 1 | 0 | 0 | -1.40 |
| 0 | 1 | 0 | 1 | -1.00 |
| 0 | 1 | 1 | 0 | -0.70 |
| 0 | 1 | 1 | 1 | -0.35 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0.30 |
| 1 | 0 | 1 | 0 | 0.60 |
| 1 | 0 | 1 | 1 | 0.90 |
| 1 | 1 | 0 | 0 | 1.20 |
| 1 | 1 | 0 | 1 | 1.50 |
| 1 | 1 | 1 | 0 | 1.75 |
| 1 | 1 | 1 | 1 | 2.00 |

*Table 5 LF Data Gain and Rx Ear Volume Command*

## System Performance




Mic.1 In to Tx Mod. Out
$V_{DD}$ = 5.0V
Signal Input Level = 55mVrms
Tx Gain set to 0dB
Mod Level set to 0dB

*Fig.5 Tx Voiceband Frequency Response*

## System Performance .....

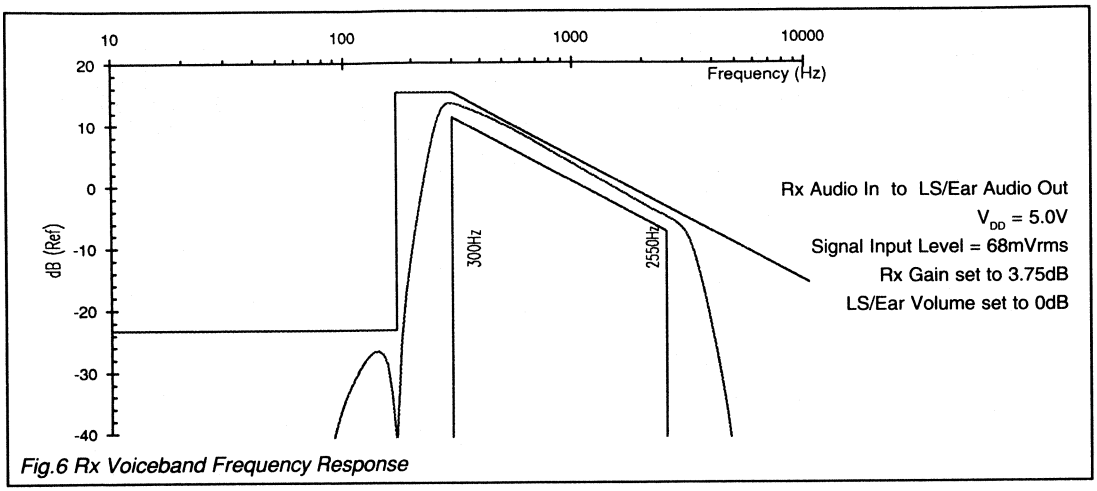



*Fig.6 Rx Voiceband Frequency Response*

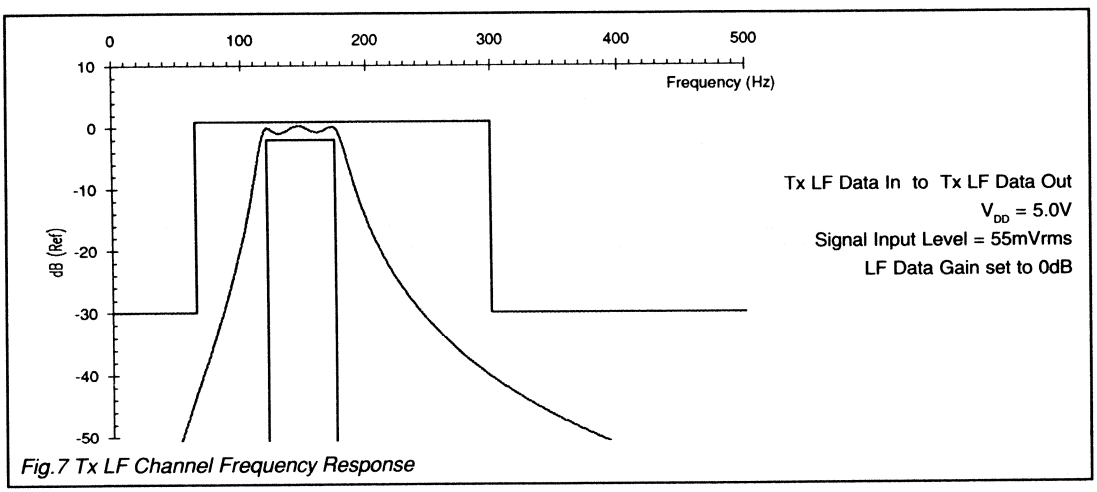



*Fig.7 Tx LF Channel Frequency Response*

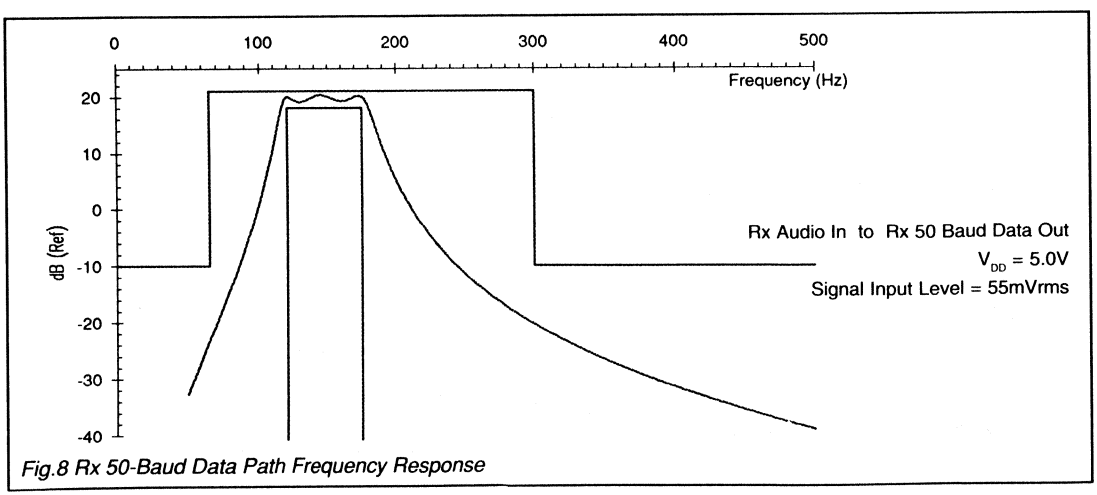



*Fig.8 Rx 50-Baud Data Path Frequency Response*

# Control Timing Information

Timing Specification – Figures 9 and 10

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CSE}$ | "CS-Enable to Clock-High" | 1 | 2.0 | – | – | µs |
| $t_{CSH}$ | Last "Clock-High to CS-High" | 1 | 4.0 | – | – | µs |
| $t_{CSOFF}$ | "CS-High" Time between transactions | 1, 2 | 2.0 | – | – | µs |
| $t_{CK}$ | "Clock-Cycle" Time | 1 | 2.0 | – | – | µs |
| $t_{NXT}$ | "Inter-Byte" Time | 1 | 4.0 | – | – | µs |
| $t_{CH}$ | "Serial Clock-High" Period | | 500 | – | – | ns |
| $t_{CL}$ | "Serial Clock-Low" Period | | 500 | – | – | ns |
| $t_{CDS}$ | "Command Data Set-Up" Time | | 250 | – | – | ns |
| $t_{CDH}$ | "Command Data Hold" Time | | 0 | – | – | ns |

**Notes**

1. These Minimum Timing values are altered during operation of the FX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

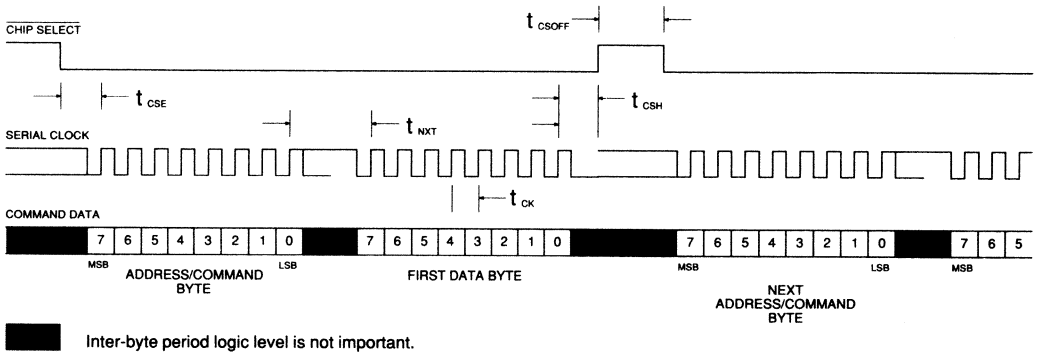



*Fig.9 Control Timing Information*

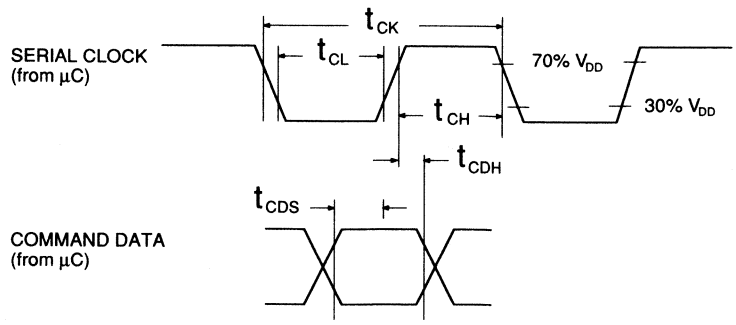



*Fig.10 Control Timing Relationships*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref. $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX836DW** | -40°C to +85°C (plastic) |
| | **FX836J** | -40°C to +85°C (cerdip) |
| Storage temperature range: | **FX836DW** | -40°C to +85°C (plastic) |
| | **FX836J** | -55°C to +125°C (cerdip) |

### Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.032MHz. Audio level 0dB ref. = 308mV rms @ 1.0kHz.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | | | | |
| All Operating | | – | 10.0 | – | mA |
| Rx Data Mode | 1 | – | 2.5 | – | mA |
| Powersave All | | – | 0.6 | – | mA |
| Alias Frequency | | – | 63.0 | – | kHz |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | – | – | MΩ |
| $R_{OUT}$ | | – | 10.0 | – | kΩ |
| Inverter Gain | | – | 10.0 | – | V/V |
| Gain/Bandwidth Product | | – | 10.0 | – | MHz |
| **Analogue Input Impedances** | | | | | |
| Mic.1 & 2 | | – | 500 | – | kΩ |
| FFSK/Play | | – | 500 | – | kΩ |
| Comp In | | – | 500 | – | kΩ |
| DTMF In | | – | 500 | – | kΩ |
| Dev. Limiter In | | – | 100 | – | kΩ |
| (Expanded) Audio In | | – | 47.0 | – | kΩ |
| Tx LF Data In | | – | 500 | – | kΩ |
| Slicer In | | 10.0 | – | – | MΩ |
| Rx Audio In | | – | 100 | – | kΩ |
| **Analogue Output Impedances** | | | | | |
| Pre-Emp Out | | – | 600 | – | Ω |
| Tx Mod Out | | – | 600 | – | Ω |
| Expand/Store | | – | 600 | – | Ω |
| LS and Ear Audio | | – | 1.0 | – | kΩ |
| FFSK Data Out | | – | 600 | – | Ω |
| Rx LF Data Out | | – | 2.0 | – | kΩ |
| Tx 50 Baud Data Out | | – | 600 | – | Ω |
| Switches – ON | | – | 1.0 | – | kΩ |
| – OFF | | 10.0 | – | – | MΩ |
| **Control Interface Parameters** | | | | | |
| Input Logic Levels | | | | | |
| Logic "1" | 2 | 3.5 | – | – | V |
| Logic "0" | 2 | – | – | 1.5 | V |
| $I_{IN}$ (logic "1" or "0") | 2 | -1.0 | – | 1.0 | µA |
| Input Capacitance | 2 | – | – | 7.5 | pF |
| **Channel Performances** | | | | | |
| **Tx Path** | | | | | |
| **Analogue Signal Input Levels** | | | | | |
| Mic. 1 and 2 | 3 | – | 0 | – | dB |
| FFSK/Play | 3 | – | 0 | – | dB |
| DTMF | 3 | – | 0 | – | dB |
| Comp. In | 3 | – | 0 | – | dB |
| Tx LF Data In | | – | 0 | – | dB |

# Specification .....

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Analogue Signal Output Levels** | | | | | |
| Pre-Emp Out | 3 | – | 0 | – | dB |
| Tx Mod Out | 3 | – | 0 | – | dB |
| Tx LF Data Out | | – | 0 | – | dB |
| **Path Gains/Levels** | | | | | |
| **Tx Gain – $11_H$** | | | | | |
| Nominal Adjustment Range | | -2.65 | | 3.65 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |
| **Dev Limiter** | | | | | |
| Threshold | | – | 1375 | – | mVp-p |
| Symmetry | | – | 7.0 | – | % |
| **Mod Level Attenuation – $11_H$** | | | | | |
| Nominal Adjustment Range | | -5.6 | | 0 | dB |
| Step Size | | 0.2 | 0.4 | 0.6 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| **Tx LF Data Signal Path** | | | | | |
| **Bandpass Filter** | | | | | |
| Passband | | 120 | | 175 | Hz |
| Gain | | – | 0 | – | dB |
| **LF Data Gain Level – $13_H$** | | | | | |
| Nominal Adjustment Range | | -2.6 | | 2.0 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |
| **Overall** | | | | | |
| Tx Distortion | | – | -40.0 | -32.0 | dBp |
| Tx Hum and Noise | | – | -40.0 | -20.0 | dB |
| **Rx Signal Path** | | | | | |
| Rx Audio Input Level | 3 | – | -7.0 | – | dB |
| LS/Ear Audio Output Level | 3 | – | 0 | – | dB |
| **Path Gains/Levels** | | | | | |
| **Rx Gain – $12_H$** | | | | | |
| Nominal Adjustment Range | | 3.75 | | 9.70 | dB |
| Error of any Setting | | -0.2 | – | 0.2 | dB |
| **De-Emphasis** | | | | | |
| Frequency Range | | 900 | – | 2100 | Hz |
| Gain at 1kHz | | -1.0 | 0 | 1.0 | dB |
| Response | | – | -6.0 | – | dB/oct |
| **LS/Ear Volume – $12_H/13_H$** | | | | | |
| Nominal Adjustment Range | | -28.0 | | 0 | dB |
| Step Size | | 1.5 | 2.0 | 2.5 | dB |
| Error of any Setting | | -1.0 | – | 1.0 | dB |
| **Overall** | | | | | |
| Rx Distortion | | – | -40.0 | -32.0 | dBp |
| Rx Hum and Noise | | – | -40.0 | -34.0 | dB |
| **Rx 50 Baud AudioPath** | | | | | |
| **Bandpass Filter** | | | | | |
| Passband | | 120 | | 175 | Hz |
| Gain | | 19.0 | 20.0 | 21.0 | dB |

**Notes**

1. With reference to the Configuration Command and Figure 3, all functions with the exception of the Rx Gain Element may be powersaved. This will still allow signalling data through the FX836 to activate the system via the µProcessor.
2. Serial Clock, Command Data and Chip Select inputs.
3. Levels equivalent to ±1.5kHz deviation with the settings below:

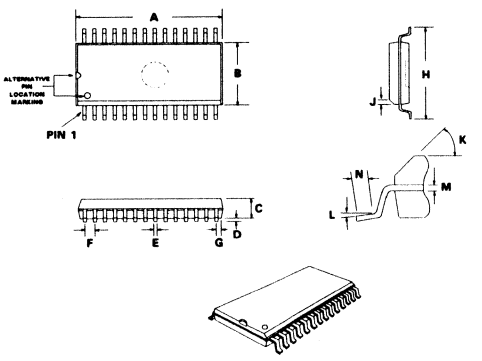
   *Tx Gain = 0dB* *Mod Level = 0dB*
   *Rx Gain = 7.05dB* *LS/Ear Volume = 0dB*

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.

## Package Outline

The FX836DW Small Outline Integrated Circuit is shown in Figure 11 and the "J" version in Figure 12. Pin 1 identification marking is shown on the relevant diagram.
Pins on both package styles number anti-clockwise when viewed from the top (marked side).

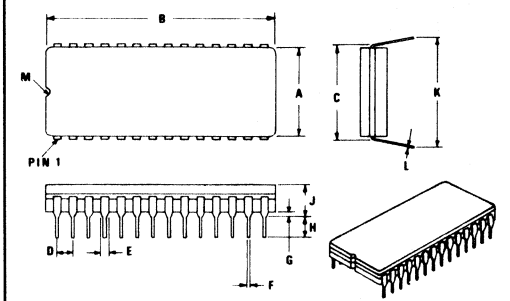
*Fig.11* ***FX836DW*** *28-pin S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 18.05 | | 17.70 | G | | 0.66 | |
| B | 7.65 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.12* ***FX836J*** *28-pin DIL Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX | MIN | DIMENSION | MAX | MIN |
|---|---|---|---|---|---|
| A | 13.36 | 13.06 | G | 1.40 | TYPICAL |
| B | 37.05 | 36.58 | H | 4.30 | 4.10 |
| C | 15.70 | 15.50 | J | 5.57 | 4.49 |
| D | 2.54 | TYPICAL | K | 17.00 | TYPICAL |
| E | 1.39 | TYPICAL | L | 0.25 | TYPICAL |
| F | 0.45 | TYPICAL | M | 0.64R | TYPICAL |

## Handling Precautions

The FX836 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

## Ordering Information

**FX836DW** 28-pin plastic S.O.I.C.

**FX836J** 28-pin cerdip DIL

# Integrated Circuits Data Book

Section 4

# Military Comms

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX619 'Eurocom' Delta Codec

Publication D/619/3 December 1990
Provisional Issue

## Features/Applications

- Designed to Meet Eurocom D1-IA8
- Military Communications
- Delta MUX, Switch and Phone Applications
- Single Chip Full Duplex Codec
- On-Chip Input and Output Filters
- Programmable Sampling Clocks
- 3 or 4-bit Compand Algorithm
- Forced Idle Facility
- Powersave Facility
- Single 5V CMOS Process
- Full Duplex CVSD* Codec

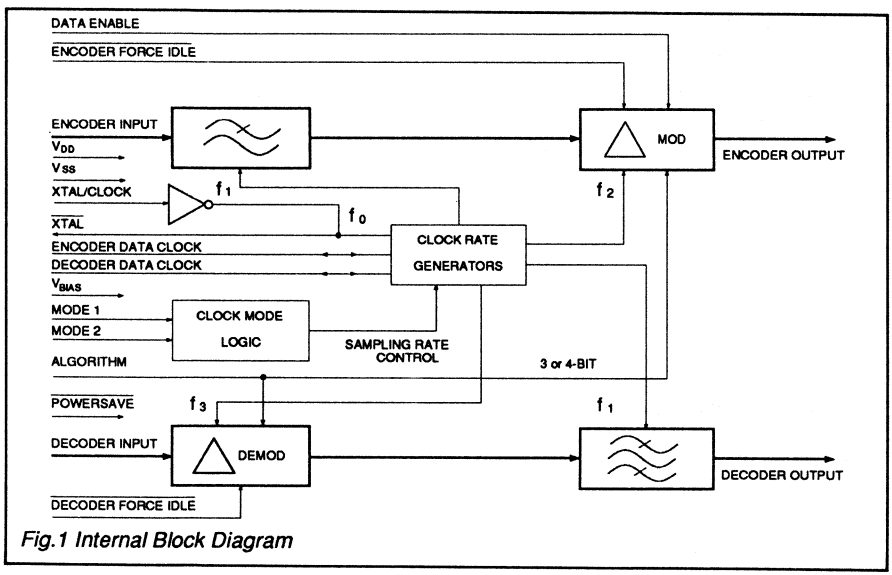



*Fig.1 Internal Block Diagram*

**FX619**

## Brief Description

The FX619 is an LSI circuit designed as a *Continuously Variable Slope Delta Codec and is intended for use in military communications systems.

Designed to meet Eurocom D1-IA8 with external components, the device is suitable for applications in military Delta Multiplexers, switches and phones.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32 or 64 k bits/second from an internal clock generator or may be externally applied in the range 8 to 64 k bits/second. Sampling clock frequencies are output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle facilities are provided forcing a 10101010..... pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuits may be operated with a 3 or 4-bit algorithm which is externally selected. The device may be put in the standby mode by selection of the powersave facility. A reference 1.024MHz oscillator uses an external clock or Xtal.

The FX619 is a low-power, 5 volt CMOS device and is available in 22-pin cerdip DIL and 28-lead ceramic leadless SMT packages.

| Pin Number FX619J | Pin Number FX619M1 | Function |
|---|---|---|
| 1 | 1 | **Xtal/Clock :** Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3. |
| | 2 | No connection |
| 2 | 3 | **$\overline{\text{Xtal}}$ :** Output of clock oscillator inverter. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986. |
| 3 | 4 | No connection |
| 4 | 5 | **Encoder Data Clock :** A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependant upon clock mode 1, 2 inputs and Xtal frequency (see Clock Mode pins). |
| 5 | 6 | **Encoder Output :** The encoder digital output, this is a three state output whose condition is set by Data Enable and Powersave inputs as shown : |
| | 7, 8 | No connection |
| 6 | 9 | **$\overline{\text{Encoder Force Idle}}$ :** When this pin is a logical '0' the encoder is forced to an idle state and the encoder digital output is 0101..., a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup. |
| 7 | 10 | **Data Enable :** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup. |
| 8 | 11 | No connection |
| 9 | 12 | **Bias :** Normally at $V_{DD}$ /2 bias, this pin requires to be externally decoupled by a capacitor, $C_4$. Internally pulled to $V_{SS}$ when "Powersave" is a logical '0'. |
| 10 | 13 | **Encoder Input :** The analogue signal input. Internally biased at $V_{DD}$ /2, external components are required on this input. The source impedance should be less than 100Ω, output idle channel noise levels will improve with an even lower source impedance. See Fig. 3. |
| 11 | 14 | **$V_{SS}$ :** Negative Supply. |

| Data Enable | $\overline{\text{Powersave}}$ | Encoder Output |
|---|---|---|
| 1 | 1 | Enabled |
| 0 | 1 | High Z (o/c) |
| 1 | 0 | Vss |

| Pin Number | | Function |
|---|---|---|
| FX619J | FX619M1 | |
| 12 | 15,16 | No connection |
| 13 | 17 | **Decoder Output :** The recovered analogue signal is output at this pin, it is the buffered output of a bandpass filter and requires external components. During "Powersave" this output is o/c. |
| 14 | 18,19 | No connection |
| 15 | 20 | $\overline{\text{Powersave}}$ **:** A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup. |
| | 21 | No connection |
| 16 | 22 | $\overline{\text{Decoder Force Idle}}$ **:** A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the decoder output goes to $V_{DD}/2$. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup. |
| 17 | 23 | **Decoder Input :** The received digital signal input. Internal 1MΩ Pullup. |
| 18 | 24 | **Decoder Data Clock :** A Logic I/O port. External decode clock input or internal data clock output, dependant upon clock mode 1, 2 inputs, see Clock Mode pins. |
| 19 | 25 | **Algorithm :** A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup. |
| 20 | 26 | **Clock Mode 2 :** |
| 21 | 27 | **Clock Mode 1 :** Internal 1MΩ Pullups. |

| Clock Mode 1 | Clock Mode 2 | Facility |
|---|---|---|
| 0 | 0 | External clocks |
| 0 | 1 | Internal, 64kb/s = f ÷ 16 |
| 1 | 0 | Internal, 32kb/s = f ÷ 32 |
| 1 | 1 | Internal, 16kb/s = f ÷ 64 |

Clock rates refer to f = 1.024 MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independant or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

| | | |
|---|---|---|
| 22 | 28 | $V_{DD}$ **:** Positive Supply. A single + 5 volt power supply is required. |

## Codec Integration

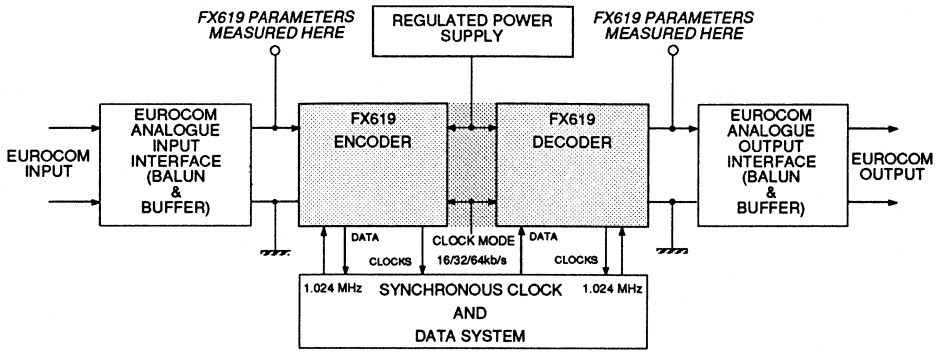



*Fig.2 Eurocom System Configuration – showing the FX619, which with the indicated interfacing, will conform to the Eurocom Basic Parameters Specification D1 – IA8.*

| Component | Unit Value | **Note** – with reference to Figure 3 (below) |
|---|---|---|
| $R_1$ | 1M | Oscillator Inverter bias resistor. |
| $R_2$ | Selectable | Xtal Drive limiting resistor. |
| $C_1$ | 33p | Xtal Circuit drain capacitor. |
| $C_2$ | 33p | Xtal Circuit gate capacitor. |
| $C_3$ | 1.0µ | Encoder Input coupling capacitor – The drive source impedance to this input should be less than 100Ω. Output Idle channel noise levels will improve with an even lower source impedance. |
| $C_4$ | 1.0µ | Bias decoupling capacitor. |
| $C_5$ | 1.0µ | $V_{DD}$ decoupling capacitor. |
| $X_1$ | 1.024 MHz | A 1.024 MHz Xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986. |
| | | Tolerance :– Resistors ± 10% Capacitors ± 20% |

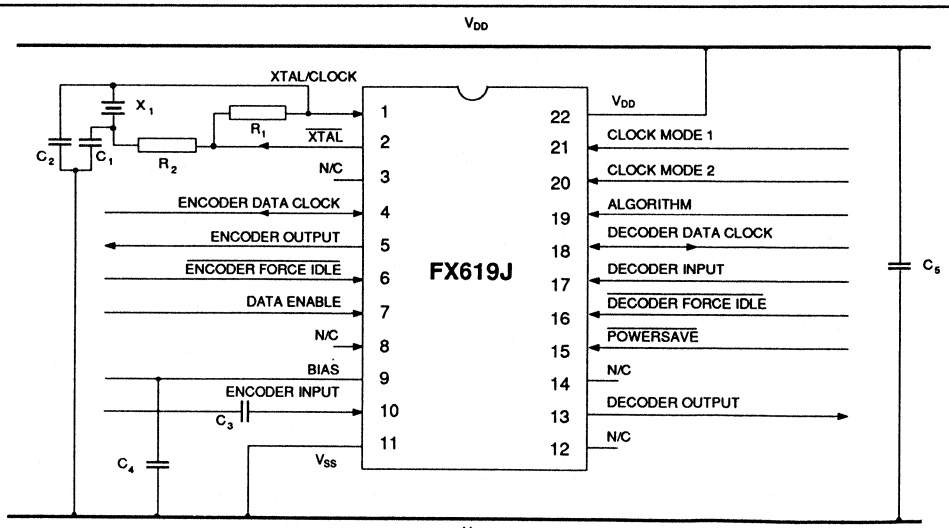
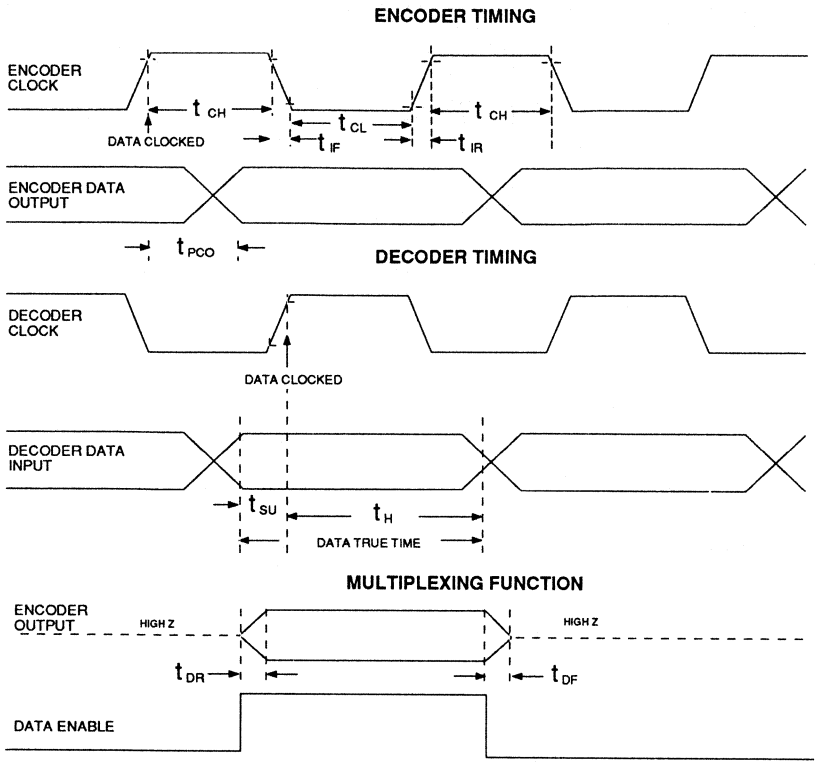



*Fig.3 Recommended External Components*

## Codec Timing Information




**TIMING**

$t_{CH}$ Clock '1' Pulse Width 1.0µs Min.

$t_{CL}$ Clock '0' Pulse Width 1.0µs Min.

$t_{IR}$ Clock Rise Time 100ns Typ.

$t_{IF}$ Clock Fall Time 100ns Typ.

$t_{SU}$ Data Set-up Time 450ns Min.

$t_{H}$ Data Hold Time 600ns Min.

$t_{SU} + t_{H}$ Data True Time.

$t_{PCO}$ Clock to Output Delay time 750ns Max.

$t_{DR}$ Data Rise Time 100ns Typ.

$t_{DF}$ Data Fall Time 100ns Typ.

Xtal Input Frequency 1.024MHz.

*Fig.4 Codec Timing Diagrams*

**Codec Performance** Using the Bit Sequence Tests (a to g) at the Decoder Input pin in accordance with the Eurocom Specification D1 – IA8, the decoder output is as shown in Table 1.

| Test | Sample Rate | Bit Sequence at Decoder Input | MLA Duty cycle | Typical Output Level |
|---|---|---|---|---|
| a. | 16kbit/s | 10110100100100101101 | 0 | - 41.5dBm0 |
| | 32kbit/s | 10110110101010010010010010010101011101101 | 0 | - 42.0dBm0 |
| b. | 16kbit/s | 11011001001001001101 | 0.05 | - 25.0dBm0 |
| | 32kbits | 10110110101010010010001001001010110110 11 | 0.05 | - 25.0dBm0 |
| c. | 16kbits | 10110101000100101011 | 0.1 | - 19.0dBm0 |
| | 32kbit/s | 11011011010100100010001001001010110111 01 | 0.1 | - 18.5dBm0 |
| d. | 16kbit/s | 11011001000010011011 | 0.2 | - 11.0dBm0 |
| | 32kbit/s | 11011101100101000100001000100110101110 11 | 0.2 | - 11.5dBm0 |
| e. | 16kbit/s | 11011010000010010111 | 0.3 | - 6.5dBm0 |
| | 32kbit/s | 11101110110010001000000100010011011101 11 | 0.3 | - 6.5dBm0 |
| f. | 16kbit/s | 11011010000001001111 | 0.4 | - 3.0dBm0 |
| | 32kbit/s | 11110111010100010000000010001010111011 11 | 0.4 | - 3.0dBm0 |
| g. | 16kbit/s | 11101010000000101111 | 0.5 | 0dBm0 |
| | 32kbit/s | 11111011101000100000000001000101110111 11 | 0.5 | 0dBm0 |

*Table 1 Bit Sequence Test Table*

**Codec Performance...** relative to the Eurocom Specification D1 - IA8

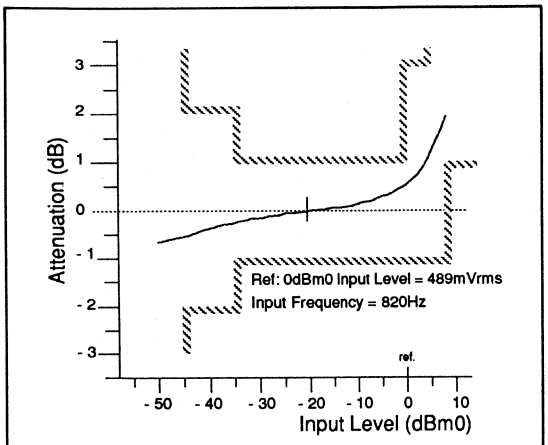



*Fig.5 Gain vs Input Level (16kbit/s)*

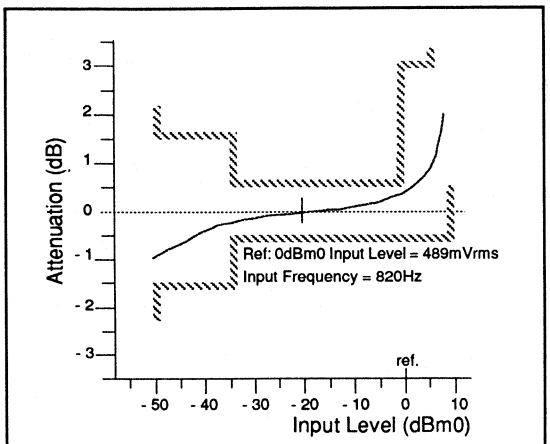



*Fig.6 Gain vs Input Level (32kbit/s)*

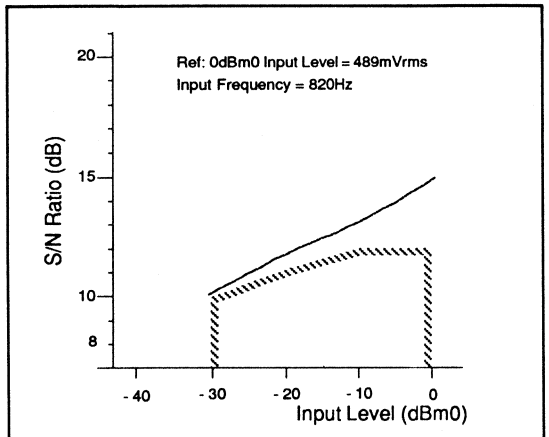



*Fig.7 S/N vs Input Level (16kbit/s)*

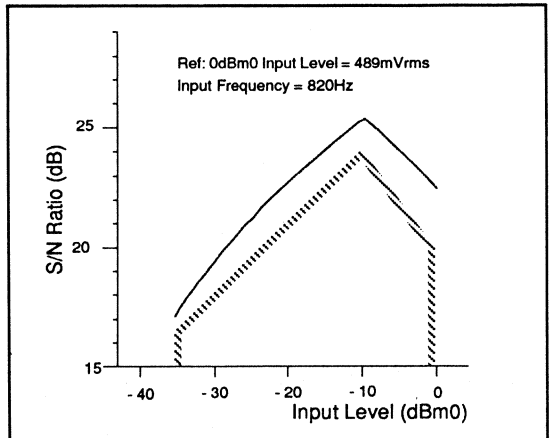



*Fig.8 S/N vs Input Level (32kbit/s)*

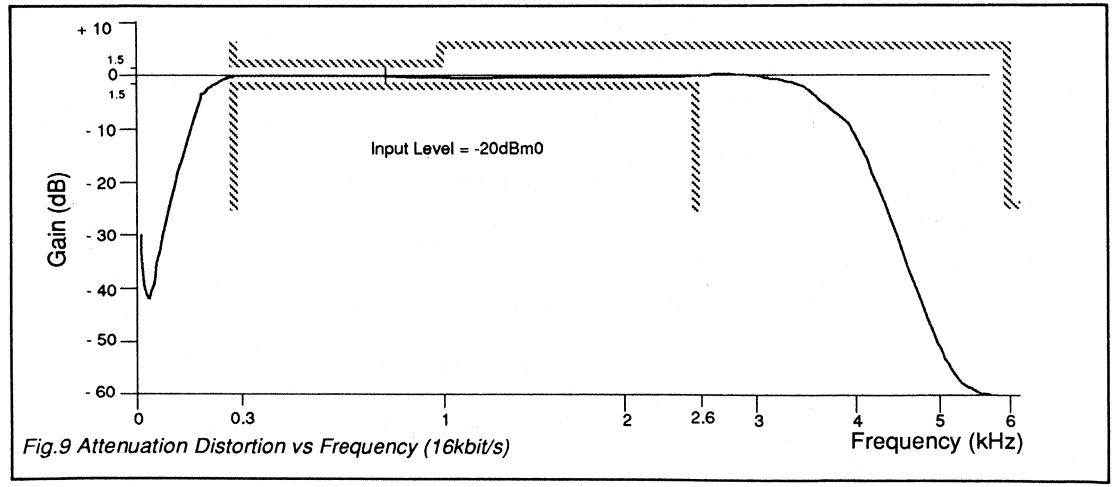



*Fig.9 Attenuation Distortion vs Frequency (16kbit/s)*

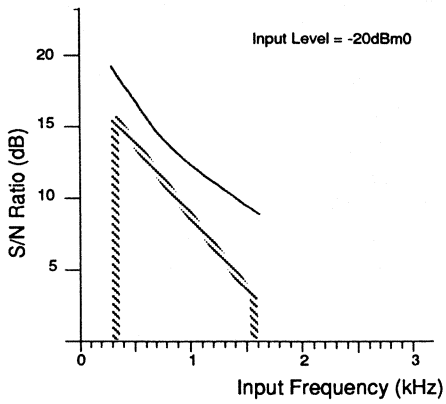



*Fig.10 S/N vs Input Frequency (16kbit/s)*

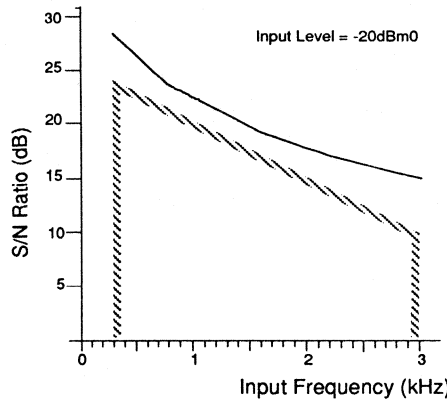



*Fig.11 S/N vs Input Frequency (32kbit/s)*

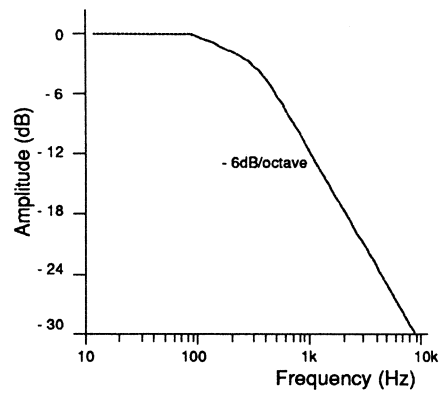



*Fig.12 Principal Integrator Response*

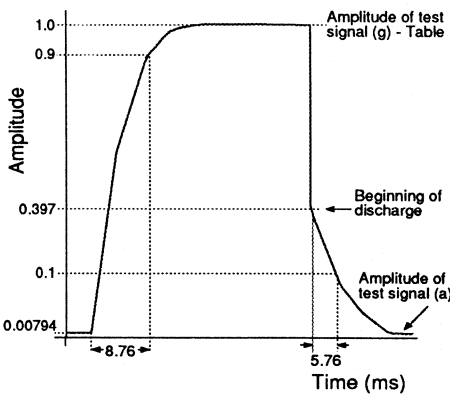



*Fig.13 Compand Envelope*

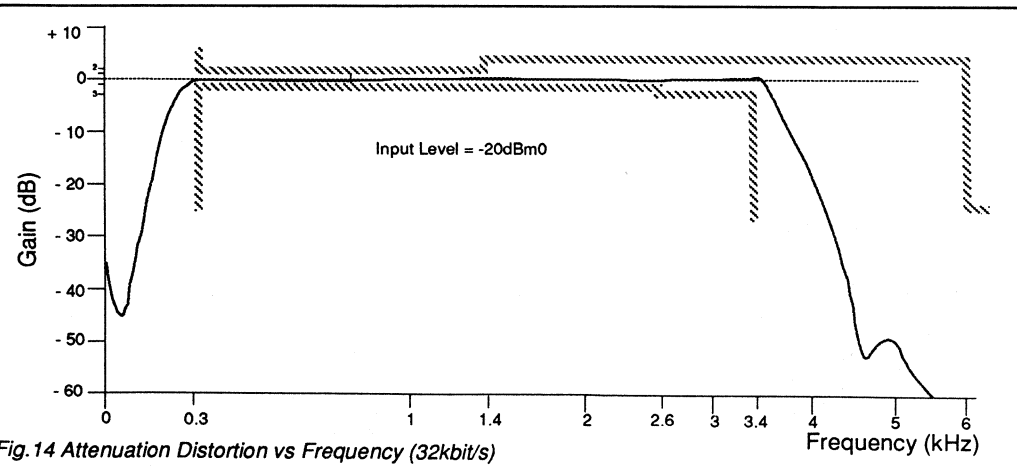



*Fig.14 Attenuation Distortion vs Frequency (32kbit/s)*

# Specifications

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Source/sink current (supply pins) | | ± 30mA |
| (other pins) | | ± 20mA |
| Total device dissipation @ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX619J** | -40°C to +85°C (cerdip) |
| | **FX619M1** | -40°C to +85°C (cerquad) |
| Storage temperature range: | **FX619J** | -55°C to +125°C (cerdip) |
| | **FX619M1** | -55°C to +125°C (cerquad) |

## Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C, Xtal/Clock $f_0$ = 1.024MHz, Audio Level 0dB ref (0dBm0) = 489 mV rms.
Audio Test Frequency = 820 Hz. Sample Clock Rate = 32kb/s. Compand Algorithm = 3-bit.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | 1 | 4.5 | 5.0 | 5.5 | V |
| Supply Current (Enabled) | | – | 4.5 | – | mA |
| Supply Current (Powersave) | | – | 1.0 | – | mA |
| Inputs Logic '1' | 8 | 3.5 | – | – | V |
| Inputs Logic '0' | 8 | – | – | 1.5 | V |
| Outputs Logic '1' | 8 | 4.0 | – | – | V |
| Outputs Logic '0' | 8 | – | – | 1.0 | V |
| Digital Input Impedance (Logic I/O pins) | | 1.0 | 10 | – | MΩ |
| Digital Input Impedance (Logic input pins, pullup resistor) | 2 | 300 | – | – | kΩ |
| Digital Output Impedance | | – | – | 4 | kΩ |
| Analogue Input Impedance | 4 | | 1 | – | kΩ |
| Analogue Output Impedance | 7 | – | – | 800 | Ω |
| Three State Output Leakage Current (output disabled) | | -4 | – | +4 | µA |
| Insertion Loss | 3 | -2 | – | +2 | dB |
| **Dynamic Values** | 1 | | | | |
| **Encoder:** | | | | | |
| Analogue Signal Input Levels | 5,9 | -35 | – | +6 | dBm0 |
| Principle Integrator Frequency | | – | 275 | – | Hz |
| Encoder Passband | | | 3400 | | Hz |
| Compand Time Constant | | – | 4 | – | ms |
| **Decoder:** | | | | | |
| Analogue Signal Output Levels | 5,9 | -35 | – | +6 | dBm0 |
| Decoder Passband | | 300 | – | 3400 | Hz |
| **Encoder Decoder (Full codec):** | | | | | |
| Compression Ratio (Cd = 0.5 to Cd = 0.0) | | – | 50 | – | |
| Passband | | 300 | – | 3400 | Hz |
| Stopband | | 6 | – | 10 | kHz |
| Stopband Attenuation | | – | 60 | – | dB |
| Passband Gain | | – | 0 | – | dB |
| Passband Ripple (300Hz –1400Hz) | | -1 | – | +1 | dB |
| (1400Hz – 2600Hz) | | -1 | – | +3 | dB |
| (2600Hz – 3400Hz) | | -2 | – | +3 | dB |
| Output Noise (Input short circuit) | 9 | – | – | -62 | dBm0p |
| Perfect Idle Channel Noise (Encoder forced) | 9 | – | -63 | – | dBm0p |
| Group Delay Distortion | 6 | | | | |
| (1000Hz to 2600Hz) | | – | – | 450 | µs |
| (600Hz to 2800Hz) | | – | – | 750 | µs |
| (500Hz to 3000Hz) | | – | – | 1.5 | ms |
| Xtal/Clock Frequency | | 500 | 1024 | 1500 | kHz |

› › › ›

# Specifications

## Process Information

The following Table gives details of the process and test controls employed in the manufacture of the FX619 Eurocom Delta Codec.

| Function | Reference | Remarks |
|---|---|---|
| Hermeticity | | |
| Fine Leak Test – | Mil Std 883C | using Method 1014 – test condition A1. |
| Coarse Leak Test – | Mil Std 883C | using Method 1014 – test condition C. |
| Burnin | Mil Std 883C | using Method 1015 – test condition E.<br>168 Hours @ 85°C with 5v power, and clocks applied. |
| Temperature Cycling | Mil Std 883C | using Method 1010 – test condition B.<br>10 cycles -55°C to +125°C. |
| The following mechanical assembly tests are Qualified to BS9450 | | |
| Vibration | BS9450 | Section 1.2.6.8.1<br>55Hz to 500Hz at 98 m/sec acceleration. |
| Shock | BS9450 | Section 1.2.6.6<br>981 m/sec for 6 msec. |
| Low Pressure | BS9450 | Section 1.2.6.12 |
| Transport and Storage – | | 225mmHg (altitude 9000m). |
| Operation – | | 600mmHg (altitude 2400m). |
| Humidity | BS9450 | Section 1.2.6.4<br>96 Hours @ 45°C, 95% relative humidity plus condensed water. |

**Notes:**
1. Dynamic characteristics are specified at 5V unless otherwise specified.
2. All logic inputs except, Encoder and Decoder Data Clocks.
3. For an Encoder/Decoder combination, Insertion Loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 5, 6, 7 and 8.
6. Group Delay Distortion for the full codec is relative to the delay with 820Hz, -20dB at the encoder input.
7. An Emitter Follower output stage.
8. 4V = 80% $V_{DD}$, 3.5V = 70% $V_{DD}$, 1.5V = 30% $V_{DD}$, 1V = 20% $V_{DD}$.
9. Analogue Voltage Levels used in this Data Sheet: 0dBm0 = 489mVrms = - 4dBm = 0dB. - 20dBm0 = 49mVrms = - 24dBm.

## Application Recommendations

Due to the very low levels of signal and idle channel noise specified in the Eurocom Basic Parameters Specification D1 – IA8 – a noisy or badly regulated power supply could cause instability putting the overall system performance out of specification. Adherence to the points noted below will assist in minimizing this problem.

(a) Care should be taken on the design and layout of the printed circuit board.

(b) All external components (as recommended in Figure 3) should be kept close to the package.

(c) Tracks should be kept short, particularly the Encoder Input capacitor and the $V_{BIAS}$ capacitor.

(d) Xtal/clock tracks should be kept well away from analogue inputs and outputs.

(e) Inputs and outputs should be screened wherever possible.

(f) A "ground plane" connected to $V_{SS}$ will assist in eliminating external pick-up on the input and output pins.

(g) It is recommended that the power supply rails have less than 1mVrms of noise allowed.

(h) The source impedance to the Encoder Input pin must be less than 100Ω, Output Idle channel noise levels will improve with even lower source impedances.

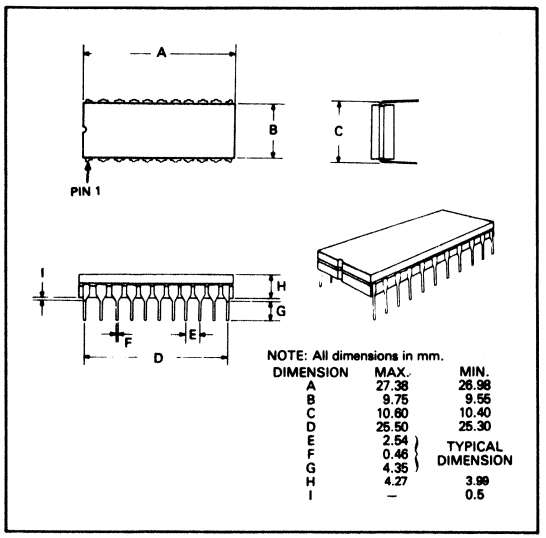
## Package Outline

The FX619J cerdip package is shown in Figure 15 with the FX619M1 package shown in Figure 16 .
To ensure correct pin identification, the FX619M1 package has a relieved corner between pins 4 and 5. Pins number anti-clockwise when viewed from the top.

## Handling Precautions

The FX619 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

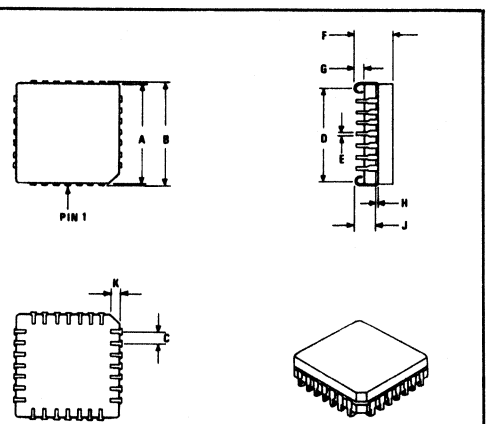
*Fig. 15* **FX619J** *DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 | TYPICAL DIMENSION |
| F | 0.46 | TYPICAL DIMENSION |
| G | 4.35 | TYPICAL DIMENSION |
| H | 4.27 | 3.99 |
| I | — | 0.5 |

*Fig. 16* **FX619MI** *CLCC Package*




NOTE: All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 11.60 | 11.35 |
| B | 12.15 | 12.05 |
| C | 1.27 TYPICAL | |
| D | 10.82 | 10.63 |
| E | 0.46 TYPICAL | |
| F | 4.38 | 4.20 |
| G | 1.15 | 1.05 |
| H | 0.50 TYPICAL | |
| J | 2.76 | 2.60 |
| K | 45° TYPICAL | |

## Ordering Information

**FX619J 22-pin cerdip DIL**
**FX619M1 28-lead ceramic, leaded chip carrier (CLCC)**

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX629 Delta Modulation Codec for Military Applications

Publication D/629/1 December 1989
Provisional Issue

## Features/Applications

- **Designed to Meet Mil-Std-188-113**
- **Military Communications**
- **Delta MUX, Switch and Phone Applications**
- **Single-Chip Full-Duplex Codec**
- **On-Chip Input and Output Filters**
- **Programmable Sampling Clocks**
- **3 or 4-bit Compand Algorithm**
- **Forced Idle Facility**
- **Powersave Facility**
- **Single 5V CMOS Process**
- **Full-Duplex CVSD* Codec**

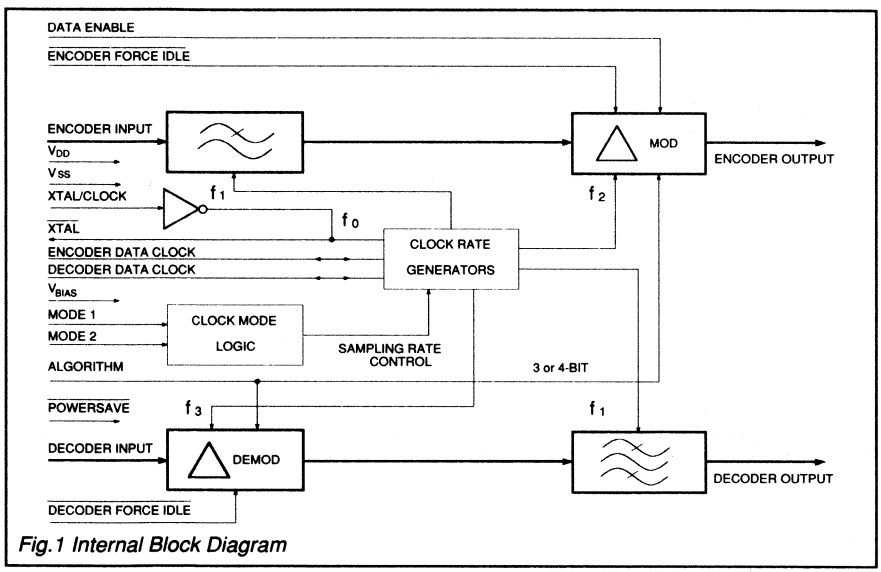



*Fig.1 Internal Block Diagram*

FX629

## Brief Description

The FX629 is an LSI circuit designed as a *Continuously Variable Slope Delta Codec and is intended for use in military communications systems.

Designed to meet Mil-Std-188-113 with external components, the device is suitable for applications in military Delta Multiplexers, switches and phones.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32 or 64 k bits/second from an internal clock generator or may be externally applied in the range 8 to 64 k bits/second. Sampling clock frequencies are output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications.

Encoder and Decoder forced idle facilities are provided, forcing a 10101010..... pattern in encode and a $V_{DD}/2$ bias in decode.

The companding circuits may be operated with a pin-selected 3 or 4-bit algorithm.

The powersave facility puts the device into the standby mode thereby reducing current consumption when not operating.

A reference 1.024MHz oscillator uses an external clock pulse or Xtal input.

The FX629 is a low-power, 5 volt CMOS device and is available in 22-pin cerdip DIL and 28-lead ceramic leadless SMT packages.

## Pin Number Function

| FX629J | FX629M1 | |
|---|---|---|
| 1 | 1 | **Xtal/Clock :** Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3. |
| | 2 | No connection |
| 2 | 3 | **$\overline{\text{Xtal}}$ :** Output of clock oscillator inverter. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986. |
| 3 | 4 | No connection |
| 4 | 5 | **Encoder Data Clock :** A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependant upon clock mode 1, 2 inputs and Xtal frequency (see Clock Mode pins). |
| 5 | 6 | **Encoder Output :** The encoder digital output, this is a three state output whose condition is set by Data Enable and Powersave inputs as shown : |
| | 7, 8 | No connection |
| 6 | 9 | **$\overline{\text{Encoder Force Idle}}$ :** When this pin is a logical '0' the encoder is forced to an idle state and the encoder digital output is 0101..., a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup. |
| 7 | 10 | **Data Enable :** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup. |
| 8 | 11 | No connection |
| 9 | 12 | **Bias :** Normally at $V_{DD}$ /2 bias, this pin requires to be externally decoupled by a capacitor, $C_4$. Internally pulled to $V_{SS}$ when "Powersave" is a logical '0'. |
| 10 | 13 | **Encoder Input :** The analogue signal input. Internally biased at $V_{DD}$ /2, external components are required on this input. The source impedance should be less than 100Ω, output idle channel noise levels will improve with an even lower source impedance. See Fig. 3. |
| 11 | 14 | **$V_{SS}$ :** Negative Supply. |

| Data Enable | $\overline{\text{Powersave}}$ | Encoder Output |
|---|---|---|
| 1 | 1 | Enabled |
| 0 | 1 | High Z (o/c) |
| 1 | 0 | Vss |

## Pin Number Function

| FX629J | FX629M1 | |
|---|---|---|
| 12 | 15,16 | No connection |
| 13 | 17 | **Decoder Output :** The recovered analogue signal is output at this pin, it is the buffered output of a bandpass filter and requires external components. During "Powersave" this output is o/c. |
| 14 | 18,19 | No connection |
| 15 | 20 | $\overline{\text{Powersave}}$ **:** A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup. |
| | 21 | No connection |
| 16 | 22 | $\overline{\text{Decoder Force Idle}}$ **:** A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the decoder output goes to $V_{DD}/2$. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup. |
| 17 | 23 | **Decoder Input :** The received digital signal input. Internal 1MΩ Pullup. |
| 18 | 24 | **Decoder Data Clock :** A Logic I/O port. External decode clock input or internal data clock output, dependant upon clock mode 1, 2 inputs, see Clock Mode pins. |
| 19 | 25 | **Algorithm :** A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup. |
| 20 | 26 | **Clock Mode 2 :** |
| 21 | 27 | **Clock Mode 1 :** Internal 1MΩ Pullups. |

| Clock Mode 1 | Clock Mode 2 | Facility |
|---|---|---|
| 0 | 0 | External clocks |
| 0 | 1 | Internal, 64kb/s = f ÷ 16 |
| 1 | 0 | Internal, 32kb/s = f ÷ 32 |
| 1 | 1 | Internal, 16kb/s = f ÷ 64 |

Clock rates refer to f = 1.024 MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization.
Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Optimum performance will be achieved when the applied external clocks are synchronous with the master Xtal/clock, and a sub-multiple of 128kHz.

| | | |
|---|---|---|
| 22 | 28 | $V_{DD}$ **:** Positive Supply. A single + 5 volt power supply is required. |

# Codec Integration

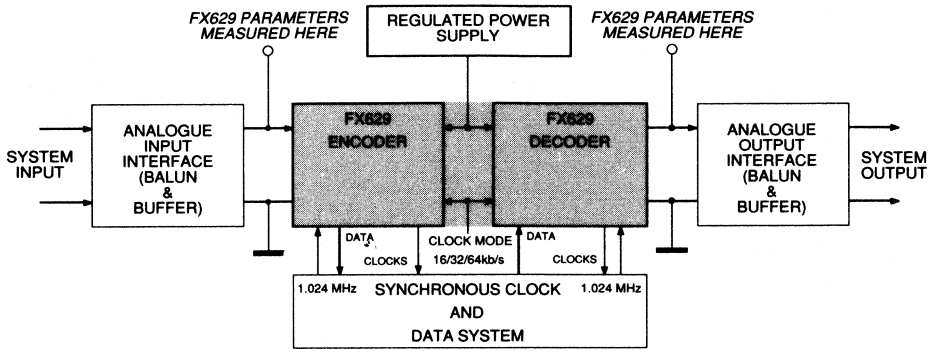



*Fig.2 System Configuration Diagram – showing the FX629, which with the indicated interfacing, will conform to the Mil-Std-188-113 Specification*

| Component | Unit Value | **Note** – with reference to Figure 3 (below) |
|---|---|---|
| $R_1$ | 1M | Oscillator Inverter bias resistor. |
| $R_2$ | Selectable | Xtal Drive limiting resistor. |
| $C_1$ | 33p | Xtal Circuit drain capacitor. |
| $C_2$ | 33p | Xtal Circuit gate capacitor. |
| $C_3$ | 1.0µ | Encoder Input coupling capacitor – The drive source impedance to this input should be less than 100Ω. Output Idle channel noise levels will improve with an even lower source impedance. |
| $C_4$ | 1.0µ | Bias decoupling capacitor. |
| $C_5$ | 1.0µ | $V_{DD}$ decoupling capacitor. |
| $X_1$ | 1.024 MHz | A 1.024 MHz Xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with CML application note D/XT/1 April 1986. |

Tolerance :– Resistors ± 10% Capacitors ± 20%

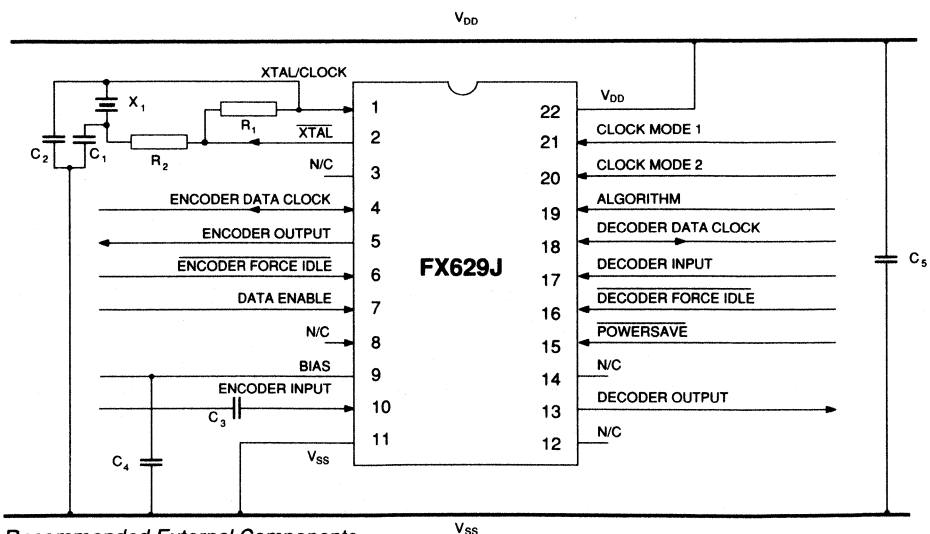
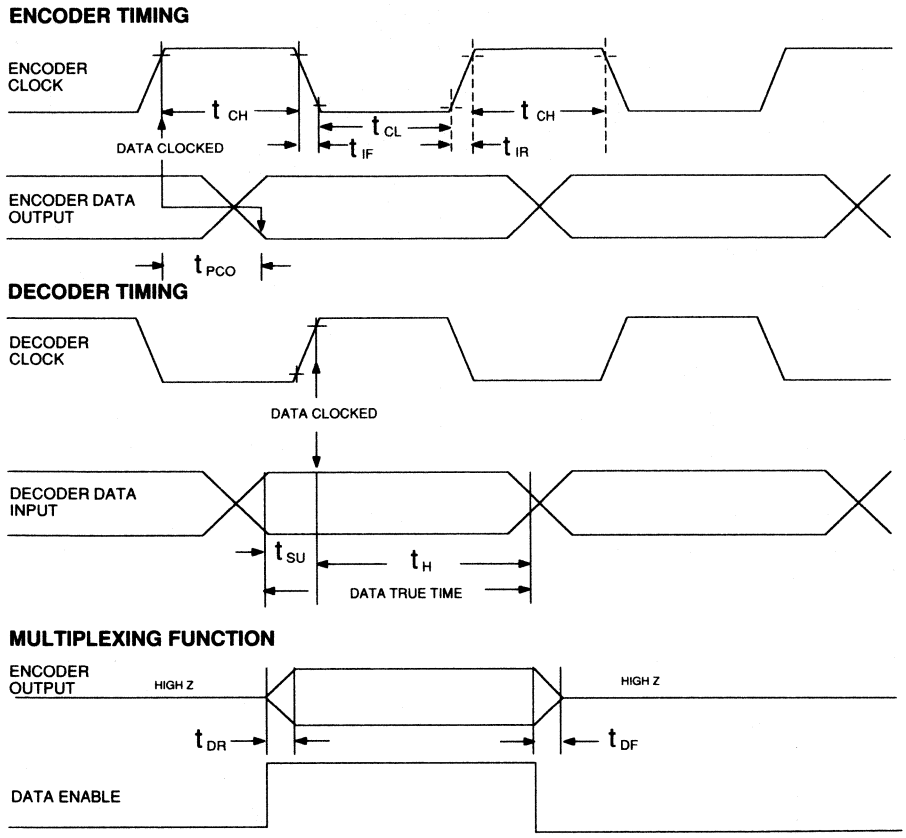



*Fig.3 Recommended External Components*

## Codec Timing Information




**TIMING**

| | | | |
|---|---|---|---|
| $t_{CH}$ **Clock '1' Pulse Width** 1.0µs Min. | $t_{IR}$ **Clock Rise Time** 100ns Typ. | $t_{SU}$ **Data Set-up Time** 450ns Min. | $t_{SU} + t_H$ **= Data True Time** |
| $t_{CL}$ **Clock '0' Pulse Width** 1.0µs Min. | $t_{IF}$ **Clock Fall Time** 100ns Typ. | $t_H$ **Data Hold Time** 600ns Min. | $t_{PCO}$ **Clock to Output Delay Time** 750ns Max. |
| | $t_{DR}$ **Data Rise Time** 100ns Typ. | $t_{DF}$ **Data Fall Time** 100ns Typ. | **Xtal Input Frequency** 1.024MHz. |

*Fig.4 Codec Timing Diagrams*

**Digital to Analogue Performance .....** Using the bit sequence tests shown in Table 1 (below) at the Decoder Input pin, the analogue signals measured at the Decoder Output pin are 800Hz ± 10Hz at the levels described.

| Sample Rate | Bit Sequence at Decoder Input | "Run of Threes" *(%)* | Output Level *(dBm0)* |
|---|---|---|---|
| 16kbit/s | 11011011010010010010 | 0 | -29.2 ± 2 |
| 32kbit/s | 11011011010101001001001001001010101101101 10 | 0 | -30.0 ± 2 |
| 16kbit/s | 1111101101000010010 | 30 | 0 ± 1 |
| 32kbits | 11111101101010100001000000100101010111101 10 | 30 | 0 ± 1 |

*Table 1 Bit Sequence Tests and Results* at 800Hz

## **Typical Codec Performance .....** relative to the Mil-Std-188-113 Specification

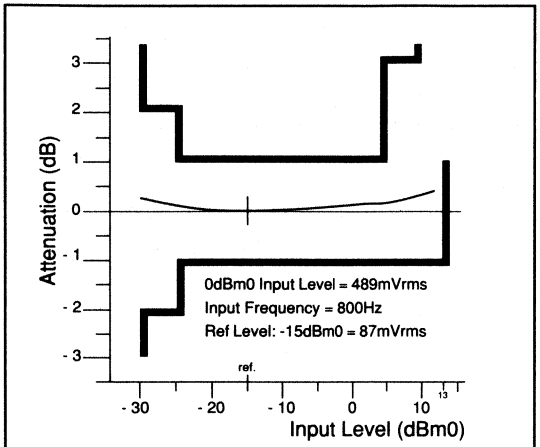



*Fig.5 Gain vs Input Level (16kbit/s)*

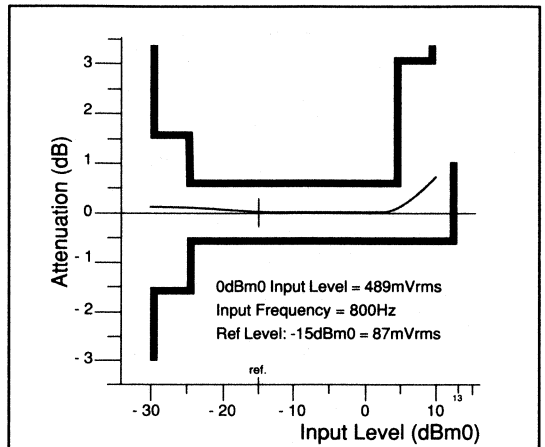



*Fig.6 Gain vs Input Level (32kbit/s)*

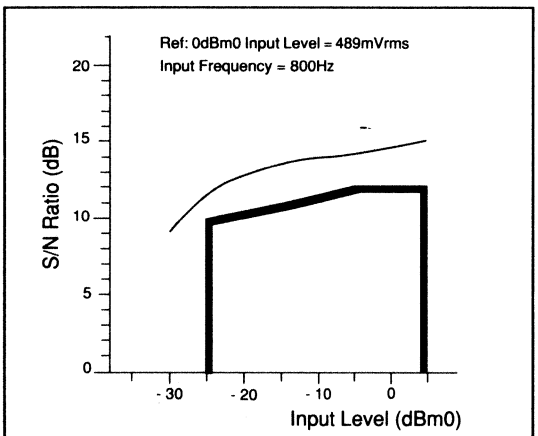



*Fig.7 S/N vs Input Level (16kbit/s)*

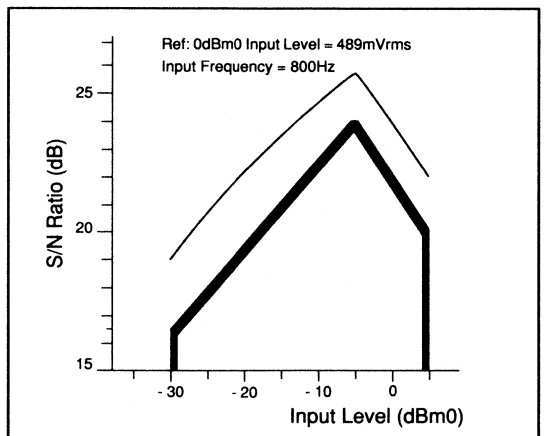



*Fig.8 S/N vs Input Level (32kbit/s)*

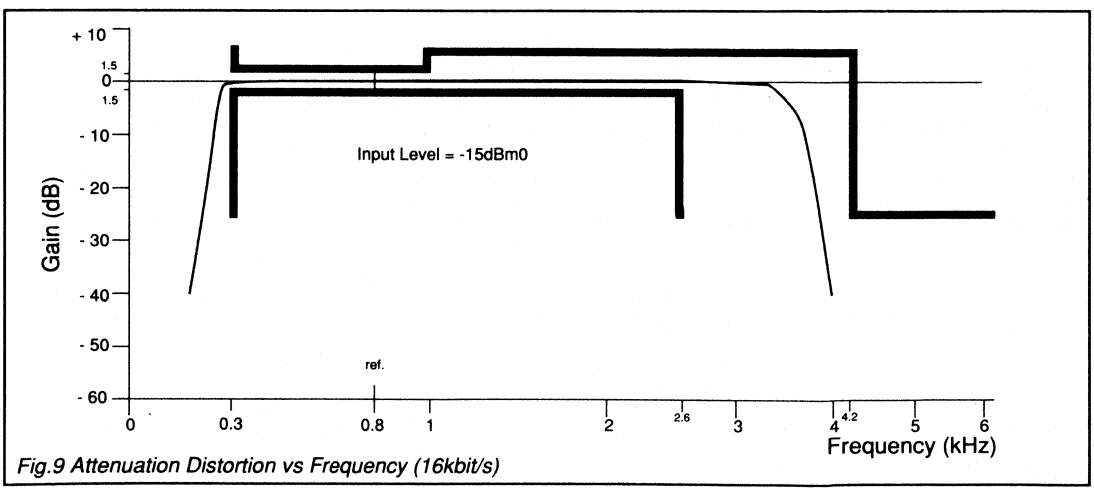



*Fig.9 Attenuation Distortion vs Frequency (16kbit/s)*

## **Typical Codec Performance .....** relative to the Mil-Std-188-113 Specification

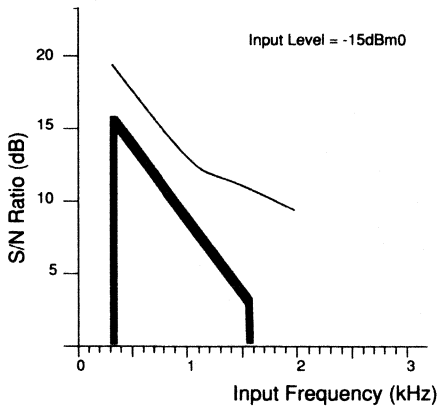



*Fig.10 S/N vs Input Frequency (16kbit/s)*

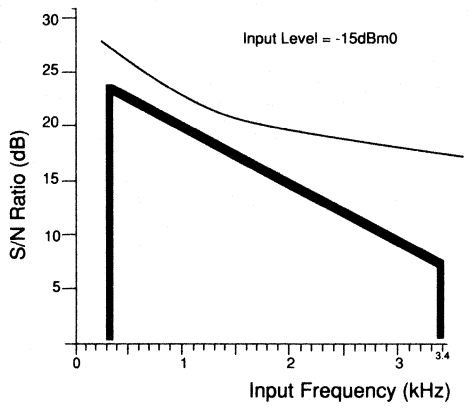



*Fig.11 S/N vs Input Frequency (32kbit/s)*

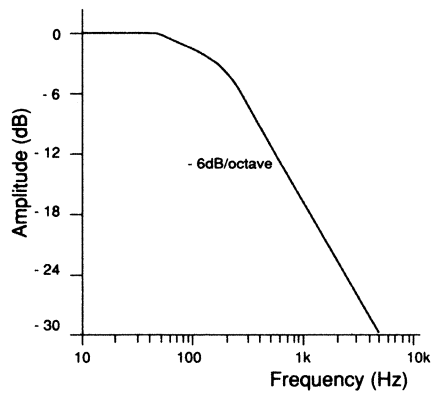



*Fig.12 Principal Integrator Response*

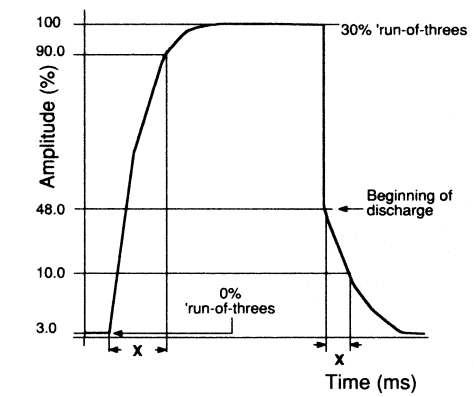



*Fig.13 Compand Envelope*

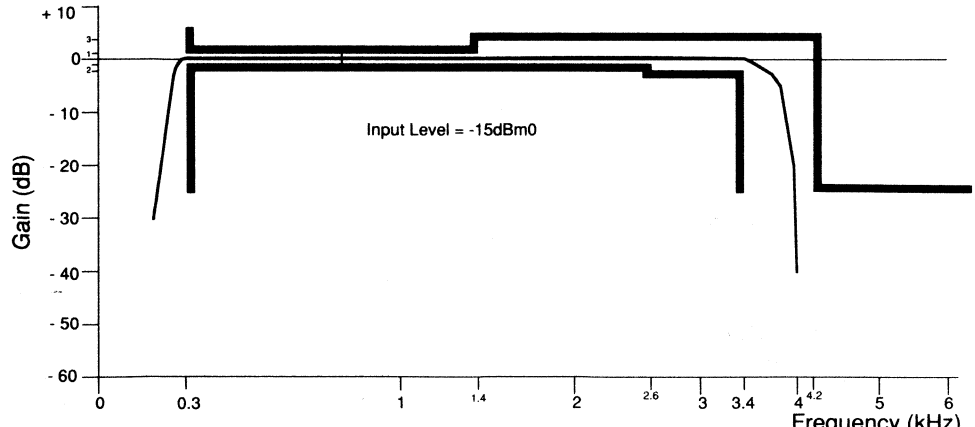



*Fig.14 Attenuation Distortion vs Frequency (32kbit/s)*

# Specifications

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Source/sink current (supply pins) | | ± 30mA |
| (other pins) | | ± 20mA |
| Total device dissipation @ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX629J** | -40°C to +85°C (cerdip) |
| | **FX629M1** | -40°C to +85°C (cerquad) |
| Storage temperature range: | **FX629J** | -55°C to +125°C (cerdip) |
| | **FX629M1** | -55°C to +125°C (cerquad) |

## Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C, Xtal/Clock $f_0$ = 1.024MHz, Audio Level 0dB ref (0dBm0) = 489 mV rms.
Audio Test Frequency = 800 Hz. Sample Clock Rate = 32kb/s. Compand Algorithm = 3-bit.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | 1 | 4.5 | 5.0 | 5.5 | V |
| Supply Current (Enabled) | | – | 5.5 | – | mA |
| Supply Current (Powersave) | | – | 0.4 | – | mA |
| Inputs Logic '1' | 8 | 3.5 | – | – | V |
| Inputs Logic '0' | 8 | – | – | 1.5 | V |
| Outputs Logic '1' | 8 | 4.0 | – | – | V |
| Outputs Logic '0' | 8 | – | – | 1.0 | V |
| Digital Input Impedance (Logic I/O pins) | | 1.0 | 10.0 | – | MΩ |
| Digital Input Impedance (Logic input pins, pullup resistor) | 2 | 300 | – | – | kΩ |
| Digital Output Impedance | | – | – | 4 | kΩ |
| Analogue Input Impedance | 4 | – | 1.0 | – | kΩ |
| Analogue Output Impedance | 7 | – | – | 800 | Ω |
| Three State Output Leakage Current (output disabled) | | -4.0 | – | +4.0 | µA |
| Insertion Loss | 3 | -2.0 | – | +2.0 | dB |
| **Dynamic Values** | 1,9 | | | | |
| **Encoder:** | | | | | |
| Analogue Signal Input Levels | 5,9 | -35.0 | – | +12.0 | dBm0 |
| Principle Integrator Frequency | | 127 | 159 | 212 | Hz |
| Encoder Passband | | | 3400 | | Hz |
| Compand Time Constant | | 4.0 | 5.0 | 6.0 | ms |
| **Decoder:** | | | | | |
| Analogue Signal Output Levels | 5,9 | -35.0 | – | +12.0 | dBm0 |
| Decoder Passband | | 300 | – | 3400 | Hz |
| **Encoder Decoder (Full codec):** | | | | | |
| Compression Ratio (Cd = 0.3 to Cd = 0.0) | | – | 16:1 | – | |
| Passband | | 300 | – | 3400 | Hz |
| Stopband | | 4.2 | – | – | kHz |
| Stopband Attenuation (4200Hz to 6000Hz) | | 25.0 | – | – | dB |
| (> 6kHz) | | – | 60.0 | – | dB |
| Passband Gain | | – | 0 | – | dB |
| Passband Ripple (300Hz –1400Hz) | | -1.0 | – | +1.0 | dB |
| (1400Hz – 2600Hz) | | -1.0 | – | +3.0 | dB |
| (2600Hz – 3400Hz) | | -2.0 | – | +3.0 | dB |
| Output Noise (Input short circuit) | 9 | – | -55.0 | – | dBm0 |
| Perfect Idle Channel Noise (Encoder forced) | 9 | – | -57.0 | – | dBm0 |
| Group Delay Distortion | 6 | | | | |
| (1000Hz to 2600Hz) | | – | – | 450 | µs |
| (600Hz to 2800Hz) | | – | – | 750 | µs |
| (500Hz to 3000Hz) | | – | – | 1.5 | ms |
| Xtal/Clock Frequency | | – | 1024 | – | kHz |

# Specifications .....

## Process Information

The following Table gives details of the process and test controls employed in the manufacture of the FX629 'Mil Std' Delta Codec.

| Function | Reference | Remarks |
|---|---|---|
| Hermeticity | | |
| Fine Leak Test – | Mil Std 883C | using Method 1014 – test condition A1. |
| Coarse Leak Test – | Mil Std 883C | using Method 1014 – test condition C. |
| Burnin | Mil Std 883C | using Method 1015 – test condition E.<br>168 Hours @ 85°C with 5v power, and clocks applied. |
| Temperature Cycling | Mil Std 883C | using Method 1010 – test condition B.<br>10 cycles -55°C to +125°C. |
| The following mechanical assembly tests are Qualified to BS9450 | | |
| Vibration | BS9450 | Section 1.2.6.8.1<br>55Hz to 500Hz at 98 m/sec acceleration. |
| Shock | BS9450 | Section 1.2.6.6<br>981 m/sec for 6 msec. |
| Low Pressure | BS9450 | Section 1.2.6.12 |
| Transport and Storage – | | 225mmHg (altitude 9000m). |
| Operation – | | 600mmHg (altitude 2400m). |
| Humidity | BS9450 | Section 1.2.6.4<br>96 Hours @ 45°C, 95% relative humidity plus condensed water. |

**Notes:**
1. Dynamic characteristics are specified at 5V unless otherwise specified.
2. All logic inputs except, Encoder and Decoder Data Clocks.
3. For an Encoder/Decoder combination, insertion loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 5, 6, 7 and 8.
6. Group Delay Distortion for the full codec is relative to the delay with 820Hz, -20dB at the encoder input.
7. An Emitter Follower output stage.
8. 4.0V = 80% $V_{DD}$, 3.5V = 70% $V_{DD}$, 1.5V = 30% $V_{DD}$, 1.0V = 20% $V_{DD}$.
9. Analogue Voltage Levels used in this Data Sheet: 0dBm0 = 489mVrms = - 4dBm = 0dB. -15dBm0 = 87mVrms. - 20dBm0 = 49mVrms = - 24dBm.

## Application Recommendations

Due to the very low levels of signal and idle channel noise required in Military applications – a noisy or badly regulated power supply could cause instability putting the overall system performance out of specification. Adherence to the points noted below will assist in minimizing this problem.

(a) Care should be taken on the design and layout of the printed circuit board.

(b) All external components (as recommended in Figure 3) should be kept close to the package.

(c) Tracks should be kept short, particularly the Encoder Input capacitor and the $V_{BIAS}$ capacitor.

(d) Xtal/clock tracks should be kept well away from analogue inputs and outputs.

(e) Inputs and outputs should be screened wherever possible.

(f) A "ground plane" connected to $V_{SS}$ will assist in eliminating external pick-up on the input and output pins.

(g) It is recommended that the power supply rails have less than 1mVrms of noise allowed.

(h) The source impedance to the Encoder Input pin must be less than 100Ω, Output Idle channel noise levels will improve with even lower source impedances.

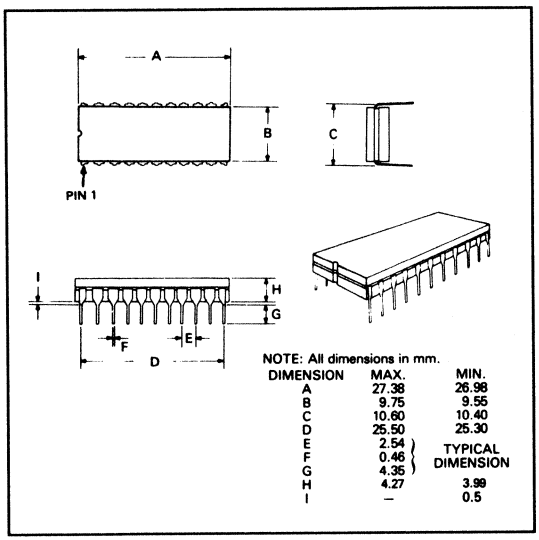
## Package Outline

The FX629J cerdip package is shown in Figure 15 with the FX629M1 ceramic package shown in Figure 16 .
To ensure correct pin identification, the FX629M1 package has a relieved corner between pins 4 and 5. Pins number anti-clockwise when viewed from the top.

## Handling Precautions

The FX629 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

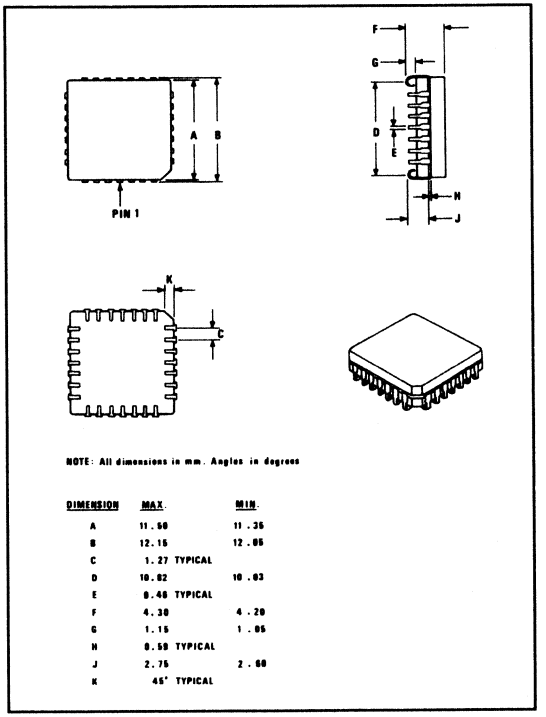
*Fig.15* ***FX629J DIL Package***




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 } | TYPICAL |
| F | 0.46 } | DIMENSION |
| G | 4.35 } | |
| H | 4.27 | 3.99 |
| I | – | 0.5 |

*Fig.16* ***FX629M1 CLCC Package***




NOTE: All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 11.60 | 11.35 |
| B | 12.15 | 12.05 |
| C | 1.27 TYPICAL | |
| D | 10.82 | 10.03 |
| E | 0.48 TYPICAL | |
| F | 4.30 | 4.20 |
| G | 1.15 | 1.05 |
| H | 0.59 TYPICAL | |
| J | 2.75 | 2.60 |
| K | 45° TYPICAL | |

## Ordering Information

**FX629J 22-pin cerdip DIL**

**FX629M1 28-lead ceramic, leaded chip carrier (CLCC)**

# Integrated Circuits Data Book

Section 5

# Cordless Telephone

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX118 Duplex Frequency Inverter for Cordless Telephones

Publication D/118/2 February 1993
Provisional Issue

## Features/Applications

- **Frequency Inversion Scrambling**
- **Full-Duplex Operation**
- **High Baseband and Carrier Rejection**
- **Audio Lowpass and Bandpass Filtering On-Chip**
- **Xtal Oscillator Stabilty**
- **Low Power Requirement** *(3.0 Volt Minimum)*
- **Cordless Telephones**
- **Base and Handheld Applications**
- **Input Gain Adjustment**
- **Plastic DIL and S.O.I.C. Package Styles**

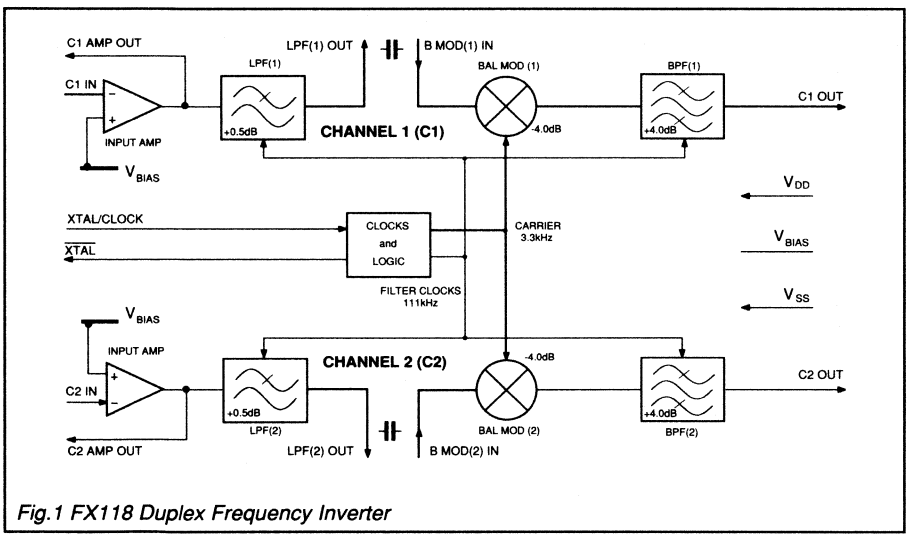



*Fig.1 FX118 Duplex Frequency Inverter*

FX118

## Brief Description

The FX118 is a low-power, full-duplex frequency inverter available to provide voice privacy for cordless telephone systems by mixing the incoming audio with an internally produced carrier frequency (3.3kHz).

This chip contains two completely separate audio channels (C1 and C2) each comprising a "component-adjustable" input amplifier, a 10th-order lowpass filter, a balanced modulator and a 14th-order bandpass filter output.

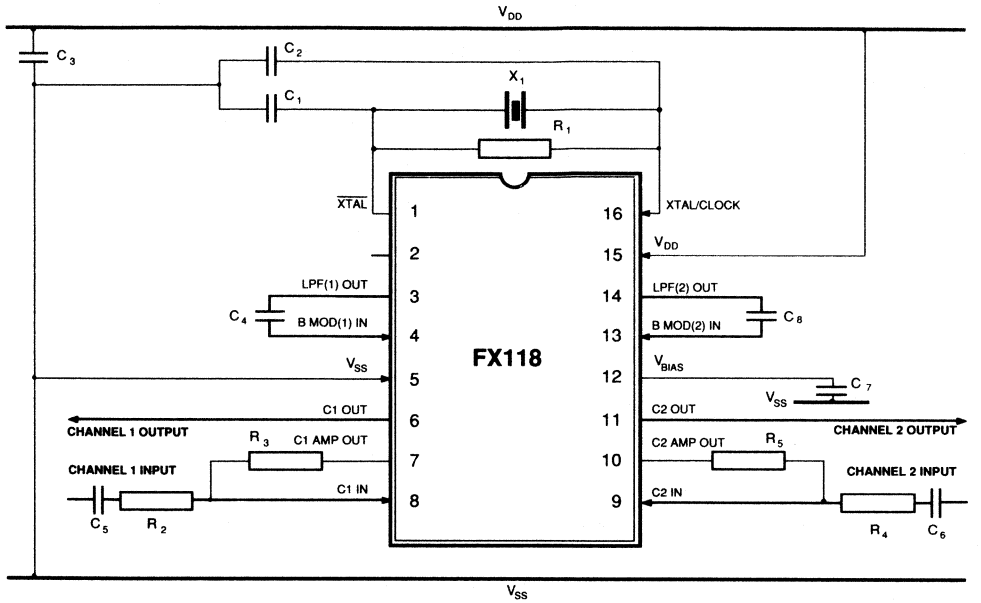
The on-chip modulation process has the properties of high baseband and carrier frequency rejection which when combined with high-order output filtering, produces a high-quality recovered voiceband audio.

The frequency stability of the FX118 is achieved by an on-chip oscillator employing an external 4.433619MHz Xtal or clock input to produce the common carrier frequency and the sampling clocks for the switched capacitor low and bandpass filters.

This microcircuit has a low power requirement of 3.0 volts (min.) and is encapsulated in either 16-pin DIL or small outline SMD (S.O.I.C.) plastic packages both of which are of a physical size suitable for either base or handset type telephone instruments as well as battery-portable and mobile communications systems.

| Pin Number<br>FX118DW<br>FX118P | Function |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** Output of clock oscillator inverter. |
| 2 | No Internal Connection: It is recommended that, to improve noise conditions, this pin is connected to $V_{SS}$. |
| 3 | **LPF(1) Out:** The output of the Channel 1 Lowpass Filter. It is to be coupled to "B Mod(1) In" via a 1.0µF capacitor – see Figure 2. |
| 4 | **B Mod(1) In:** The input to Channel 1 balanced modulator. Internally biased at $V_{DD}/2$ it is to be coupled to "LPF(1)" via a 1.0µF capacitor – see Figure 2. |
| 5 | **$V_{SS}$:** Negative supply (GND). |
| 6 | **C1 Out:** The analogue output of Channel 1. |
| 7 | **C1 Amp Output:** Channel 1 amplifier with external components (see Figure 2) can be used to provide gain in the signal path. |
| 8 | **C1 In:** The negative input of Channel 1 Amplifier. Recommended external components are shown in Figure 2. |
| 9 | **C2 In:** The negative input of Channel 2 Amplifier. Recommended external components are shown in Figure 2. |
| 10 | **C2 Amp Output:** Channel 2 amplifier with external components (see Figure 2) can be used to provide gain in the signal path. |
| 11 | **C2 Out:** The analogue output of Channel 2. |
| 12 | **$V_{BIAS}$:** The internal analogue bias line at $V_{DD}/2$. It should be decoupled to $V_{SS}$ via a 1.0µF or greater capacitor. See Figure 2. |
| 13 | **B Mod(2) In:** The input to Channel 2 balanced modulator. Internally biased at $V_{DD}/2$ it is to be coupled to "LPF(2)" via a 1.0µF capacitor – see Figure 2. |
| 14 | **LPF(2) Out:** The output of the Channel 2 Lowpass Filter. It is to be coupled to "B Mod(2) In" via a 1.0µF capacitor – see Figure 2. |
| 15 | **$V_{DD}$:** The positive supply rail. A single positive supply voltage (3.0v – 5.0v) is required. Levels and voltages within the Duplex Frequency Inverter are dependent upon this supply. |
| 16 | **Xtal/Clock:** 4.433619 MHz Xtal or externally derived clock is injected at this pin. See Figure 2. Operation of the FX118 without a Xtal or clock input may cause device damage. |

## Application Information




| Component | | Value | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $R_1$ | = | 1.0MΩ | $C_2$ | = | 33pF | $C_7$ | = | 1.0µF |
| $R_2 R_3 C_5$ | | See Note | $C_3$ | | 0.47µF | $C_8$ | | 1.0µF |
| $R_4 R_5 C_6$ | | See Note | $C_4$ | | 1.0µF | $X_1$ | | 4.33619MHz |
| $C_1$ | | 47pF | | | | | | |

***Tolerances*** $C = \pm 20\%$ $R = \pm 10\%$

**NOTES**
1. Configurations $R_2$, $R_3$, $C_5$ and $R_4$, $R_5$, $C_6$ should be chosen with respect to the specific application.
2. Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast-reaction fuse).

*Fig.2 Recommended External Components*

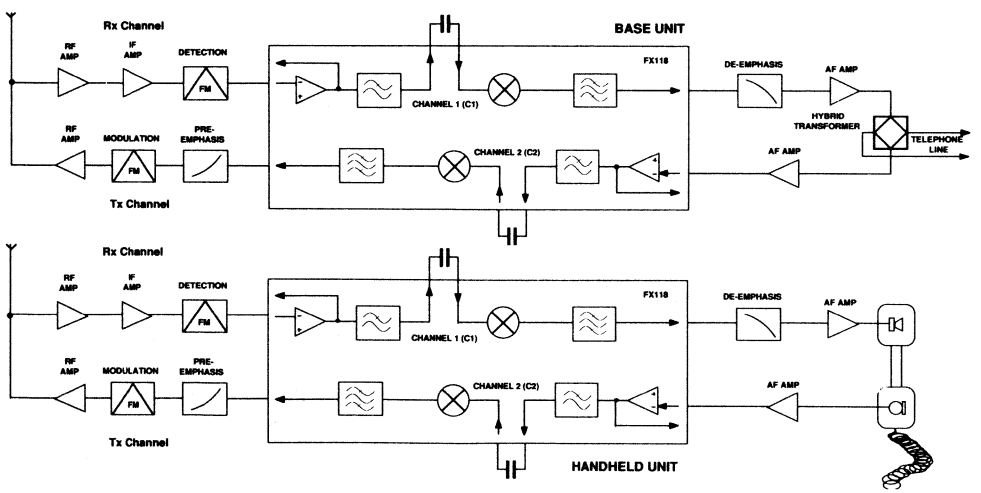



*Fig.3 Example of the FX118 Employed in a Cordless Telephone Application*

# Application Information .....

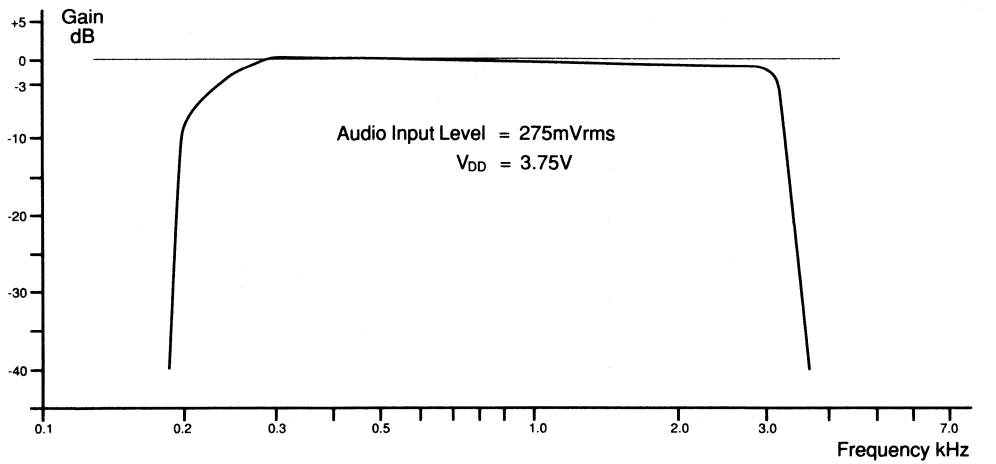



*Fig.4 Typical Audio Frequency Response of a Single Scrambled or De-scrambled Channel*

### System Gains

When calculating the external components for the operation of the FX118 the following points should be considered:

(a) The Input Lowpass Filter has a (typical) gain of 0.5dB.

(b) The Balanced Modulator has a (typical) attenuation of 4.0dB.

(c) The Output Bandpass Filter has a (typical) gain of 4.5dB.

---

## How the Inverter Works

Carrier Frequency *minus* Input Voice Frequency *equals* Scrambled Voice Frequency

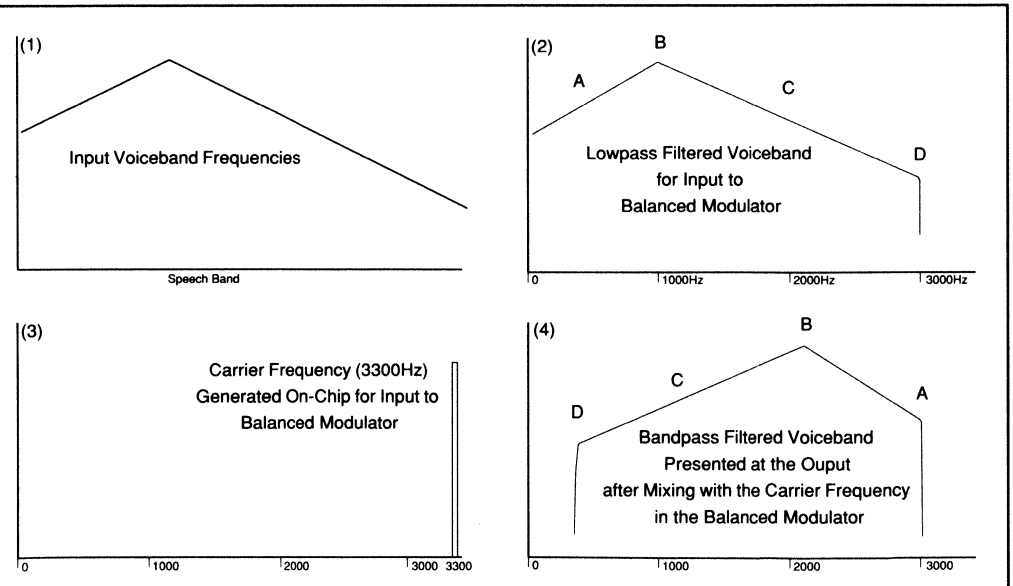



*Fig.5 A Pictorial Explanation of the FX118 "Scramble Operation"*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current | (supply pins) | +/- 30mA |
| | (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX118DW/P** | -40°C to +85°C |
| Storage temperature range: | **FX118DW/P** | -40°C to +85°C |

**Operating Limits**

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 3.75V. $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.433619MHz. Audio level 0dB ref: = 388mV rms @ 1.0kHz.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 3.0 | 3.75 | 5.5 | V |
| Supply Current | | – | 4.0 | 6.0 | mA |
| Input Impedance (Amplifiers) | | 1.0 | 10.0 | – | MΩ |
| Output Impedance (LP Filters) | | – | 2.0 | – | kΩ |
| Output Impedance (C1, C2 ) | | – | 200 | – | Ω |
| Output Impedance (C1, C2 Amps) | | – | 10.0 | – | kΩ |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | – | – | MΩ |
| $R_{OUT}$ | | – | 10.0 | – | kΩ |
| Inverter Gain | | – | 10.0 | – | V/V |
| Gain/Bandwidth Product | | – | 10.0 | – | MHz |
| **Dynamic Values** | | | | | |
| Analogue Signal Input Levels | | -16.0 | – | 4.0 | dB |
| SINAD | 6 | – | 30.0 | – | dB |
| Unwanted Modulation Products | 1, 2 | – | -40.0 | – | dB |
| Carrier Breakthrough | 1, 2 | – | -55.0 | – | dB |
| Baseband Breakthrough | 1, 2 | – | -40.0 | – | dB |
| Carrier Frequency | | – | 3299 | – | Hz |
| Analogue Output Noise | 3 | – | -42.0 | – | dB |
| Analogue Output Noise | 5 | – | -46.0 | – | dBp |
| **Filters** | | | | | |
| **Input Lowpass Filter** | 1 | | | | |
| Cut-Off Frequency (-3dB) | | – | 3100 | – | Hz |
| Passband Ripple (300Hz - 3kHz) | | – | ±1.0 | – | dB |
| Attenuation at 3.3kHz | | – | 30.0 | – | dB |
| Attenuation at 3.6kHz | | – | 45.0 | – | dB |
| Passband Gain | | – | 0.5 | – | dB |
| **Output Bandpass Filter** | 1, 4 | | | | |
| Passband Frequencies | | 300 | – | 3000 | Hz |
| Passband Ripple | | – | ±1.0 | – | dB |
| Low Freq. Roll-Off <200Hz | | 12.0 | – | – | dB/oct. |
| High Freq. – Attenuation at 3.4kHz | | – | 48.0 | – | dB |
| Passband Gain | | 3.5 | 4.5 | 5.5 | dB |
| **Overall Modulated and De-Modulated Channel Response** | | | | | |
| Passband Frequencies (Tx and Rx Channel) | | 300 | – | 3000 | Hz |
| Passband Ripple | | -3.0 | – | 2.0 | dB |
| Low Freq. Roll-Off <250Hz | | 18.0 | – | – | dB/oct. |
| High Freq. – Attenuation at 3.4kHz | | – | 48.0 | – | dB |
| Passband Gain | 4 | – | 0.5 | – | dB |
| Distortion | 1 | – | 3.0 | – | % |

**Notes:**

1. Measured with an audio input level of -3.0dB.
2. With respect to a single modulated (scrambling) channel.
3. Measured with a short circuit input, at any analogue output, in a 30.0kHz bandwidth.
4. With Input Amplifier gain at 0dB.
5. Measured psophometrically weighted, at any analogue output.
6. Measured in a 30kHz bandwidth.

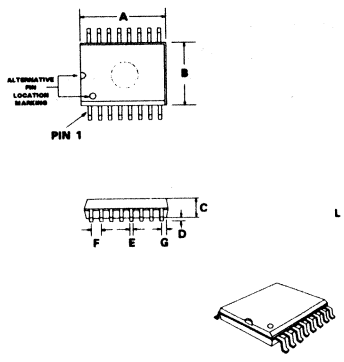
## Package Outline

The FX118DW, the Small Outline Integrated Circuit (S.O.I.C.) is shown in Figure 6 and the FX118P plastic dual-in-line package is shown in Figure 7.
Pin 1 identification marking is shown on the relevant diagram and pins on both package styles number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX118 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

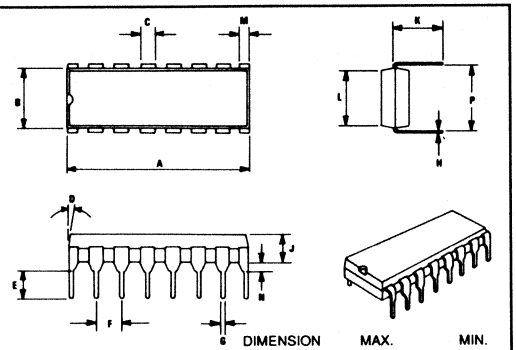
*Fig.6* ***FX118DW*** *16-pin S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.31 | | 10.03 | G | | 0.66 | |
| B | 7.59 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.7* ***FX118P*** *16-pin DIL Package*




| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.24 | 18.86 |
| B | 6.41 | 6.29 |
| C | 1.54 | 1.51 |
| D | 7°,30' | 6°,30' |
| E | 3.20 | 3.15 |
| F | 2.54 | TYPICAL |
| G | 0.46 | |
| H | 0.25 | |
| J | 3.33 | 3.27 |
| K | 5.77 | 5.65 |
| L | 5.90 | 5.78 |
| M | 1.00 | 0.98 |
| N | 1.78 | 0.51 |
| P | 9.40 | 8.38 |

NOTE: All dimensions in mm. Angles in degrees.

## Ordering Information

**FX118DW** 16-pin surface mount S.O.I.C.

**FX118P** 16-pin plastic DIL

# Integrated Circuits Data Book

Section 6

# Telecoms

# CML Semiconductor Products

PRODUCT INFORMATION

# FX611 Subscriber Private Metering (SPM) Detector

Publication D/611/6 February 1993
Provisional Issue

## Features/Applications

- Meets 12kHz and 16kHz SPM Specifications
- Tone Follower and SPM Packet Detection Modes
- Adjustable Input Gain
- Low-Power 5V CMOS Process
- PABX and Payphone Applications
- General Purpose Pulse Detection
- Surface Mount and DIL Package Styles
- Crystal Controlled

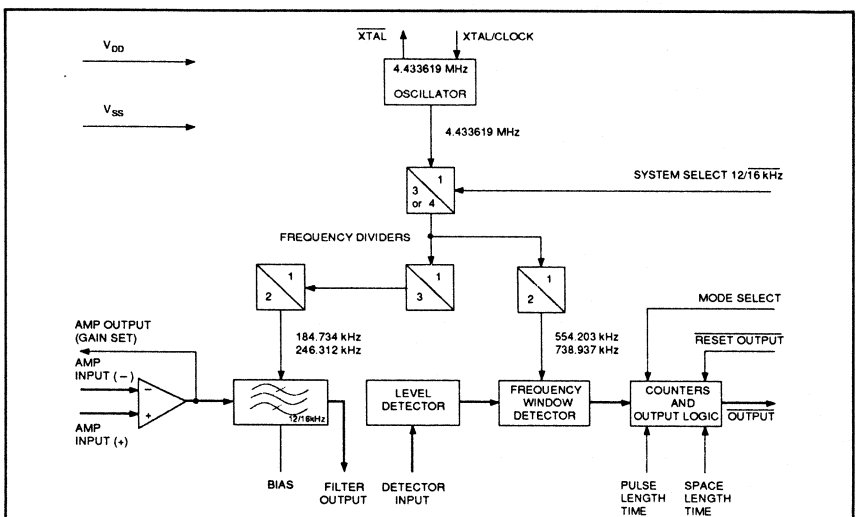



*Fig.1 Internal Block Diagram*

FX611

## Brief Description

The FX611 is a single-chip, low-power CMOS tone detector designed for use in both the PABX and general payphone applications for Subscriber Private Metering. The Decode and Not-Decode band edges are accurately defined by the use of an external 4.433619MHz crystal.
Operation to either of the 12kHz or 16kHz SPM systems is pin programmable, with system amplitude sensitivities and pulse period timing being provided by the use of external components.

The FX611 has 2 modes of operation :

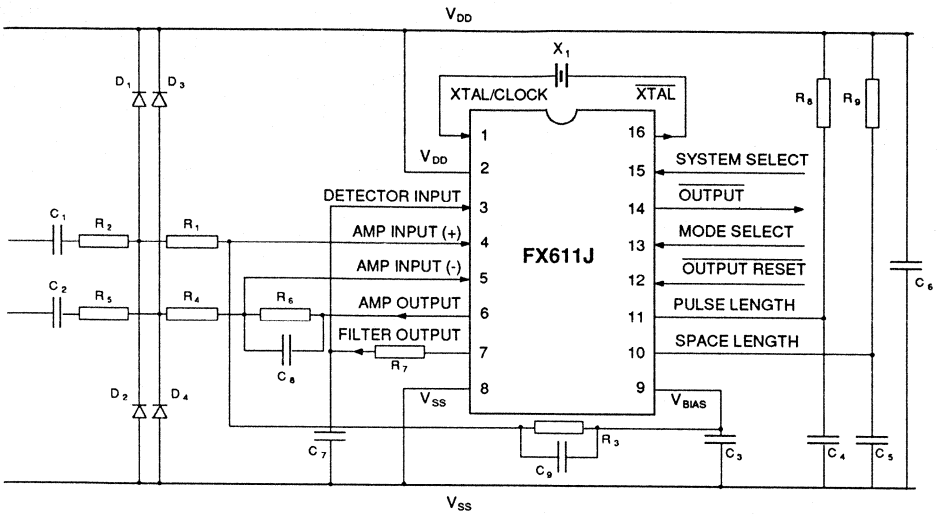
1) Tone Follower Mode.
2) SPM Packet Mode.

1) Tone Follower Mode.
   A logic '0' is output whenever a tone of the correct frequency and period is detected.
2) SPM Packet Mode.
   In this mode an output is obtained only when both the mark and space timing criteria of an SPM pulse have been fulfilled.

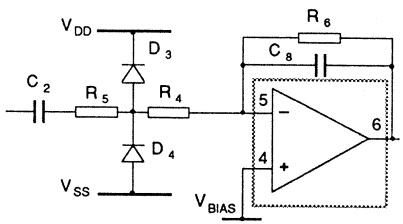
This device, which is available in DIL and SMT packages, requires only a single 5-volt power supply, a 4.433619MHz crystal and external gain and timing components to meet most SPM specifications.

| Pin Number | | Function |
|---|---|---|
| DIL FX611J | Quad FX611LG/LS | |
| 1 | 1 | **Xtal/Clock :** Input to the clock oscillator inverter. A single 4.33619MHz Xtal or external clock pulse is required at this input (see Figure 2). |
| 2 | 2 | $V_{DD}$ : The positive supply rail, a single +5-volt supply is required. |
| 3 | 5 | **Detector Input :** "Schmitt Trigger" level detector circuitry, whose input thresholds are set internally. This input must be connected to the Filter Output pin using the external integration components $R_7$ and $C_7$, as shown in Figure 2. |
| 4 | 6 | **Amplifier Input (+) :** The positive and negative amplifier inputs. With single or differential inputs the amplifier and its external circuitry are used to provide the gain required to set the device to the user's National Level Specification. The external diodes are used at both inputs (if in use) to provide protection when the line input level exceeds the supply rails (ie above the Absolute Maximum Rating), see Figures 2 and 3. |
| 5 | 7 | **Amplifier Input (–) :** |
| 6 | 8 | **Amplifier Output :** The output of the input stage amplifier and is used with gain setting components as described above (see Figures 2 and 3). |
| 7 | 11 | **Filter Output :** The switched (12kHz/16kHz) bandpass filter output. This output must be connected to the Detector Input pin using the external integration components $R_7$ and $C_7$, as shown in Figure 2. |
| 8 | 12 | $V_{SS}$ : The negative supply rail, (GND). |
| 9 | 13 | $V_{BIAS}$ : The analogue bias point, requires to be externally decoupled to $V_{SS}$ via capacitor $C_3$. |
| 10 | 14 | **Space Length Time :** Active only in the 'SPM Packet' mode, this input, using an external RC network, sets the minimum valid No-Tone (Space) period for the incoming packet. The minimum valid No-Tone length is set using the formula : $t_S = 0.7\ (R_9 \times C_5)$. If the 'SPM Packet' mode is not required, these timing components may be omitted. See Figure 2. |
| 11 | 17 | **Pulse Length Time :** Active only in the 'SPM Packet' mode, this input, using an external RC network, sets the minimum valid Tone period for the incoming packet. The minimum valid Tone length is set using the formula : $t_M = 0.7\ (R_8 \times C_4)$. If the 'SPM Packet' mode is not required, these timing components may be omitted. See Figure 2. |
| 12 | 18 | $\overline{\text{Output Reset}}$ : This input is used only in the 'SPM Packet' mode. Once an SPM Packet has been detected and an output generated (logic "0") from this device the output remains set until this input is set to a logic "0" (note the minimum reset period $t_{RESET}$, shown on Figure 4). This input has an internal 1MΩ pullup resistor. |
| 13 | 19 | **Mode Select :** A control pin to select either the 'Tone Follower' mode or the 'SPM Packet' mode. A logic "1 " selects 'Tone Follower', a logic "0" selects 'SPM Packet'. This input has an internal 1MΩ pullup resistor (Tone Follower). |
| 14 | 20 | $\overline{\text{Output}}$ : The digital output of the SPM Detector. In the 'Tone Follower' mode, a valid Tone gives a logic "0" and No-Tone gives a logic "1." Tonebursts and tone dropouts of less than 16 cycles are ignored. In the 'SPM Packet' mode, the output is set to a logic "0" when a valid 'packet' is measured. The output remains so until reset by a logic "0" at the Output Reset function, see Figure 4. |
| 15 | 23 | **System Select :** A control pin to set the device to work on either a 12kHz (logic "1") or 16kHz (logic "0") SPM system. This input has an internal 1MΩ pullup resistor (12kHz ). |
| 16 | 24 | $\overline{\text{Xtal}}$ : The output of the clock oscillator inverter, see Figure 2. |
| | 3, 4, 9, 10, 15, 16, 21, 22. | No internal connection. Leave open circuit. |

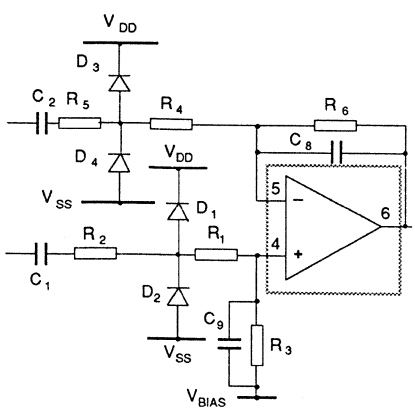
## External Components




| Component | Reference | Component | Reference |
|---|---|---|---|
| $R_1$ | Figure 3 | $C_1$ | Figure 3 |
| $R_2$ | Figure 3 | $C_2$ | Figure 3 |
| $R_3$ | Figure 3 | $C_3$ | 1.0µF ± 20% |
| $R_4$ | Figure 3 | $C_4$ | Note 1 |
| $R_5$ | Figure 3 | $C_5$ | Note 1 |
| $R_6$ | Figure 3 | $C_6$ | 1.0µF ± 20% |
| $R_7$ | 47kΩ ± 1% | $C_7$ | 100pF ± 1% |
| $R_8$ | Note 1 | $C_8$ | Note 5 |
| $R_9$ | Note 1 | $C_9$ | Note 5 |
| $D_1$ to $D_4$ | 1N4148 or equivalent | $X_1$ | 4.433619MHz |




*(a) Single Input*




*(b) Differential Input*

*Fig.2 External Component Connections*

### Notes

**1.** Component values ($R_8$, $C_4$), set the minimum tone 'Mark' period and ($R_9$, $C_5$), set the minimum 'Space' period in the SPM Packet mode and are calculated as :-

$t_M = 0.7\ (R_8 \times C_4)$. $t_S = 0.7\ (R_9 \times C_5)$.

*– Mark and Space calculations should be made taking into consideration response times – $t_R$ and $t_D$ (Figure 4). Current consumption will increase if low values of timing resistor are used. –*

**2.** Input Amplifier gain components (Figure 2 (a & b) – these components set the gain required (Figure 3) to achieve the various National Level Specifications.

**3.** Protection diodes – as most telephone systems operate at voltages in excess of the Absolute Maximum Limits for damage, diodes $D_1 - D_4$ are essential for device protection.

**4.** Example component values for the West German 'FTZ' Specification (16kHz) :–

**"Will Decode" Sensitivity (Min.)** **-21dB**

**"Will Not Decode" Sensitivity** **-27dB**

Calculated gain range: 0 to 3dB. Selected gain: 1.4dB.

$R_1$– 47kΩ , $R_2$ – 47kΩ, $R_3$–130kΩ, $R_4$ – 47kΩ, $R_5$– 47kΩ, $R_6$– 130kΩ.
$C_1$– 330pf, $C_2$– 330pf, $C_8$– 39pf, $C_9$– 39pf.

Tolerances : Resistors = 1%. Capacitors = 10%.

**5.** $C_8$, $C_9$, are anti-aliasing components and should be set for a cut-off frequency of approximately 32kHz.

## Amplitude and Timing

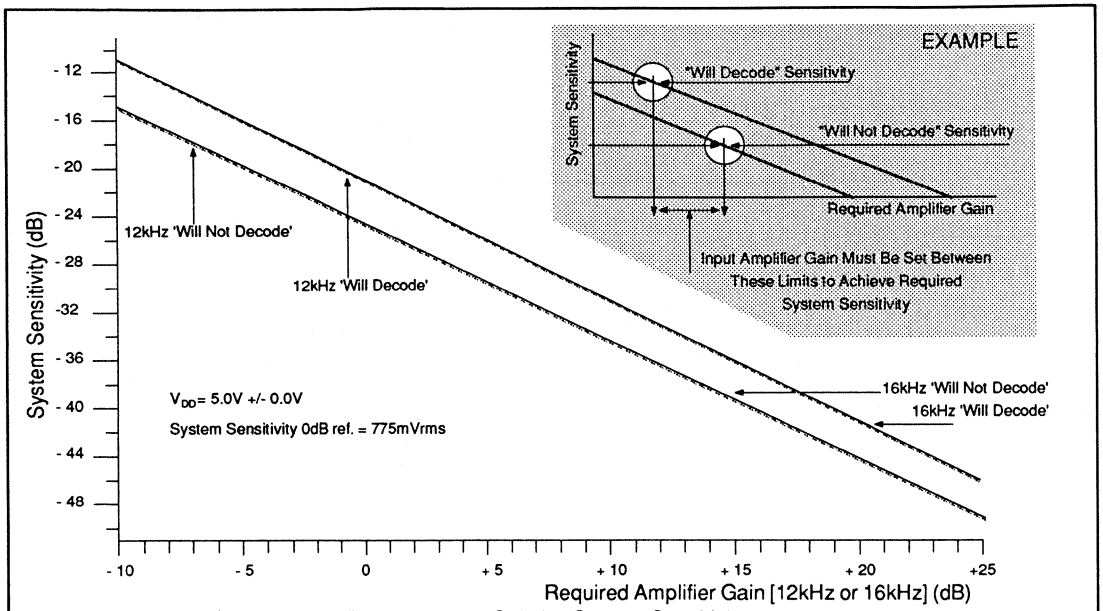



*Fig.3 Graph for the Calculation of Required Input Gain Vs System Sensitivity*

### Input Gain Calculation

Apply the system 'Will' and 'Will-Not' Decode sensitivity values ('Y' axis) to the relevant graph in Figure 3. The 'X' axis indicates the input gain area required.

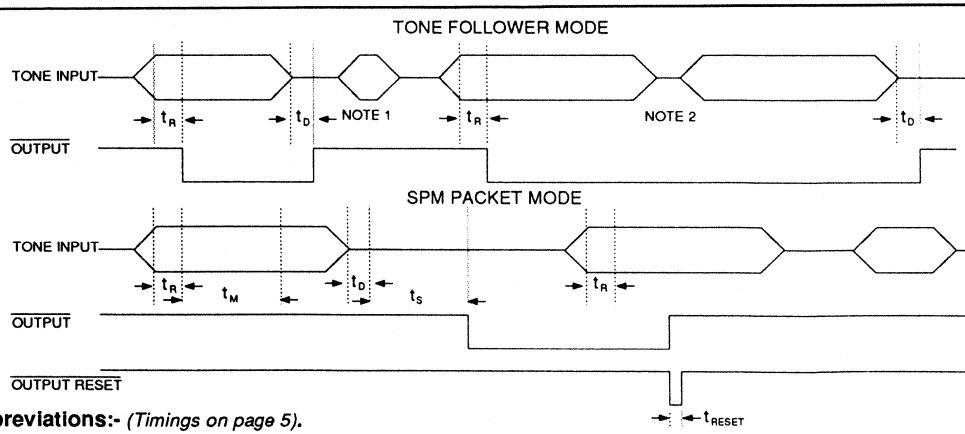
Gain is calculated as :–

$$\frac{Z_{feedback}}{Z_{input}} = \frac{R_6 \,//\, X(C_8)}{R_4 + R_5 + X(C_2)}$$

and

$R_3 = R_6$
$R_1 = R_4$
$R_2 = R_5$ — if the differential amplifier is used.
$C_9 = C_8$
$C_1 = C_2$

Input resistor, $R_{protect}$ ($R_1$ or $R_4$ ) is intended to prevent the amplifier input pins going beyond the supply rail voltages, therefore when calculating the input gain the value of $R_{protect}$ must be greater or equal to 0.15 $R_{feedback}$ ($R_3$ or $R_6$ ).
It is recommended that the input time constant is set as a highpass value between audio and the SPM tone frequencies, with $C_1$ or $C_2$ being calculated with input resistors to achieve both time and gain requirements.




**Abbreviations:-** *(Timings on page 5).*

$t_R$ – Tone Response Time
$t_D$ – Tone De–response Time
$t_M$ – Pulse Length Time
$t_S$ – Space Length Time
$t_{RESET}$ – SPM Output Reset Time

*Note 1 – No reaction to pulses with periods less than 'Tone Response Time'.*
*Note 2 – No reaction to drop-outs with periods of less than 'Tone De-response Time'.*

*Fig.4 Timing Information*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply Voltage | | -0.3 to 7.0V |
| Input Voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | ± 30mA |
| (other pins) | | ± 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX611J** | -30°C to + 85°C (ceramic) |
| | **FX611LG/LS** | -30°C to + 70°C (plastic) |
| Storage temperature range: | **FX611J** | -55°C to +125°C (ceramic) |
| | **FX611LG/LS** | -40°C to + 85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified :- $V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C, Xtal/Clock $f_0$ = 4.433619MHz, Audio level 0dB ref: = 775mV rms.

Signal to Noise Ratio ≥18dB.

| Characteristics | System | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Values** | | | | | | |
| Supply Voltage ($V_{DD}$) | | | 4.5 | 5.0 | 5.5 | V |
| Supply Current ($I_{DD}$) | | | – | 3.0 | – | mA |
| Analogue Input Impedance (at pins) | | | 1.0 | – | – | MΩ |
| Digital Input Impedance | | | – | 1.0 | – | MΩ |
| Digital Output Impedance | | | – | – | 10.0 | kΩ |
| **Dynamic Values** | | | | | | |
| Sensitivity | 12kHz | 7 | – | -24.0 | – | dB |
| Sensitivity | 16kHz | 7 | – | -25.5 | – | dB |
| Signal to Noise Ratio | | 4 | 18.0 | – | – | dB |
| Detector Threshold (Upper) | | 8 | 2.95 | 3.0 | 3.05 | V |
| Detector Threshold (Lower) | | 8 | 1.95 | 2.0 | 2.05 | V |
| **Bandpass Filter** | | | | | | |
| Passband Gain | 12kHz | | – | 16.5 | – | dB |
| Passband Gain | 16kHz | | – | 16.5 | – | dB |
| Passband Ripple | 12kHz | 6 | – | – | 1.0 | dB |
| Passband Ripple | 16kHz | 6 | – | – | 1.0 | dB |
| Audio Band Attenuation (< 3.4kHz) | 12kHz | | – | 40.0 | – | dB |
| | 16kHz | | – | 50.0 | – | dB |
| **Frequency Discrimination** | | | | | | |
| 'Will Decode' Frequency Limits | 12kHz | | 11.82 | – | 12.18 | kHz |
| | 16kHz | | 15.76 | – | 16.24 | kHz |
| 'Will-Not Decode' Frequency | | | | | | |
| Upper Limits | 12kHz | | 12.48 | – | 50.0 | kHz |
| | 16kHz | | 16.64 | – | 50.0 | kHz |
| Lower Limits | 12kHz | | 0 | – | 11.52 | kHz |
| | 16kHz | | 0 | – | 15.36 | kHz |
| **Timing Information** | | | | | | |
| Valid Toneburst Length ($t_M$) | 12kHz/16kHz | 1,2 | 16.0 | – | – | cycles |
| Valid 'Space' Length ($t_S$) | 12kHz/16kHz | 2 | 5.0 | – | – | ms |
| Tone Response Time ($t_R$) | 12kHz | 1,3,4 | 1.7 | – | 3.0 | ms |
| | 16kHz | 1,3,4 | 1.2 | – | 2.0 | ms |
| De-response Time ($t_D$) | 12kHz | 4,5,9 | 1.7 | – | 30.0 | ms |
| | 16kHz | 4,5,9 | 1.2 | – | 20.0 | ms |
| SPM Output Reset Time ($t_{RESET}$) | 12kHz/16kHz | 2 | 150.0 | – | – | ns |

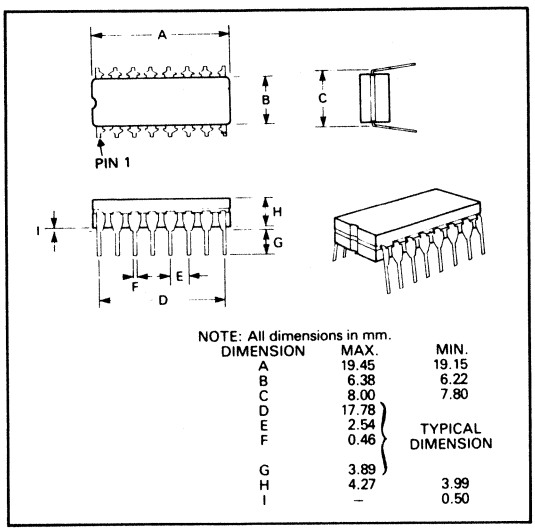
**Notes:**

1. Tone Follower mode.
2. SPM Packet mode – in this mode the minimum valid Pulse (Space) length is programmable by means of an RC network on the Pulse (Space) Length Time pin. If no RC network is used, the minimum valid tone length reverts to16 cycles.
3. The time for the circuit to recognise a valid 'Tone' in the Tone Follower mode.
4. With the noise level at the input < -11.0dB (100kHz noise bandwidth).
5. The time for the circuitry to recognize a valid 'no tone' in the tone follower mode.
6. Over the 'Will Decode' bandwidth of the frequency discriminator.
7. With the input gains set to unity. Input gain requirements are calculated with reference to Figure 3.
8. These thresholds are measured at 5-volt $V_{DD}$, any supply variation will alter thresholds accordingly.
9. As the Noise or Gain is increased the de-response time increases.

## Package Outline

The FX611J, the cerdip package, is shown in Figure 5. The 'LG' version is shown in Figure 6, and the 'LS' version in Figure 7.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4.
Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 5* **FX611J** *16-pin DIL Package*



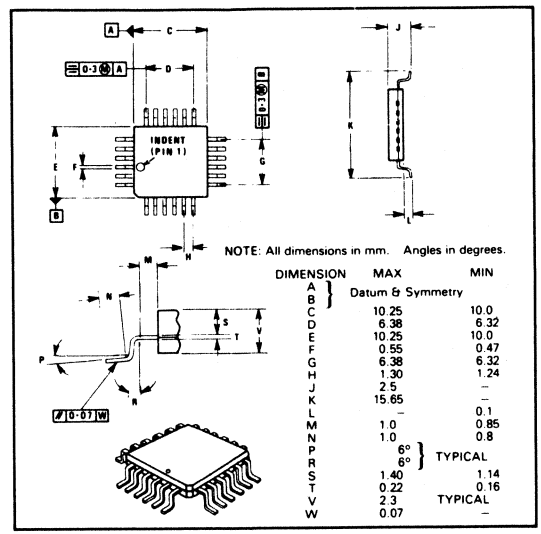

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.45 | 19.15 |
| B | 6.38 | 6.22 |
| C | 8.00 | 7.80 |
| D | 17.78 | TYPICAL DIMENSION |
| E | 2.54 | |
| F | 0.46 | |
| G | 3.89 | |
| H | 4.27 | 3.99 |
| I | – | 0.50 |

## Handling Precautions

The FX611 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

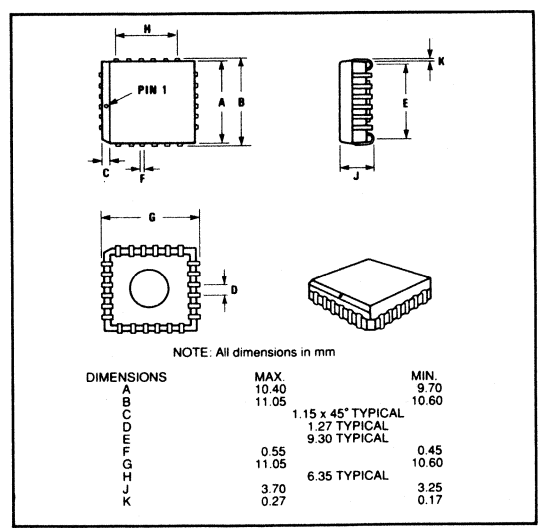
*Fig. 6* **FX611LG** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | Datum & Symmetry | |
| B | | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig. 7* **FX611LS** *24-lead Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

## Ordering Information

| | |
|---|---|
| **FX611J** | **16-pin cerdip DIL** |
| **FX611LG** | **24-pin quad plastic encapsulated bent and cropped** |
| **FX611LS** | **24-lead plastic leaded chip carrier** |

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX613 Universal Call Progress Decoder

Publication D/613/1 September 1992
Advance Information

## Features

- **Covers Worldwide Call Progress Frequencies (300Hz to 2,150Hz)**
- **3 Volt <1mA Requirement**
- **Decodes Single or Modulated Tones**
- **Analogue In/Serial Data Out**
- **Speech Discrimination Ability**
- **µProcessor Compatible Outputs**
- **Telephone/Telecoms, Radio and Fax/Modem Applications**
- **Mixed Analogue/Digital Technology**

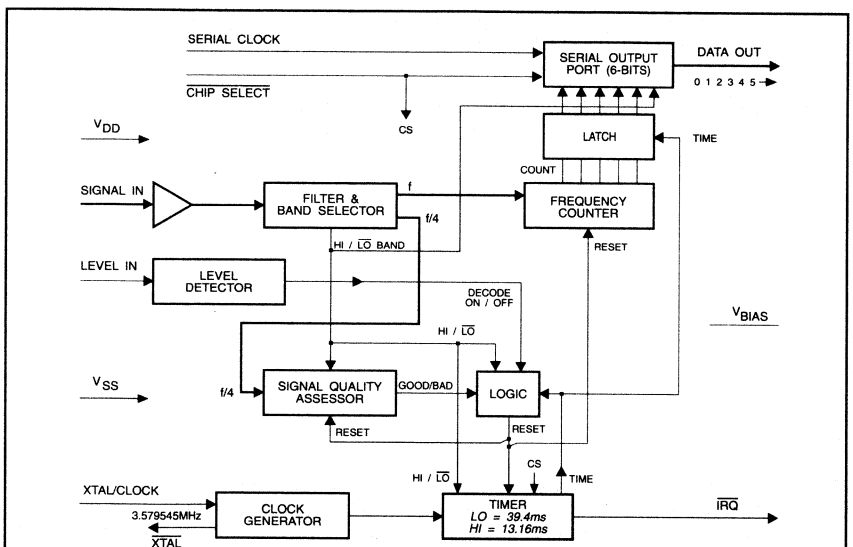



*Fig.1 Functional Block Diagram*

FX613

## Brief Description

The FX613 is a wide-band, 'N-Tone', non-predictive tone decoder to measure telephone system call progress tones in PABX, Pay/Feature-Phone, Fax and Modem systems.

Adhering to Must/Must-Not Decode limits and able to measure inband frequencies in outband modulation, this decoder measures the frequency of input signals in the range 300Hz to 2,150Hz; the result of each measurement is presented to a system µProcessor, as a 6-bit serial word.

The decode frequency range, which covers the World's call progress application spectrum, is processed internally as two bands: LO = 300Hz to 660Hz and HI = 900Hz to 2150Hz. Frequency measurement is achieved by counting the number of cycles in a set time period (LO = 39.47ms or HI = 13.16ms). Bad signal/level quality or NOTONE results in a count-abort, timing-reset and no output from the decoder.

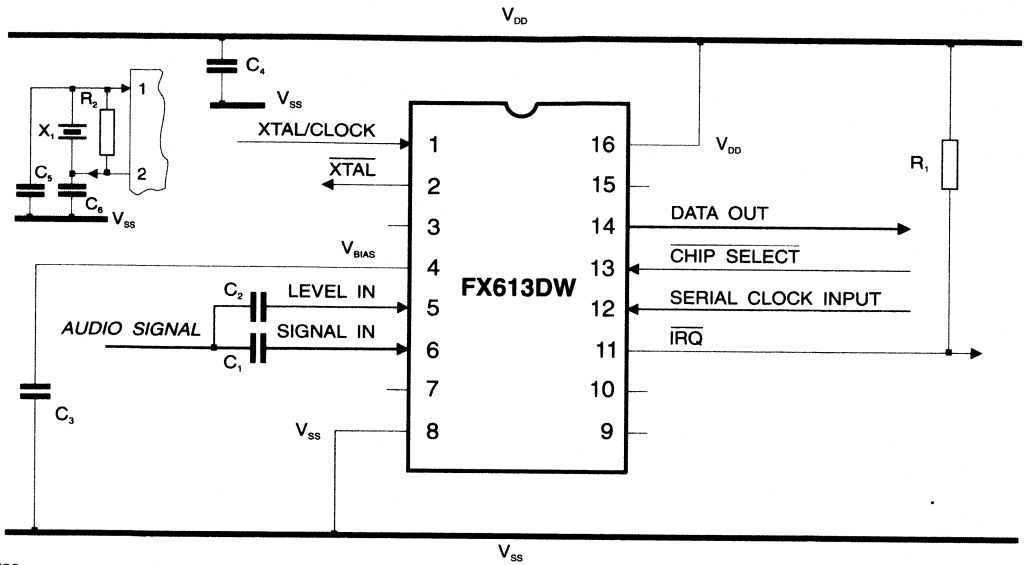
Current frequency information is output for the µProcessor using a Serial Data, Clock and Interrupt interface.

Data from the FX613 should be processed by a µProcessor whose algorithms are able to recognize the frequency, sequence and/or cadence of input signals as national call progress information; e.g.: 'Dial', 'Busy', 'Number-Unobtainable', 'Ringing' and automatic tones employed by Fax, Modem systems. Software can be simply configured to reject speech frequencies.
Due to its 'N-Tone', non-predictive decoding capability, units employing the FX613 can be redeployed under a new national standard by a simple software amendment.

Available in 16-pin plastic S.O.I.C. SMD and 14-pin plastic DIL packages, this low-cost, mixed analogue/digital microcircuit has a typical power requirement of less than 1mA at 3 volts and utilizes a telecom-system clock input of 3.579545MHz to maintain frequency accuracy.

| Pin Number | | Function |
|---|---|---|
| FX613DW | FX613P | |
| 1 | 1 | **Xtal/Clock**: The input to the on-chip clock oscillator inverter. A 3.579545MHz Xtal or externally derived telephone system clock ($f_{XTAL}$) should be connected here.<br>Note - The operation of the FX613 without a suitable Xtal/Clock input may cause device damage. |
| 2 | 2 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter. See Figure 2. |
| 3 | 3 | No internal connection. |
| 4 | 4 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$. |
| 5 | 5 | **Level In:** The input for level discrimination. This input is internally biased to $V_{BIAS}$, signals must be a.c. coupled. The audio signal must be fed to both this pin and the Signal In pin. Correct level detection determines the operation of this device (see Principles of Decoder Operation), however to disregard the amplitude of the input levels the FX613 may be permanently enabled by pulling this pin to $V_{DD}$ and disabled by pulling to $V_{SS}$. |
| 6 | 6 | **Signal In:** The input for frequency discrimination and decoding. This input is internally biased to $V_{BIAS}$, signals must be a.c. coupled. The audio signal must be fed to both this pin and the Level In pin. |
| 7 | | No internal connection. |
| 8 | 7 | **$V_{SS}$:** Negative supply rail. Signal ground. |
| 9 | 8 | No internal connection. |
| 10 | | No internal connection. |
| 11 | 9 | **$\overline{\text{IRQ}}$:** This Interrupt Request output from the FX613 is 'wire-OR able' allowing the interrupt outputs of other peripherals to be combined and connected to the Interrupt input of a µProcessor. This input has a low-impedance pulldown to $V_{SS}$ when active and a high-impedance when inactive. An interrupt is produced on completion of a HI or LO frequency measurement. |
| 12 | 10 | **Serial Clock:** The serial clock from the µProcessor. Data Out is clocked into the µProcessor on the rising edge of the Serial Clock. See Data-Read Timing diagram. |
| 13 | 11 | **$\overline{\text{Chip Select}}$:** A logic "0" at this input will select this device. |
| 14 | 12 | **Data Out:** The serial data output. Under the control of the Chip Select and Serial Clock inputs, data should be read from this output in 6-bit blocks MSB (Bit-5) first.<br>If 8 serial clock pulses are applied, two additional logic "0s" will be output after Bit-0. |
| 15 | 13 | No internal connection. |
| 16 | 14 | **$V_{DD}$:** Positive supply rail. A single, stable supply is required. Levels and voltages within the FX613 are dependent upon this supply. This pin should be decoupled to $V_{SS}$ by a capacitor located close to the FX613 pins. |

## Application Information




**Notes**

(1) The Xtal/Clock input may be driven from the host telephone system's 3.579545MHz clock; if a Xtal drive is required, the configuration shown INSET is recommended.

(2) The audio signal should be input to both Signal In and Level In pins via separate coupling capacitors. If it is wished to operate the device with disregard to on-chip level thresholds and permanently enable the FX613, the Level In pin should be held at $V_{DD}$. To disable the FX613 the Level In pin should be held at $V_{SS}$. Level thresholds are preset internally.

| Component | Value |
|---|---|
| $R_1$ | 22.0kΩ |
| $R_2$ | 1.0MΩ |
| $C_1$ | 0.01µF |
| $C_2$ | 0.1µF |
| $C_3$ | 1.0µF |
| $C_4$ | 1.0µF |
| $C_5$ | 33.0pF |
| $C_6$ | 33.0pF |
| $X_1$ | 3.579545MHz |

Tolerances: C = ± 20% R = ± 10%

*Fig.2 External Component Connections*

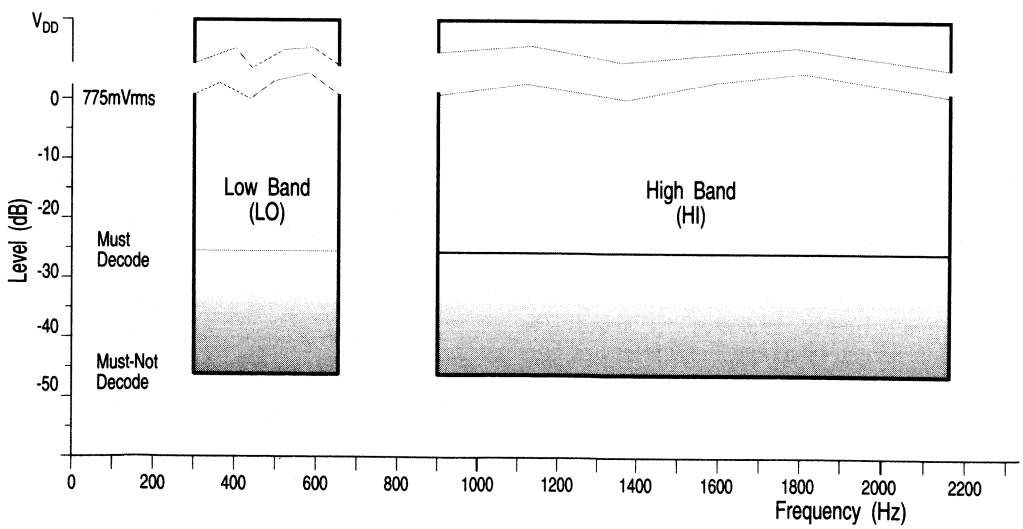



*Fig.3 HI/LO Decode Bands*

# Application Information .....

## Principles of Decoder Operation

### Level Detection

As level and frequency discrimination operations take place in parallel the audio signal should, under normal circumstances, be input to both Signal In and Level In pins via coupling capacitors.

If the input signal level (Level In) is outside the preset 'Must/Must Not Decode' thresholds (Specification Page), the Universal Call Progress Decoder will be disabled.

If it is wished to disregard signal input *levels* at the Level In pin and attempt to decode under all conditions, the decoder may be permanently enabled by holding the Level In pin at $V_{DD}$.
The device can disabled by pulling Level In to $V_{SS}$.

### NOTONE Recognition

The NOTONE condition can be recognized using µProcessor software timing as below.

a. Set the µP timer period to a period greater than the relevant frequency-band measurement period (13.16ms or 39.47ms).

b. Each 'Tone Measurement Complete' interrupt from the FX613 must reset the µP timer.

c. With NOTONE or white noise at the decoder input, the FX613 on-chip timer will be continually reset.

ii No 'Tone Measurement Complete' interrupt will occur - the µP timer will run.

ii The µP Timer time-out can be considered as a **NOTONE** indication.

| Level In | Timer | IRQ | Data Out |
|---|---|---|---|
| In Limits | Running | Enabled | Enabled |
| Out of Limits | Reset | Disabled | Disabled (frozen to previous bit-5 level |
| $V_{DD}$ | Running/Reset | Enabled/Disabled | Enabled (dependent upon Quality measurement) |
| $V_{SS}$ | Reset | Disabled | Disabled (frozen to previous bit-5 level) |

### Frequency Band Discrimination

The input signal is amplified by a self-biased (zero-crossing) inverting amplifier and then 'filtered' to remove high-frequency noise and jitter.

High (HI) and Low (LO) counters are employed to determine the input frequency band (HI = 900Hz to 2150Hz, LO = 300Hz to 660Hz).

If the input frequency is in the LO Band, the device will operate as a LO Band decoder and will remain so until a HI frequency signal is detected. If the input frequency is in the HI Band, the device will operate as a HI Band decoder and will remain so until a LO frequency signal is detected.

Frequency band monitoring is continuous with the band selection taking place every 9.8ms. It will therefore take 9.8ms from Power-Up to set up the initial correct decode frequency band.

### On-Chip Timer Operation

For frequency measurement, the FX613 counts the number of input cycles in a fixed time period. This fixed period, measured by the continuous on-chip timer, is set to 13.16ms for HI Band inputs and 39.47ms for LO Band inputs.

### On-Chip Timer Operation .....

When the timer expires the following actions take place:

a. A HI or LO ("1" or "0") band indication bit is latched into Bit-5 of the Serial Output Port.

b. The Frequency Counter count of 5-bits is latched into the Serial Output Port (Bit-4 [MSB] to Bit-0). The Serial Output Port Contains 6-bits, if 8 Serial Clock edges are employed, two extra "0s", which should be ignored, will be output last.

c. An interrupt is generated ($\overline{IRQ}$) to the µProcessor. The contents of the Serial Output Port should be read before the next interrupt is expected; if not data will be overwritten.

When the Chip Select input is set to "0" the interrupt is reset.

The On-Chip Timer and Frequency Counter will be reset in mid-count, and therefore unable to allow a valid measurement, under the following conditions:

a. A change of decode frequency band.

b. Decoder disabled; signal input level out of specification or Level Detect input set to $V_{SS}$.

c. Signal Quality Assessment considered 'Bad'.

d. Input signal frequency outside limits.

## Application Information .....

N = int (Frequency x Measurement Period)

Measurement Period = 39.47ms for Low Band (300Hz to 660Hz)
= 13.16ms for High Band (900Hz to 2150Hz)

Note: For input frequencies of between 661Hz and 899Hz the FX613 will give no reliable output.

| Bit 5 Output First | Band Bit (5) | MSB (4) | (3) | (2) | (1) | LSB (0) | Bits 0 to 4 = N |
|---|---|---|---|---|---|---|---|
| | HI-"1"/LO-"0" | Bits 0 to 4 represent the measured frequency in the selected band | | | | | |

When a 'correct' decode has been allowed and an interrupt generated, a 6-bit data word will be presented at the Serial Output Port. This 6-bit word indicates the input frequency's band and value as described above.

As an example, the following binary-word presented at the Serial Output Port **(1 1 0 1 1 0)** will indicate a frequency in the **HI Band** of between **1680Hz** and **1740Hz (Bit-5 = "1" = HI, 'N' = 22)**.

| LO Band | HI Band | N | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ |
|---|---|---|---|---|---|---|---|---|
| *280* | *840* | 11 | H/L | 0 | 1 | 0 | 1 | 1 |
| *285* | *855* | 11 | | | | | | |
| *290* | *870* | 11 | | | | | | |
| *295* | 885 | 11 | | | | | | |
| 300 | 900 | 11 | | | | | | |
| 305 | 915 | 12 | H/L | 0 | 1 | 1 | 0 | 0 |
| 310 | 930 | 12 | | | | | | |
| 315 | 945 | 12 | | | | | | |
| 320 | 960 | 12 | | | | | | |
| 325 | 975 | 12 | | | | | | |
| 330 | 990 | 13 | H/L | 0 | 1 | 1 | 0 | 1 |
| 335 | 1005 | 13 | | | | | | |
| 340 | 1020 | 13 | | | | | | |
| 345 | 1035 | 13 | | | | | | |
| 350 | 1050 | 13 | | | | | | |
| 355 | 1065 | 14 | H/L | 0 | 1 | 1 | 1 | 0 |
| 360 | 1080 | 14 | | | | | | |
| 365 | 1095 | 14 | | | | | | |
| 370 | 1110 | 14 | | | | | | |
| 375 | 1125 | 14 | | | | | | |
| 380 | 1140 | 14 | | | | | | |
| 385 | 1155 | 15 | H/L | 0 | 1 | 1 | 1 | 1 |
| 390 | 1170 | 15 | | | | | | |
| 395 | 1185 | 15 | | | | | | |
| 400 | 1200 | 15 | | | | | | |
| 405 | 1215 | 15 | | | | | | |
| 410 | 1230 | 16 | H/L | 1 | 0 | 0 | 0 | 0 |
| 415 | 1245 | 16 | | | | | | |
| 420 | 1260 | 16 | | | | | | |
| 425 | 1275 | 16 | | | | | | |
| 430 | 1290 | 16 | | | | | | |
| 435 | 1305 | 17 | H/L | 1 | 0 | 0 | 0 | 1 |
| 440 | 1320 | 17 | | | | | | |
| 445 | 1335 | 17 | | | | | | |
| 450 | 1350 | 17 | | | | | | |
| 455 | 1365 | 17 | | | | | | |
| 460 | 1380 | 18 | H/L | 1 | 0 | 0 | 1 | 0 |
| 465 | 1395 | 18 | | | | | | |
| 470 | 1410 | 18 | | | | | | |
| 475 | 1425 | 18 | | | | | | |
| 480 | 1440 | 18 | | | | | | |
| 485 | 1455 | 19 | H/L | 1 | 0 | 0 | 1 | 1 |
| 490 | 1470 | 19 | | | | | | |
| 495 | 1485 | 19 | | | | | | |
| 500 | 1500 | 19 | | | | | | |

| LO Band | HI Band | N | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ |
|---|---|---|---|---|---|---|---|---|
| 505 | 1515 | 19 | H/L | 1 | 0 | 0 | 1 | 1 |
| 510 | 1530 | 20 | H/L | 1 | 0 | 1 | 0 | 0 |
| 515 | 1545 | 20 | | | | | | |
| 520 | 1560 | 20 | | | | | | |
| 525 | 1575 | 20 | | | | | | |
| 530 | 1590 | 20 | | | | | | |
| 535 | 1605 | 21 | H/L | 1 | 0 | 1 | 0 | 1 |
| 540 | 1620 | 21 | | | | | | |
| 545 | 1635 | 21 | | | | | | |
| 550 | 1650 | 21 | | | | | | |
| 555 | 1665 | 21 | | | | | | |
| 560 | 1680 | 22 | H/L | 1 | 0 | 1 | 1 | 0 |
| 565 | 1695 | 22 | | | | | | |
| 570 | 1710 | 22 | | | | | | |
| 575 | 1725 | 22 | | | | | | |
| 580 | 1740 | 22 | | | | | | |
| 585 | 1755 | 23 | H/L | 1 | 0 | 1 | 1 | 1 |
| 590 | 1770 | 23 | | | | | | |
| 595 | 1785 | 23 | | | | | | |
| 600 | 1800 | 23 | | | | | | |
| 605 | 1815 | 23 | | | | | | |
| 610 | 1830 | 24 | H/L | 1 | 1 | 0 | 0 | 0 |
| 615 | 1845 | 24 | | | | | | |
| 620 | 1860 | 24 | | | | | | |
| 625 | 1875 | 24 | | | | | | |
| 630 | 1890 | 24 | | | | | | |
| 635 | 1905 | 25 | H/L | 1 | 1 | 0 | 0 | 1 |
| 640 | 1920 | 25 | | | | | | |
| 645 | 1935 | 25 | | | | | | |
| 650 | 1950 | 25 | | | | | | |
| 655 | 1965 | 25 | | | | | | |
| 660 | 1980 | 26 | H/L | 1 | 1 | 0 | 1 | 0 |
| *665* | 1995 | 26 | | | | | | |
| *670* | 2010 | 26 | | | | | | |
| *675* | 2025 | 26 | | | | | | |
| *680* | 2040 | 26 | | | | | | |
| *685* | 2055 | 27 | H/L | 1 | 1 | 0 | 1 | 1 |
| *690* | 2070 | 27 | | | | | | |
| *695* | 2085 | 27 | | | | | | |
| *700* | 2100 | 27 | | | | | | |
| *705* | 2115 | 27 | | | | | | |
| *710* | 2130 | 28 | H/L | 1 | 1 | 1 | 0 | 0 |
| *715* | 2145 | 28 | | | | | | |
| *720* | 2160 | 28 | | | | | | |
| *725* | *2175* | 28 | | | | | | |

*Table 1 Decode Frequency Data*

# Application Information .....

## Decoder Timing

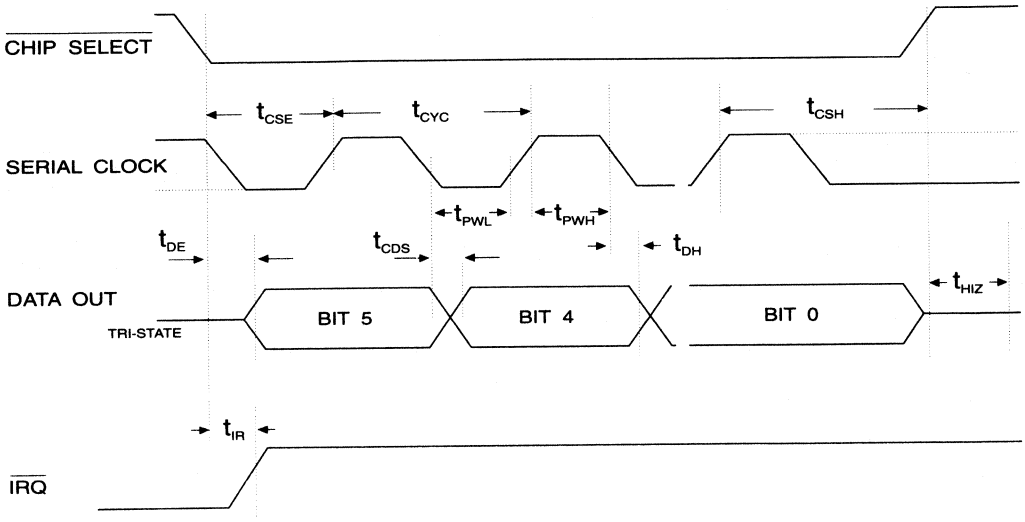



*Fig.4 Data-Read Timing*

## Decoder Timing Characteristics

With reference to Figure 4, *Data-Read Timing.*

| | Characteristics | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{PWH}$ | Serial Clock "High" Pulse Width | 250 | - | - | ns |
| $t_{PWL}$ | Serial Clock "Low" Pulse Width | 250 | - | - | ns |
| $t_{CYC}$ | Serial Clock-Cycle Time | 600 | - | - | ns |
| $t_{CSE}$ | Chip Select Low to Clock "High" Edge | 450 | - | - | ns |
| $t_{CSH}$ | Last Clock "High" Edge to CS "High" | 600 | - | - | ns |
| $t_{DH}$ | Data Out Hold Time | 0 | - | - | ns |
| $t_{CDS}$ | Clock Edge to Data Out Set Time | - | - | 200 | ns |
| $t_{IR}$ | Interrupt (IRQ) Reset Time | - | - | 200 | ns |
| $t_{DE}$ | Chip Select "Low" to Data Enable | - | - | 200 | ns |
| $t_{HIZ}$ | Chip Select "High" to Output Tri-State | - | - | 1000 | ns |

**Notes**

1 Data is output bit 5 first. Bit 5 can be clocked into the µProcessor by the first Serial Clock rising edge. If 8 Serial Clock pulses are employed the last 2 data-bits will be "0" and should be ignored by the software.

2 Chip Select should be used to react to Interrupts and then returned to a logic "1". If Chip Select stays low there will be no further Interrupts and no Data Output update.

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | |
|---|---|
| Supply voltage | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | +/- 30mA |
| (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | 800mW Max. |
| Derating | 10mW/°C |
| Storage temperature range: **FX613DW/P** | -40°C to +85°C (plastic) |

| **Operating Limits .....** | **Min.** | **Max.** | **Unit** | |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | 3.0 | 5.5 | V | at 25°C |
| Operating Temperature ..... | -40 | +85 | °C | |

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 3.3V, $T_{OP}$ = -40 to +85 °C. Audio Level 0dB ref: = 775mVrms. Xtal/Clock Frequency = 3.579545MHz

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Current | | - | 0.3 | 1.0 | mA |
| Input Logic "1" | | 70.0 | - | 100 | % $V_{DD}$ |
| Input Logic "0" | | 0 | - | 30.0 | % $V_{DD}$ |
| Output Logic "1" | 1 | 90.0 | - | 100 | % $V_{DD}$ |
| Output Logic "0" | 1 | - | - | 10.0 | % $V_{DD}$ |
| **Impedances** | | | | | |
| Chip Select and Serial Clock Input | | 10.0 | - | - | MΩ |
| Signal Input | | - | 50.0 | - | kΩ |
| Level Input | | - | 210 | - | kΩ |
| IRQ Output (logic "0") | | - | - | 500 | Ω |
| Data Output (logic "0") | | - | 500 | - | Ω |
| (Logic "1") | | - | - | 2.5 | kΩ |
| **Dynamic Values** | | | | | |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | - | - | MΩ |
| $R_{OUT}$ | | - | 230 | 825 | kΩ |
| DC Voltage Gain | | 25.0 | 42.0 | - | V/V |
| Bandwidth at Unity Gain | | 5.0 | 11.0 | - | MHz |
| **Single Tone Operation** | | | | | |
| Must-Decode Input Level | 2 | -25.2 | - | - | dB |
| Must-Not Decode Input Level | 2 | - | - | -46.0 | dB |
| LO Band Frequency Range | 4 | 300 | | 660 | Hz |
| HI Band Frequency Range | 4 | 900 | | 2150 | Hz |
| Frequency Resolution (Table 1) | | | | | |
| LO Band | | - | - | 25.0 | Hz |
| HI Band | | - | - | 75.0 | Hz |
| Input Signal/White-Noise Ratio (HI & LO Bands) | | - | 18.0 | - | dB |
| Interrupt Rate (LO Band) | 3 | 19.0 | - | - | /sec |
| (HI Band) | 3 | 57.0 | - | - | /sec |
| False Decodes Due to Noise | 6 | - | 1.0 | - | /2 secs |
| Outband modulation level limits for correct decode ($f_{IN}$ = 340Hz to 620Hz) | 5 | - | - | 10.0 | % |

**Notes**

1. Into a high-impedance load (>1.0MΩ).
2. Must decode signal above -25.2dB; Must Not decode signal below -46.0dB. If a supply other than 3.3 volts is used, levels will change pro-rata.
3. Under 'Pure Tone' input conditions.
4. For input frequencies of between 661Hz and 899Hz the FX613 will provide no reliable output.
5. With an amplitude modulating frequency of between 16.0Hz and 100Hz.
6. Test noise input = 5.0kHz at 100mVrms

## Package Outlines

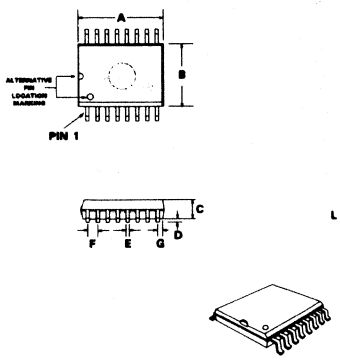
The FX613DW, the Small Outline Integrated Circuit (S.O.I.C.) package is shown in Figure 5, and the 'P' plastic version in Figure 6.

Pin 1 identification marking is shown on the relevant diagram and pins on both package styles number anti-clockwise when viewed from the top (marked side).

## Handling Precautions

The FX613 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

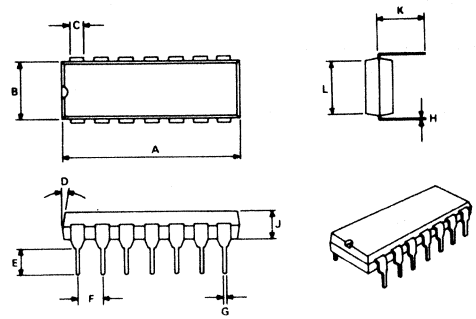
*Fig.5* ***FX613DW 16-pin S.O.I.C. Package***




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.31 | | 10.03 | G | | 0.66 | |
| B | 7.59 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.6* ***FX613P 14-pin plastic Package***




| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.24 | 18.86 |
| B | 6.41 | 6.29 |
| C | 1.54 | 1.51 |
| D | 7°30' | 6°30' |
| E | 3.20 | 3.15 |
| F | 2.54 | TYPICAL |
| G | 0.46 | |
| H | 0.25 | |
| J | 3.33 | 3.27 |
| K | 5.77 | 5.65 |
| L | 5.90 | 5.78 |

NOTE: All dimensions in mm. Angles in degrees.

## Ordering Information

**FX613DW** **16-pin plastic S.O.I.C.**

**FX613P** **14-pin plastic DIL**

# CML Semiconductor Products

PRODUCT INFORMATION

# FX621 Low-Power Subscriber Private Metering (SPM) Detector

Publication D/621/2 June 1991
Provisional Issue

## Features/Applications

- Meets 12kHz and 16kHz SPM Specifications
- Low-Power CMOS [ 3.5 – 5 Volt Operation ]
- Tone Follower and SPM Packet Detection Modes
- Adjustable Input Gain
- PABX, Payphone and Telephone Applications
- General-Purpose Tone Detection
- Crystal Oscillator Stability

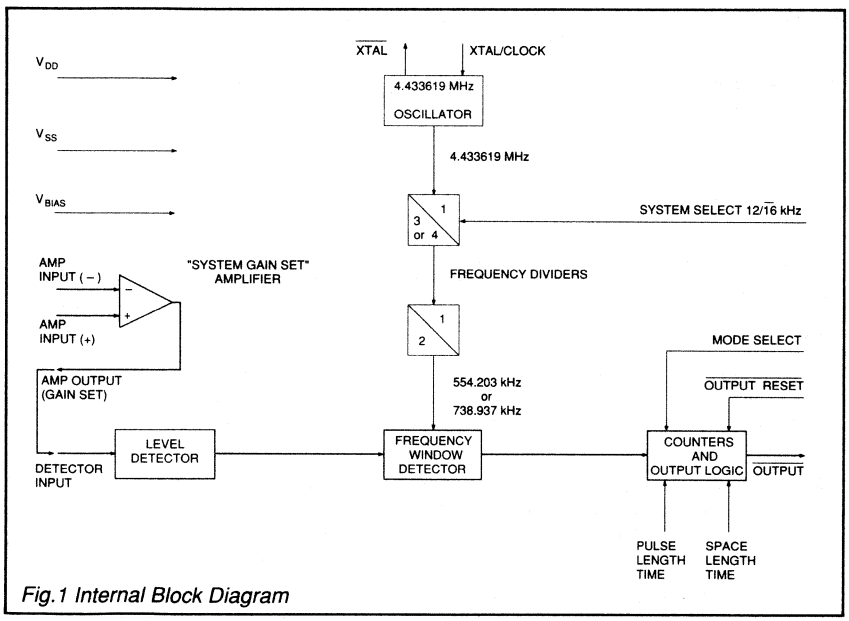



*Fig.1 Internal Block Diagram*

FX621

## Brief Description

The FX621 is a single-chip, low-power CMOS tone detector designed for use in both PABX and general payphone applications for Subscriber Private Metering.

The Decode and Not-Decode band edges are accurately defined by the use of an external 4.433619MHz crystal.

Operation to either of the 12kHz or 16kHz SPM systems is pin programmable, with system amplitude sensitivities and pulse-length timing being provided by the use of external components.

The FX621 has 2 pin-selectable modes of operation:

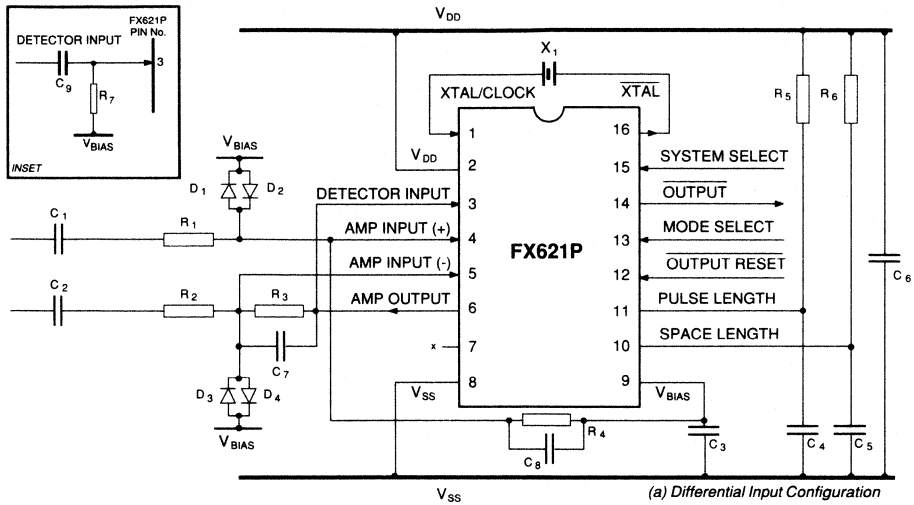
1) *Tone Follower Mode.*
   A logic "0" is output whenever a tone of the correct frequency and length is detected.
2) *SPM Packet Mode.*
   An output is obtained only when both the mark and space timing criteria of an input SPM tone have been fulfilled.

The FX621, which is available in plastic DIL and SMD packages, requires only a single 3.5-volt (min.) power supply, a 4.433619MHz crystal with external gain and timing components to meet most SPM specifications.

| Pin Number | | Function |
|---|---|---|
| DIL FX621P | Quad FX621LG/LS | |
| 1 | 1 | **Xtal/Clock:** Input to the clock oscillator inverter. A single 4.433619MHz Xtal or external clock pulse input is required (see Figure 2). |
| 2 | 2 | **$V_{DD}$:** The positive supply rail. A single, stable supply in the range 3.5V to 5V is required. |
| 3 | 5 | **Detector Input:** "Schmitt Trigger" level detector circuitry whose input thresholds are set internally and dependent on the applied $V_{DD}$. For use with low signal-level systems this input should be preceded by the "System Gain Set" amplifier. To use this input without the "System Gain Set" amplifier, the components indicated in Figure 2 (inset) should be used with the protection diodes ($D_1$ - $D_4$). |
| 4 | 6 | The positive and negative inputs to the "System Gain Set" Amplifier. **Amplifier Input (+):** With single or differential inputs this amplifier and its external circuitry can be used to provide the extra gain required to set the device to the user's National Level Specification. External diodes are used at both inputs (if in use) to provide protection when the line input level exceeds the supply rails (above the Absolute Maximum Rating). |
| 5 | 7 | **Amplifier Input (–):** If this device is used without this amplifier, the protection diodes should be employed at the Detector Input. See Figure 2. |
| 6 | 8 | **Amplifier Output:** The output of the "System Gain Set" Amplifier, is used with gain setting components. See Figures 1 and 2. |
| 8 | 12 | **$V_{SS}$:** The negative supply rail, (GND). |
| 9 | 13 | **$V_{BIAS}$:** The internal analogue bias pin, this point is at $V_{DD}/2$ and requires to be externally decoupled to $V_{SS}$ via capacitor $C_3$. |
| 10 | 14 | **Space Length Time:** Active only in the 'SPM Packet' mode, this input, with an external RC network, sets the minimum valid No-Tone (Space) period for the incoming packet using the formula: $t_S = 0.7\ (R_6 \times C_5)$. If the 'SPM Packet' mode is not required these timing components may be omitted. |
| 11 | 17 | **Pulse Length Time:** Active only in the 'SPM Packet' mode, this input, with an external RC network, sets the minimum valid Tone period for the incoming packet using the formula: $t_M = 0.7\ (R_5 \times C_4)$. If the 'SPM Packet' mode is not required these timing components may be omitted. |
| 12 | 18 | **$\overline{\text{Output Reset}}$:** This input is used only in the 'SPM Packet' mode. Once an SPM packet has been detected and an output generated (logic "0") from this device the output remains as set until this input is strobed to a logic "0." See Figure 3. This input has an internal 1MΩ pullup resistor. |
| 13 | 19 | **Mode Select:** A control pin to select either the 'Tone Follower' mode or the 'SPM Packet' mode. A logic "1" selects 'Tone Follower', a logic "0" selects 'SPM Packet.' This input has an internal 1MΩ pullup resistor (Tone Follower). |
| 14 | 20 | **$\overline{\text{Output}}$:** The digital output of the SPM Detector. In the 'Tone Follower' mode a valid tone gives a logic "0" and no-tone gives a logic "1." Tonebursts and tone dropouts of less than 16 cycles are ignored. In the 'SPM Packet' mode the output is set to a logic "0" when a valid 'packet' is measured. The output remains as set until reset by a logic "0" at the Output Reset function, see Figure 3. |
| 15 | 23 | **System Select:** A control pin to set the device to work on either a 12kHz (logic "1") or 16kHz (logic "0") SPM system. This input has an internal 1MΩ pullup resistor (12kHz). |
| 16 | 24 | **$\overline{\text{Xtal}}$:** The output of the clock oscillator inverter, see Figure 2. |
| 7 | 3, 4, 9, 10, 11, 15, 16, 21, 22. | No internal connection – leave open circuit. |

# Application Information

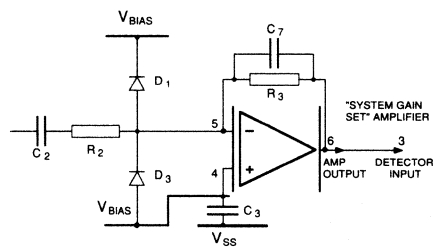
The notes on these pages are intended to assist in calculating the external components required to operate the FX621 as an SPM Detector.




*(a) Differential Input Configuration*

**Component References**

| Component | Reference | Component | Reference |
|---|---|---|---|
| $R_1$ | Note 4 | $C_1$ | Note 4 |
| $R_2$ | Note 4 | $C_2$ | Note 4 |
| $R_3$ | 390kΩ ± 1.0% | $C_3$ | 1.0µF ± 20% |
| $R_4$ | 390kΩ ± 1.0% | $C_4$ | Note 5 |
| $R_5$ | Note 5 | $C_5$ | Note 5 |
| $R_6$ | Note 5 | $C_6$ | 1.0µF ± 20% |
| $R_7$ | 1.0MΩ | $C_7$ | 12.0pF ± 10.0% |
| $D_1$ to $D_4$ | 1N4148 or equivalent (small signal type) | $C_8$ | 12.0pF ± 10.0% |
| | | $C_9$ | 0.1µF ± 10.0% |
| $X_1$ | 4.433619MHz | | |




*(b) Single Input Configuration*

*Fig.2 Recommended External Components*

# Gain Component Calculations

***(1)*** **Calculate** the FX621 sensitivity.

**Device Sensitivity** – at the Detector Input (Figure 1) is dependent upon the $V_{DD}$ value and is calculated as:

$$\text{Device Sensitivity} \approx \frac{0.2 \times V_{DD}}{2 \times \sqrt{2}} \quad (Vrms)$$

***(2)*** **Ascertain** the required National {Minimum Will-Decode} and [Maximum Will-Not Decode] Levels.

***(3)*** **Calculate** the acceptable range of required Gain/Attenuation for the levels in Note 2, using the "System Gain Set" amplifier.

The gain requirement is calculated as :

$$\text{[Max] / \{Min\} Gain} = \frac{\text{Device Sensitivity}}{\text{\{ Minimum Will-Decode Level \}}}$$

*[or]* [ Maximum Will-Not Decode Level ]

Choose a gain figure that meets both level requirements.

***(4)*** **Calculate** the gain/attenuation components for the chosen gain.

**Gain Components** – for a differential input:

$$R_1 = R_2 \qquad C_8 = C_7$$
$$R_3 = R_4 \qquad C_1 = C_2$$

$$\text{Gain} = \frac{Z_{Feedback}}{Z_{Input}} \quad \frac{(R_4 \,//\, X(C_8))}{(R_1 + X(C_1))}$$

*This calculation approximates as:*

$$R_1 \approx \frac{R_4}{1.2 \times \text{(selected gain)}}$$

and $$C_1 \approx \frac{1}{2\pi \times R_1 \times 6.0\text{kHz}}$$

– using the nearest preferred value components.

The values of $R_1$ and $C_1$ have been calculated to give a high-pass cut-off between the audio and SPM tone frequencies, approximately 6kHz. $C_7$ and $C_8$ are anti-alias components and are calculated for an approximate cut-off frequency of 32kHz.

# Application Information...

### (5) Timing Components

In the 'SPM Packet' mode $R_5$ and $C_4$ set the minimum 'Tone' period ($t_M$), $R_6$ and $C_5$ set the minimum 'Space' period ($t_S$), and are calculated as follows:

$$t_M = 0.7(R_5 \times C_4). \qquad t_S = 0.7(R_6 \times C_5).$$

*When calculating Tone and Space time settings the following points should be taken into consideration:*

*(1) Response and De-response times $t_R$ and $t_D$.*
*(2) Component tolerances can alter the calculation.*
*(3) The MINIMUM expected pulse/space length must be catered for.*

### (6) Protection Diodes

As most telephone systems operate at voltages in excess of the Absolute Maximum Limits for damage, diodes $D_1$ – $D_4$ are essential for device protection.

### (7) Component Tolerances

The tolerances of external components used with this device are dependent upon the required accuracy of the gain and pulse period timings.

## Timing

Figure 3 shows the FX621 output timing – Timing value limits are given on the "Specification" page.

*Note* – There is no reaction to pulses or drop-outs of less than the valid Response or De-response time.

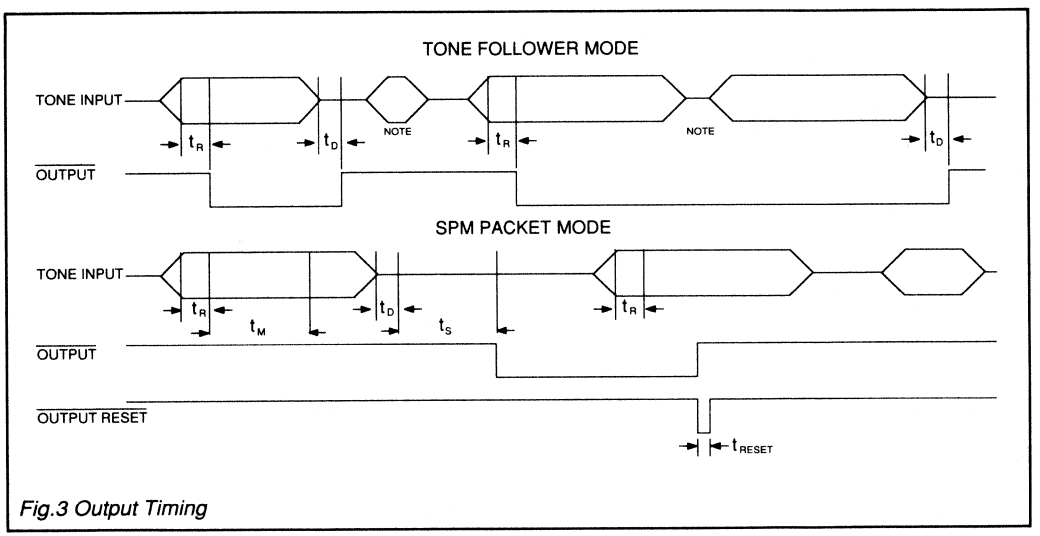



*Fig.3 Output Timing*

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**Example Values** – for the FX621 to operate with the West German (16kHz) 'FTZ' Specification.

| | | | |
|---|---|---|---|
| (a) Min. 'Will Decode' Level | = | 71.3 mV rms | |
| (b) Max. 'Will Decode' Level | = | 10.0 V rms | |
| (c) Max. 'Will-Not Decode' Level | = | 34.6 mVrms | |
| (d) Device Sensitivity @ 3.5V $V_{DD}$ | ≈ | 248.0 mVrms | |
| Min. Gain Required *(d÷a)* | ≈ | 3.47 | |
| Max. Gain Allowed *(d÷c)* | ≈ | 7.17 | |
| Chosen Gain Figure | = | 4.7 | |

For a chosen gain figure of 4.7, a minimum Tone length of 80ms, a minimum Space length of 135ms and a $V_{DD}$ of 3.5V, the required component values are :

| | | | |
|---|---|---|---|
| $R_1$ | 68kΩ | $C_1$ | 330pF |
| $R_2$ | 68kΩ | $C_2$ | 330pF |
| $R_3$ | 390kΩ | $C_3$ | 1.0µF |
| $R_4$ | 390kΩ | $C_4$ | 820nF |
| $R_5$ | 100kΩ | $C_5$ | 1.0µF |
| $R_6$ | 120kΩ | $C_6$ | 1.0µF |
| | | $C_7$ | 12pF |
| $X_1$ | 4.433619MHz | $C_8$ | 12pF |

Tolerances: Resistors = ±1%. Capacitors = ±10%.

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply Voltage | | -0.3 to 7.0V |
| Input Voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | ± 30mA |
| (other pins) | | ± 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX621P/LG/LS** | -30°C to + 70°C |
| Storage temperature range: | **FX621P/LG/LS** | -40°C to + 85°C |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified :

$V_{DD}$ = 3.5V $T_{AMB}$ = 25°C Xtal/Clock $f_C$ = 4.433619MHz Audio level 0dB ref = 775mV rms

| Characteristics | System | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Values** | | | | | | |
| Supply Voltage ($V_{DD}$) | | | 3.5 | – | 5.0 | V |
| Supply Current ($I_{DD}$) | | | – | 1.0 | 1.4 | mA |
| Input Logic "1" | | | 70.0 | – | 100 | % $V_{DD}$ |
| Input Logic "0" | | | 0 | – | 30.0 | % $V_{DD}$ |
| Output Logic "1" | | | 80.0 | – | – | % $V_{DD}$ |
| Output Logic "0" | | | – | – | 20.0 | % $V_{DD}$ |
| **Impedances** | | | | | | |
| "Gain Set" Amplifier Input | | | 1.0 | – | – | MΩ |
| "Gain Set" Amplifier Output | | | – | – | 10.0 | kΩ |
| Analogue Detector Input | | | 1.0 | – | – | MΩ |
| Digital Inputs | | | 0.5 | 1.0 | – | MΩ |
| Digital Output | | | – | – | 10.0 | kΩ |
| **Dynamic Values** | | | | | | |
| Sensitivity | 12kHz/16kHz | 1, 2 | – | 248 | – | mVrms |
| Required Signal to Noise Ratio | | 7 | – | 45.0 | – | dB |
| Upper Detector Threshold | | 2 | 2.06 | 2.1 | 2.14 | V |
| Lower Detector Threshold | | 2 | 1.36 | 1.4 | 1.44 | V |
| Amplifier Input Offset | | | – | 15.0 | – | mV |
| Xtal Oscillator Frequency | | | | 4.433619 | | MHz |
| **Frequency Discrimination** | | | | | | |
| 'Will-Decode' Frequency Limits | 12kHz | | 11.82 | – | 12.18 | kHz |
| | 16kHz | | 15.76 | – | 16.24 | kHz |
| 'Will-Not Decode' Frequency Limits | 12kHz | | 0 | – | 11.52 | kHz |
| | 12kHz | | 12.48 | – | – | kHz |
| | 16kHz | | 0 | – | 15.36 | kHz |
| | 16kHz | | 16.64 | – | – | kHz |
| **Timing Information** – Fig.3 | | | | | | |
| Valid Tone Burst Length ($t_M$) | 12/16kHz | 3, 4 | 16.0 | – | – | cycles |
| Valid Space Length ($t_S$) | 12/16kHz | 4 | 5.0 | – | – | ms |
| Tone Response Time ($t_R$) | 12kHz | 5, 7 | – | 1.7 | 3.0 | ms |
| | 16kHz | 5, 7 | – | 1.2 | 2.0 | ms |
| De-response Time ($t_D$) | 12kHz | 6, 7 | – | 1.7 | 3.0 | ms |
| | 16kHz | 6, 7 | – | 1.2 | 2.0 | ms |
| SPM Output Reset Time ($t_{RESET}$) | 12/16kHz | 4 | 150.0 | – | – | ns |

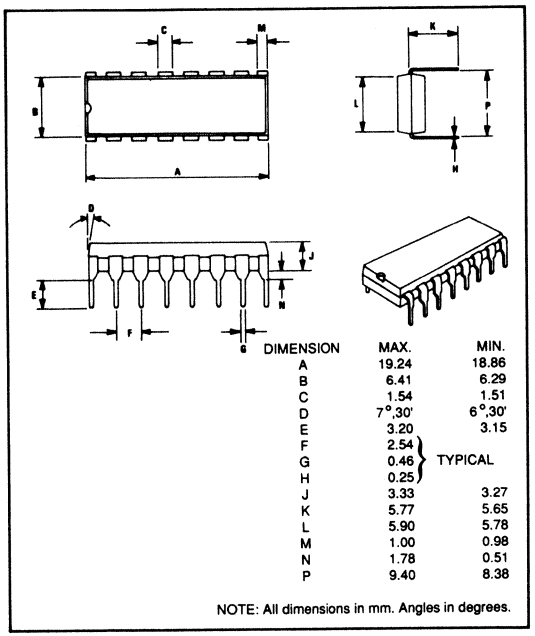
**Notes**

1. Device sensitivity at the Detector Input pin, or using the 'Gain Set' Amplifier at unity.
2. These values are quoted at 3.5 volt $V_{DD}$, any supply variation will alter levels accordingly.
3. Tone Follower mode.
4. SPM Packet mode, in this mode the minimum valid Pulse (Space) length is programmable by means of an RC network on the Pulse (Space) Length Time pin. If no RC network is used, the minimum valid tone length reverts to 16 cycles.
5. The time for the circuit to recognize a valid 'Tone' in the Tone Follower mode.
6. The time for the circuit to recognize a valid 'No Tone' in the Tone Follower mode.
7. The FX621 is a low-power zero crossing detector without on-chip filtering, for use with a good Signal-to-Noise ratio. The *FX611* is recommended for high noise environments. If the supply current requirement of the *FX611* is unacceptable, separate external filters should be employed with the FX621.

## Package Outline

The FX621P package is shown in Figure 4. The 'LG' version is shown in Figure 5, and the 'LS' version in Figure 6.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4.
Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 4* **FX621P** *16-pin DIL Package*



| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.24 | 18.86 |
| B | 6.41 | 6.29 |
| C | 1.54 | 1.51 |
| D | 7°,30' | 6°,30' |
| E | 3.20 | 3.15 |
| F | 2.54 | TYPICAL |
| G | 0.46 | TYPICAL |
| H | 0.25 | |
| J | 3.33 | 3.27 |
| K | 5.77 | 5.65 |
| L | 5.90 | 5.78 |
| M | 1.00 | 0.98 |
| N | 1.78 | 0.51 |
| P | 9.40 | 8.38 |

NOTE: All dimensions in mm. Angles in degrees.

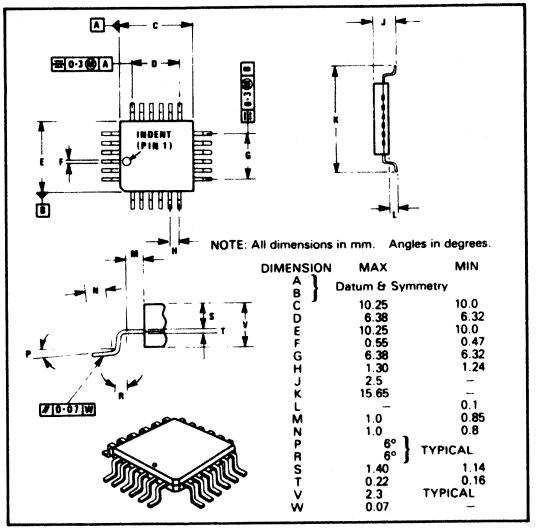
## Ordering Information

| | |
|---|---|
| **FX621P** | **16-pin plastic DIL** |
| **FX621LG** | **24-pin quad plastic encapsulated bent and cropped** |
| **FX621LS** | **24-lead plastic leaded chip carrier** |

## Handling Precautions

The FX621 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

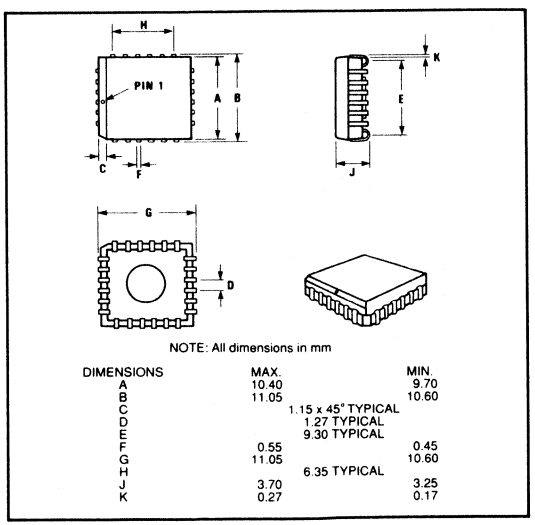
*Fig. 5* **FX621LG** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig. 6* **FX621LS** *24-lead Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX623 Call Progress Tone Decoder

Publication D/623/2 February 1993
Provisional Issue

## Features

- **Measures Call Progress Tone Frequencies ['Busy', 'Dial', 'Fax-Tone' etc.]**
- **Telephone, PABX, Fax and Dial-Up Modem Applications**
- **Low-Power Requirement (600µA at 3.3 Volts$_{TYP}$) for Line-Powered Applications**
- **Custom Tone Decoder [13 Call-Progress Frequencies Recognized]**
- **Operates to a 3.579545MHz Telephone System Clock**
- **Operates Under Simple Logic or µProcessor System Control**

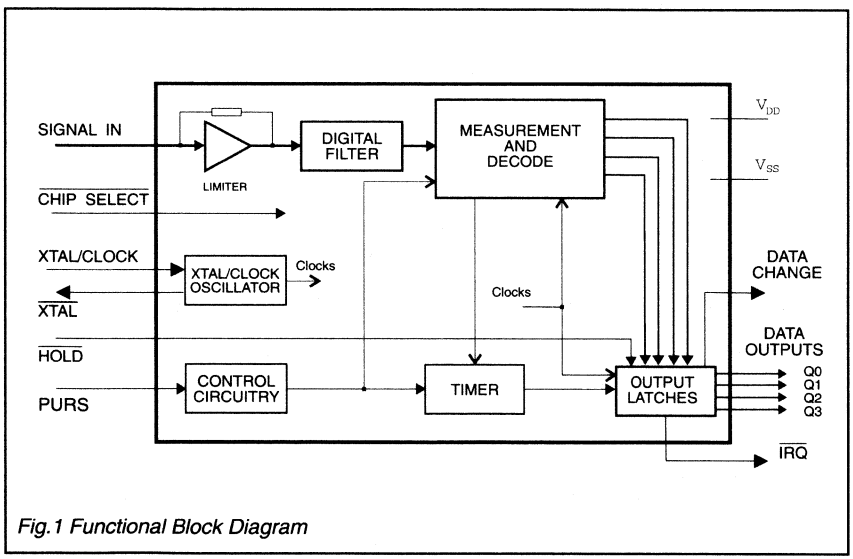



*Fig.1 Functional Block Diagram*

**FX623**

## Brief Description

The FX623 is a low-power decoding microcircuit that measures the frequency of telephone system call progress tones.

With progress signals input from the telephone line, this single-chip product is programmed to recognize up to thirteen of the World's most commonly used call-progress frequencies, analyze signal quality and present the measured result as a 4-bit parallel data word at the tri-state Data Output.

Using the parallel information from the FX623, the host system suitably configured, can recognize such call progress information as: 'Dial', 'Busy', 'Number Unobtainable', 'Ringing' and Fax/Modem system signals.

This information can then be employed in telephone applications (simple or complex) to control telephone operations. The data output will require a suitable software format to analyze the frequency information from the FX623.

Requiring only a single 3.0$_{[MIN]}$ volt power supply, the FX623 may be line-powered and will operate under simple logic or system µProcessor control using the 'Data-Change, 'Hold' and 'Chip-Select' functions.

The FX623, whose small size and low power consumption makes it ideal for remote applications, requires a 3.579545MHz telephone system clock or Xtal input, is available in a 16-pin plastic DIL package.

| Pin Number FX623P | Function |
|---|---|
| 1<br>2<br>3<br>4 | **Q3:** **Data Outputs:** A 4-bit parallel data word, forming a HEX character representing the<br>**Q2:** decoded tone frequency. This word is output after a successful decode. Table 1 details the<br>**Q1:** Hex character output codes for the relevant decoded tone frequencies. Upon power-up this<br>**Q0:** output is set to '$E_H$', but no Data Change pulse generated. These are tri-state outputs. |
| 5 | **$V_{DD}$:** Positive supply rail. A minimum supply voltage of 3.0 volts is required. Levels and voltages within this decoder are dependent upon this supply. |
| 6 | **Signal In:** The composite audio input. Signals to this pin should be a.c. coupled. The d.c. bias of the limiter section is set internally; this pin should not be loaded with any other circuitry. |
| 7 | No internal connection. Leave open circuit. |
| 8 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter. |
| 9 | No internal connection. Leave open circuit. |
| 10 | **Xtal/Clock:** The input to the clock oscillator inverter. A 3.579545MHz Xtal or externally derived clock should be connected here (see Figure 2). |
| 11 | **$V_{SS}$:** Negative supply rail (GND). |
| 12 | **$\overline{\text{Hold}}$:** An input to control the Output Latch condition; employed in combination with the Data Change output to facilitate, if required, Interrupt and/or handshake operations with a µProcessor. With Hold placed "Low", with a tone input, the Data Change output will be held "High" at the next data change, and the current output code is locked in the Output Latches regardless of any changes to the input signal.<br>The output code remains as held until this input is returned "High" (see Figure 3). Whilst this input is "High" the output data, Q0 - Q3, cycles normally with the input audio.<br>This pin has an internal 1.0MΩ pullup resistor. |
| 13 | **PURS:** Power-Up ReSet. To reset internal circuitry at power-up; a logic "1" level is required at this pin for a duration of at least 2.5mS after the Xtal/Clock input and full $V_{DD}$ levels are applied.<br>The component configuration shown in Figure 2 is recommended; for slow-rising power supplies the time constant of components should be increased accordingly. |
| 14 | **$\overline{\text{IRQ}}$:** Interrupt Request. An output for µProcessor operation; normally "High" this output is latched "Low" when an internal data change occurs if the Chip Select input is "High". This output is reset ("High") the when Chip Select line is taken "Low".<br>To permit "wire-OR" connection with other peripherals, this output has a low-impedance when "Low" and a high-impedance when "High". |
| 15 | **$\overline{\text{CS}}$:** Chip Select- A controlling function. When held "High" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are disabled.<br>When taken "Low" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are enabled; the Interrupt Request (IRQ) is reset ("High") when CS is taken "Low". See Figures 3 and 4. |
| 16 | **Data Change:** A positive-going pulse is generated at this output when the data changes (Tone or NOTONE). New tone-data is presented to the Q0, Q1, Q2 and Q3 Data Outputs if the Hold input is set "High". This is a tri-state output. |

## Application Information

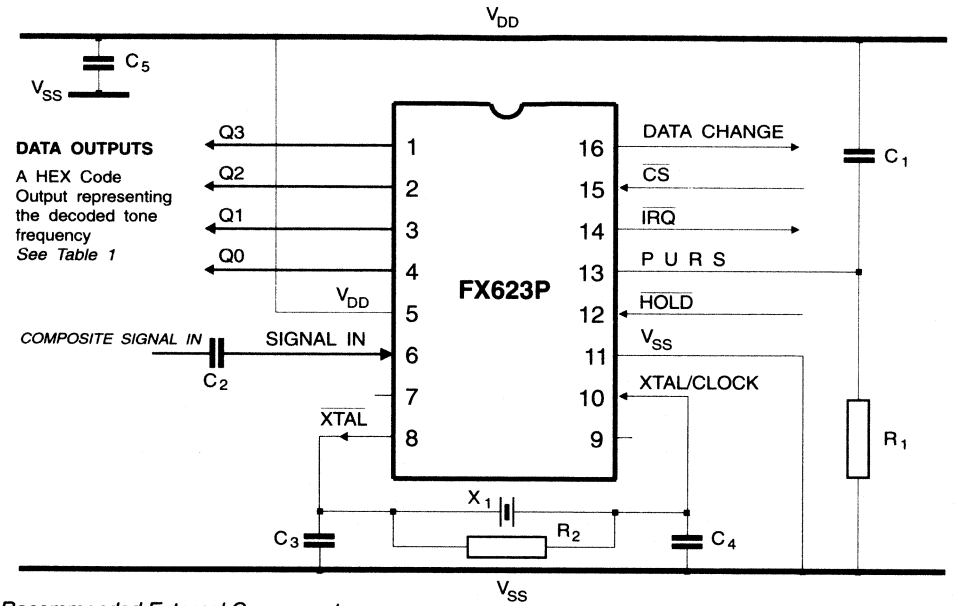



*Fig.2 Recommended External Components*

| Hex Character | Output Code Q3 | Q2 | Q1 | Q0 | Band Edges (Hz) Lower Edge | Upper Edge | Nominal Centre Freq. |
|---|---|---|---|---|---|---|---|
| **0** | 0 | 0 | 0 | 0 | 364 | 386 | *375* |
| **1** | 0 | 0 | 0 | 1 | 488 | 520 | *500* |
| **2** | 0 | 0 | 1 | 0 | 520 | 580 | *550* |
| **3** | 0 | 0 | 1 | 1 | 580 | 618 | *600* |
| **4** | 0 | 1 | 0 | 0 | 386 | 412 | *400* |
| **5** | 0 | 1 | 0 | 1 | 412 | 436 | *425* |
| **6** | 0 | 1 | 1 | 0 | 436 | 463 | *450* |
| **7** | 0 | 1 | 1 | 1 | 463 | 487 | *475* |
| **8** | 1 | 0 | 0 | 0 | 900 | 1008 | *950* |
| **9** | 1 | 0 | 0 | 1 | 1273 | 1325 | *1300* |
| **A** | 1 | 0 | 1 | 0 | 1350 | 1455 | *1400* |
| **B** | 1 | 0 | 1 | 1 | 1750 | 1855 | *1800* |
| **C** | 1 | 1 | 0 | 0 | 2062 | 2140 | *2100* |
| **D** | 1 | 1 | 0 | 1 | frequency not guaranteed | | |
| **E** | 1 | 1 | 1 | 0 | frequency not guaranteed | | |
| **F** | 1 | 1 | 1 | 1 | NOTONE | | |

*Table 1 Tone Decode Frequencies*

| Component | Value |
|---|---|
| $R_1$ | 1.0MΩ |
| $R_2$ | 1.0MΩ |
| $C_1$ | 47.0nF |
| $C_2$ | 4.7nF |
| $C_3$ | 33.0pF |
| $C_4$ | 33.0pF |
| $C_5$ | 1.0µF |
| $X_1$ | 3.579545MHz |
| *Tolerances R = ±10%* | *C = ±20%* |

## Timing Information

*With CS Low - Figure 3.*

After initial power-up and the Hold input inactive (High), as frequencies are input, with the Data Change output as an active (High) indicator, the data is presented at the Data Outputs.

If/when the Hold input is placed active (Low), the data at the Data Outputs is frozen and the Data Change output held High at its next active excursion -until the Hold input is returned High.

*With the Hold input held High - Figure 4.*

As frequencies are input a correct decode will produce an active (Low) interrupt level.

This interrupt (IRQ) is serviced and reset by an active (Low) CS input.

Note the 'valid data' period at the Data Outputs.

# Application Information

## Decoder Timing

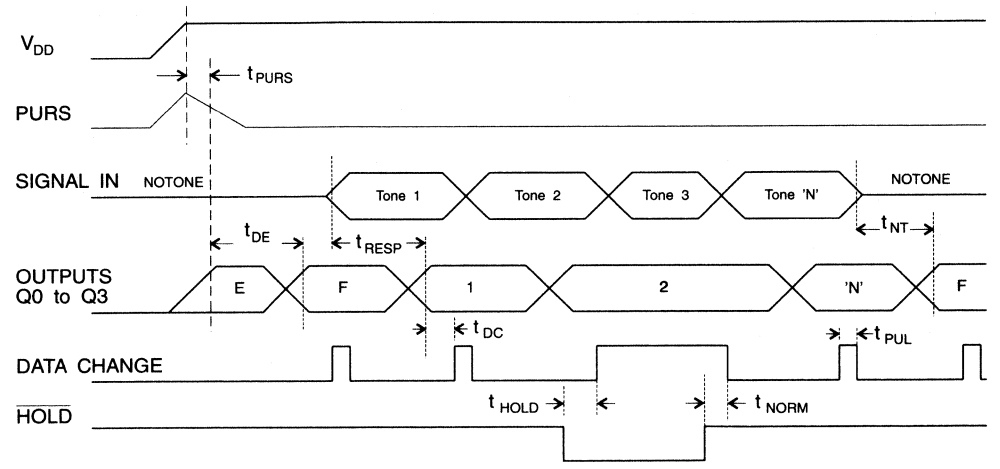



*Fig.3 Timing with the Chip Select Input Held "Low"; CS and IRQ are not used*

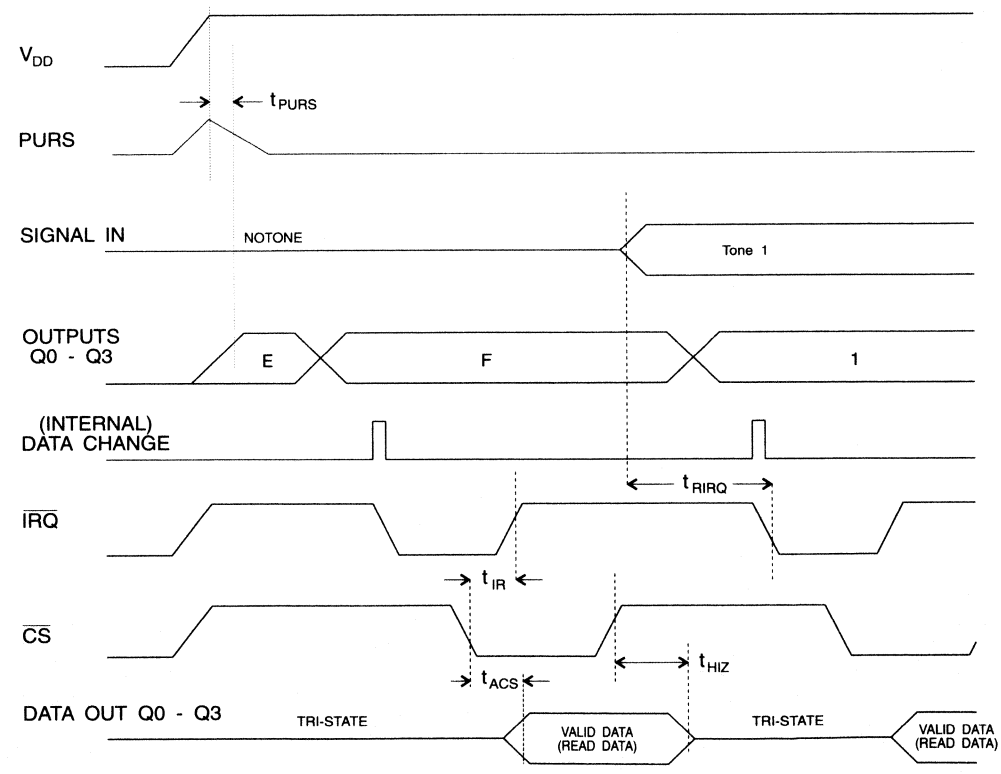



*Fig.4 Timing with the HOLD Input Held "High"; CS and IRQ are used*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | |
|---|---|
| Supply voltage | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | +/- 30mA |
| (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | 800mW Max. |
| Derating | 10mW/°C |
| Storage temperature range: **FX623P** | -40°C to +85°C (plastic) |

## Operating Limits .....

| | Min. | Max. | Unit | |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | 3.0 | 5.5 | V | at 25°C |
| Operating Temperature ..... | -40 | +85 | °C | |

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 3.3V, $T_{OP}$ = -40 to +85 °C. Audio Level 0dB ref: = 775mVrms. Xtal/Clock Frequency = 3.579545MHz

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Values** | | | | | | |
| Supply Current | | | - | 0.6 | 1.0 | mA |
| Input Logic "1" | | | 0.7 | - | - | $\%V_{DD}$ |
| Input Logic "0" | | | - | - | 0.3 | $\%V_{DD}$ |
| Output Logic "1" | | | 0.8 | - | - | $\%V_{DD}$ |
| Output Logic "0" | | | - | - | 0.2 | $\%V_{DD}$ |
| **Impedance** | | | | | | |
| CS and PURS Input | | | 10.0 | - | - | MΩ |
| Hold Input | | 1 | 0.5 | - | - | MΩ |
| Signal Input | | | 0.1 | - | - | MΩ |
| IRQ Output (logic "1") | | | - | 30.0 | 100 | kΩ |
| IRQ Output (logic "0") | | | - | 175 | 500 | Ω |
| Q0 - Q3 & Data-Change Outputs (logic "1") | | | - | 0.7 | 2.0 | kΩ |
| Q0 - Q3 & Data-Change Outputs (logic "0") | | | - | 175 | 500 | Ω |
| Q0 - Q3 & Data-Change Outputs (high Z) | | | 1.0 | - | - | MΩ |
| **Dynamic Values** | | | | | | |
| Signal Input Range | | 2, 5 | 35.0 | | 1,166 | mVrms |
| Decode Bandedge Tolerance | | 3 | -1.0 | - | 1.0 | % |
| **Xtal Inverter** | | | | | | |
| Voltage Gain | | | 20.0 | - | - | V/V |
| Input Impedance | | | 10.0 | - | - | MΩ |
| Output Impedance | | | - | - | 160 | kΩ |
| **Decoder Timing** - *Figures 3 and 4* | | | | | | |
| Power Up Reset Time | $t_{PURS}$ | | 2.5 | - | - | ms |
| Data 'E' Time | $t_{DE}$ | | 31.0 | - | - | ms |
| NOTONE to Tone Response Time | $t_{RESP}$ | 4 | - | 27.0 | 50.0 | ms |
| Tone to NOTONE Response Time | $t_{NT}$ | 4 | - | - | 60.0 | ms |
| Data to Data-Change Pulse Time | $t_{DC}$ | | 0.625 | - | 1.15 | ms |
| Data-Change Pulse Width | $t_{PUL}$ | | - | 1.25 | - | ms |
| Hold to Data-Change Rise Time | $t_{HOLD}$ | | 63.0 | - | - | µs |
| HOLD to Data-Change Fall Time | $t_{NORM}$ | | - | - | 150 | µs |
| IRQ Tone Response Time | $t_{RIRQ}$ | | - | 29.0 | 52.0 | ms |
| IRQ Reset Time | $t_{IR}$ | | - | - | 250 | ns |
| Data Access Time | $t_{ACS}$ | | - | - | 250 | ns |
| CS High to Output Tri-State Time | $t_{HIZ}$ | | - | - | 100 | ns |

Notes

1. This pin has an on-chip 1.0MΩ pullup resistor.
2. An a.c. coupled sine or squarewave.
3. See Table 1, Tone Decode Frequencies.
4. Delay between the change of input (Tone/NOTONE) and the change at the Q0 - Q3 outputs.
5. The signal input maximum value is determined by the formula $V_{DD}/2.83$.

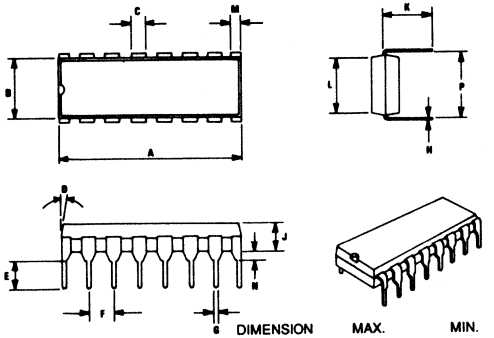
## Package Outlines

The FX623P plastic package is shown in Figure 5. Pin 1 identification marking is shown on the diagram and pins number anti-clockwise when viewed from the top (marked side).

## Handling Precautions

The FX623 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

*Fig.5* ***FX623P 16-pin plastic Package***



| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.24 | 18.86 |
| B | 6.41 | 6.29 |
| C | 1.54 | 1.51 |
| D | 7°,30' | 6°,30' |
| E | 3.20 | 3.15 |
| F | 2.54 | TYPICAL |
| G | 0.46 | TYPICAL |
| H | 0.25 | TYPICAL |
| J | 3.33 | 3.27 |
| K | 5.77 | 5.65 |
| L | 5.90 | 5.78 |
| M | 1.00 | 0.98 |
| N | 1.78 | 0.51 |
| P | 9.40 | 8.38 |

NOTE: All dimensions in mm. Angles in degrees.

## Ordering Information

**FX623P** **16-pin plastic DIL**

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX631 Low-Voltage SPM Detector

Publication D/631/2 February 1993
Advance Information

## Features

- **Detects 12kHz and 16kHz SPM Frequencies**
- **Low Power (3.0 $Volt_{MIN}$ <1.0mA) Operation**
- **High Speechband Rejection Properties**
- **Tone-Follower and Packet Mode Outputs**
- **Applications**
  - **Complex and/or Simple Telephone Systems**
  - **Call-Charge/-Logging Systems**

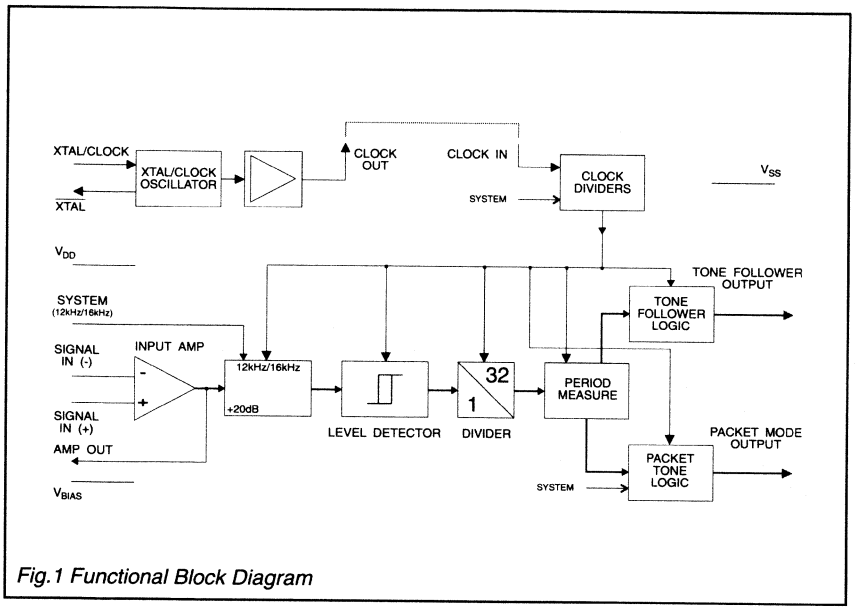



*Fig.1 Functional Block Diagram*

FX631

## Brief Description

The FX631 is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector to indicate the presence, on a telephone line, of both 12kHz and 16kHz telephone call-charge frequencies.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier, whilst the 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The FX631, which demonstrates high 12kHz and 16kHz performance in the presence of both voice and noise, can operate from either a single or differential analogue signal input from which it will produce two individual logic outputs.

1. Tone Follower Output - A 'tone-following' logic output producing a "Low" level for the period of a correct decode and a "High" level for a bad decode or NOTONE.
2. Packet (Cumulative Tone) Mode Output - To respond and de-respond after a cumulative 40ms of good tone (or NOTONE) in any 48ms period.
   This process will ignore small fluctuations or fades of a valid frequency input and is available for µProcessor 'Wake-Up', Minimum tone detection, NOTONE indication or transient avoidance.

This system (12kHz/16kHz) selectable microcircuit, which may be line-powered, is available in 16-pin plastic DIL and small outline surface mount packages.

| Pin Number<br>FX631<br>DW/P | Function |
|---|---|
| 1 | **Xtal/Clock :** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the $\overline{\text{Xtal}}$ output (see Figure 2); circuit components are on chip. Using this mode of clock operation, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is employed to the Clock In pin, this pin must be connected directly to $V_{DD}$ (see Figure 2). |
| 2 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter. |
| 3 | **Clock Out:** The buffered output of the on-chip clock oscillator inverter. If a Xtal input is employed this output should be connected directly to the Clock In pin. |
| 4 | **Clock In:** The 3.579545MHz clock pulse input to the internal clock-dividers. If a clock pulse input is employed, the Xtal/Clock input (Pin 1) should be connected to $V_{DD}$. See Figure 2. |
| 5 | No internal connection, leave open circuit. |
| 6 | No internal connection, leave open circuit. |
| 7 | **$V_{BIAS}$:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to $V_{SS}$ (see Figure 2). |
| 8 | **$V_{SS}$:** Negative supply rail (GND). |
| 9<br>10<br>11 | **Signal In (+):**<br>**Signal In (-):**<br>**Amp Out:**<br>The positive and negative signal inputs to, and the output from, the input gain adjusting signal amplifier. Refer to the graph in Figure 4 for guidance on setting level sensitivities to national specifications, and the selection of gain adjusting components. |
| 12 | No internal connection, leave open circuit. |
| 13 | **Tone Follower Output:** This output provides a logic "0" (Low) for the period of a detected tone, and a logic "1" (High) for NOTONE detection. See Figure 6. |
| 14 | **Packet Mode Output:** A logic output that will be available after a cumulation of 40ms of 'good' tone has been received. This packet mode tone follower will only respond when a tone frequency of sufficient quality has been received for sufficient time, i.e. a cumulation of 40ms in any 48ms, short tone bursts or breaks will be ignored. This output provides a logic "0" (Low) for a detected tone and a logic "1" (High) for NOTONE detection. See Figure 6. |
| 15 | **System:** The logic input to select device operation to either 12kHz (logic "1" - High) or 16kHz (logic "0" - Low) SPM systems. This input has an internal 1MΩ pullup resistor (12kHz). |
| 16 | **$V_{DD}$:** Positive supply rail. A single, stable power supply is required. Critical levels and voltages within the FX631 are dependant upon this supply. This pin should be decoupled to $V_{SS}$ by a capacitor mounted close to the pin.<br>Note that if this device is 'line' powered, the resulting supply must be stable. See notes on Microcircuit Protection from high and spurious line voltages. |

# Application Information
## External Components

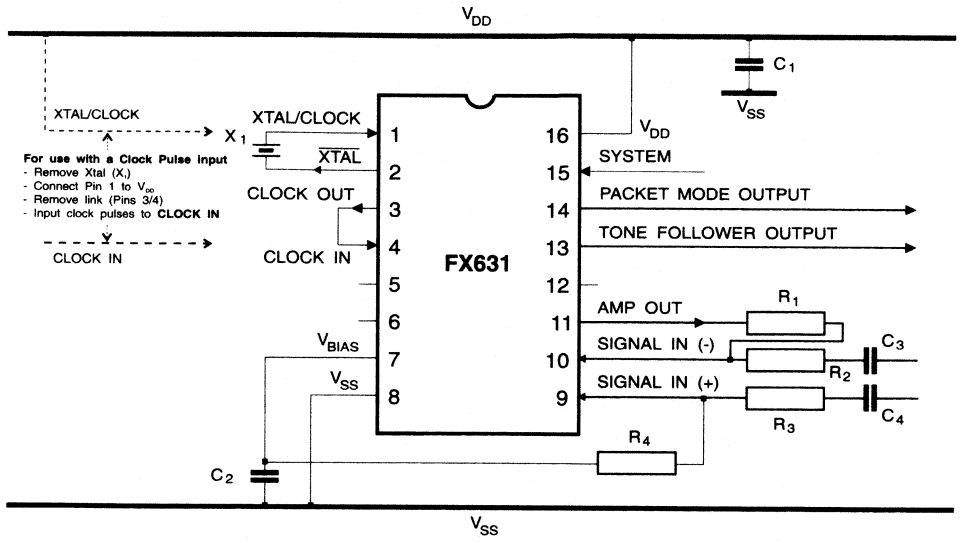



*Fig.2 Recommended External Components - Differential Input Mode*

| Component | Value |
|---|---|
| $R_1$ | $R_{FEEDBACK}$ |
| $R_2$ | $R_{IN(-)}$ |
| $R_3$ | $R_{IN(+)}$ |
| $R_4$ | $R_{BIAS}$ |
| $C_1$ | 1.0µF ±20% |
| $C_2$ | 1.0µF ±20% |
| $C_3$ | $C_{IN(-)}$ |
| $C_4$ | $C_{IN(+)}$ |
| $X_1$ | 3.579545MHz |

**External Components**

1. The values of the Input Amp gain components illustrated are calculated using the Input Gain Calculation Graph (Figure 4).
   Whilst calculating input gain components, for correct operation, it is recommended that the values of resistors $R_1$ and $R_4$ are always greater than, or equal to, 100kΩ.

2. Refer to following pages for advice on Microcircuit Protection from high and spurious line voltages.

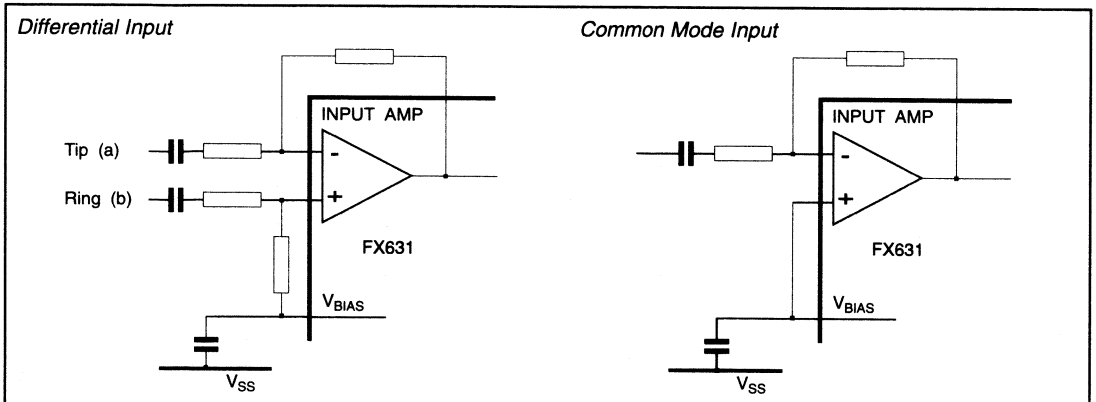



*Fig.3 Example Input Configurations*

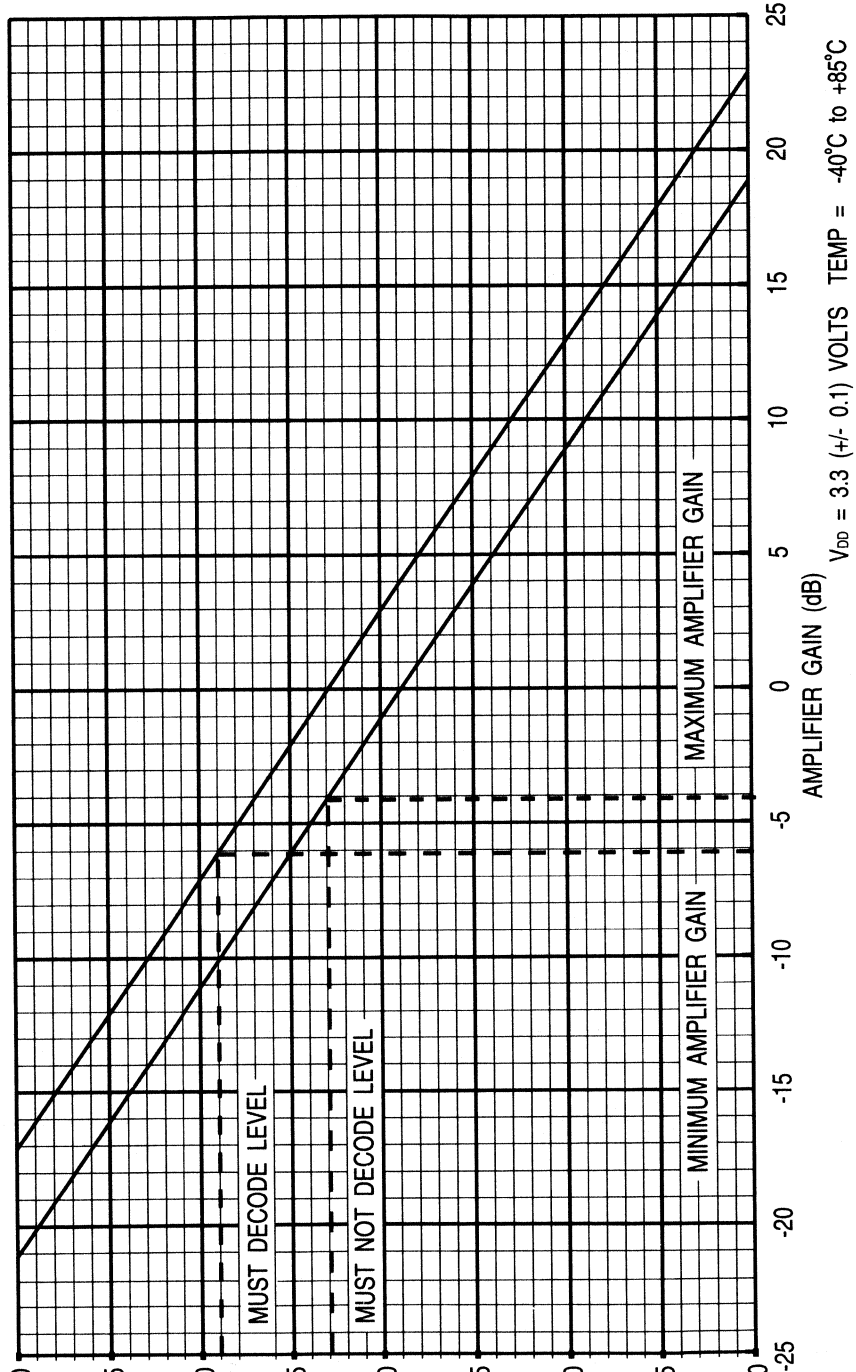



*Fig.4 Input Gain Calculation Graph*

# Application Information .....

## Input Gain Calculation

The input amplifier, with its external circuitry, is provided on-chip to set the sensitivity of the FX631 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graph in Figure 4, the following steps will assist in the determination of the required gain/attenuation.

**Step 1**

Draw two horizontal lines from the Y-axis (Signal Levels (dB)).
The upper line will represent the required 'Must' decode level.
The lower line will represent the required 'Must-Not' decode level.

**Step 2**

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).
The point where the vertical line meets the X-axis will indicate the MINIMUM Input Amp gain required for reliable decoding of valid signals.

**Step 3**

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.
The point where the vertical line meets the X-axis will indicate the MAXIMUM allowable Input Amp gain.
Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.
Select the gain components as described opposite.

## Input Gain Components

With reference to the gain components shown in Figures 2 and 3.

The user should calculate and select external components ($R_1$, $R_2/C_3$, $R_3/C_4$, $R_4$) to provide an amplifier gain within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits.

It is recommended that the designed gain is near the centre of the calculated range. The graph in Figure 4 is for the calculation of input gain components for an FX631 using a $V_{DD}$ of 3.3 (±0.1) volts.

Use this area to keep a permanent record of your calculated gains and components

## Implementation Notes

### Aliasing

Due to the switched-capacitor filters employed in the FX631, care should be taken, with the chosen external components, to avoid the effects of alias distortion.

Possible Alias Frequencies:
12kHz Mode = 52kHz
16kHz Mode = 69kHz

If these alias frequencies are liable to cause problems and/or interference, it is recommended that anti-alias capacitors are employed across input resistors $R_1$ and $R_4$.

Values of anti-alias capacitors should be chosen so as to provide a highpass cutoff frequency, in conjunction with $R_1$ ($R_4$) of approximately 20kHz to 25kHz (12kHz system) or 25kHz to 30kHz (16kHz system).

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_1}$$

When anti-alias capacitors are used, allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

### Microcircuit Protection

Telephone systems may have high d.c. and a.c. voltages present on the line. If the FX631 is part of a host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within $V_{DD}$ + 0.3V and $V_{SS}$ -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the FX631 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating Temperature ($T_{OP}$): | **FX631DW/P** | -40°C to +85°C |
| Storage temperature range ($T_{ST}$): | **FX631DW/P** | -40°C to +85°C |

## Functional Limits .....

| | Min. | Max. | Unit | |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | 3.0 | 5.5 | V | at 25°C |

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 3.3V $T_{OP}$ = -40 to +85 °C. Audio Level 0dB ref: = 775mVrms. Noise Bandwidth = 50kHz.
Xtal/Clock or 'Clock In' Frequency = 3.579545MHz. 12kHz or 16kHz System Setting.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Current | | - | - | 1.0 | mA |
| Input Logic "1" (High) | | 2.3 | - | - | V |
| Input Logic "0" (Low) | | - | - | 1.0 | V |
| Output Logic "1" (High) | | 2.9 | - | - | V |
| Output Logic "0" (Low) | | - | - | 0.4 | V |
| Xtal/Clock or Clock In Frequency | | 3.558918 | – | 3.589368 | MHz |
| "High" External Clock Pulse Width | | 100 | - | - | ns |
| "Low" External Clock Pulse Width | | 100 | - | - | ns |
| Input Amp | | | | | |
| D.C. Gain | | 60.0 | - | - | dB |
| Bandwidth (-3dB) | | - | 100 | - | Hz |
| Input Impedance | | - | 1.0 | - | MΩ |
| Logic Impedances | | | | | |
| Input (System) | | 0.7 | - | 3.8 | MΩ |
| (Clock In) | | 10.0 | - | - | MΩ |
| Output | | - | 14.0 | 30.0 | kΩ |
| Overall Performance | | | | | |
| 12kHz Detect Bandwidth | 1 | 11.820 | | 12.180 | kHz |
| 12kHz Not-Detect Frequencies (below 12kHz) | 1 | - | - | 11.520 | kHz |
| 12kHz Not-Detect Frequencies (above 12kHz) | 1 | 12.480 | - | - | kHz |
| 16kHz Detect Bandwidth | 1 | 15.760 | | 16.240 | kHz |
| 16kHz Not-Detect Frequencies (below 16kHz) | 1 | - | - | 15.360 | kHz |
| 16kHz Not-Detect Frequencies (above 16kHz) | 1 | 16.640 | - | - | kHz |
| Sensitivity | 2 | 7.8 | 10.0 | 15.5 | mVp-p |
| Tone Operation Characteristics | | | | | |
| Signal-to-Noise Requirements (Amp Input) | 3, 4, 5, 6 | 22.0 | 20.0 | - | dB |
| Signal-to-Voice Requirements (Amp Input) | 3, 4, 5, 7 | -36.0 | -40.0 | - | dB |
| Signal-to-Voice Requirements (Amp Output) | 5, 6 | -25.0 | - | -29.0 | dB |
| Packet Mode Output | | | | | |
| Response and De-Response Times | 1, 8 | - | - | 10.0 | ms |
| Cumulative Tone Follower Output | | | | | |
| Response and De-Response Times | 1, 8 | 40.0 | - | 48.0 | ms |

**Notes .. .. .. .. ..**

## Specification .....

**Notes**

1. With adherence to Signal-to-Voice and Signal-to Noise specifications.
2. With Input Amp gain setting: $15.5dB_{MIN}$/$18.0dB_{MAX}$.
3. Common Mode SPM and balanced voice signal.
4. Immune to false responses.
5. Immune to false de-responses
6. With SPM and voice signal amplitudes balanced; To avoid false de-responses due to saturation, the peak-to-peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
7. Maximum voice frequencies = 3.4kHz
8. Response, De-Response and Power-up Response Timing.

## Application Information .....

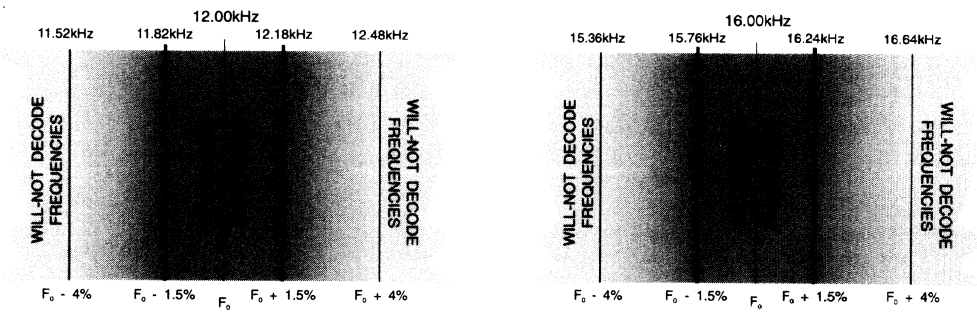



*Fig. 5 Will/Will-Not Decode Frequencies*

## System Timing

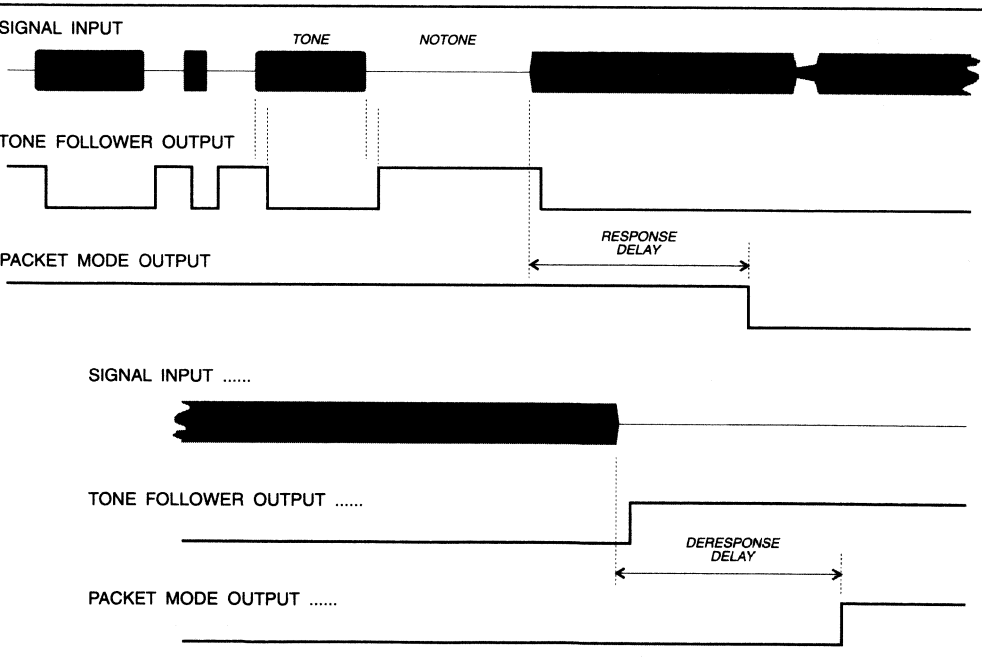



*Fig.6 Examples of Input and Output Relationships*

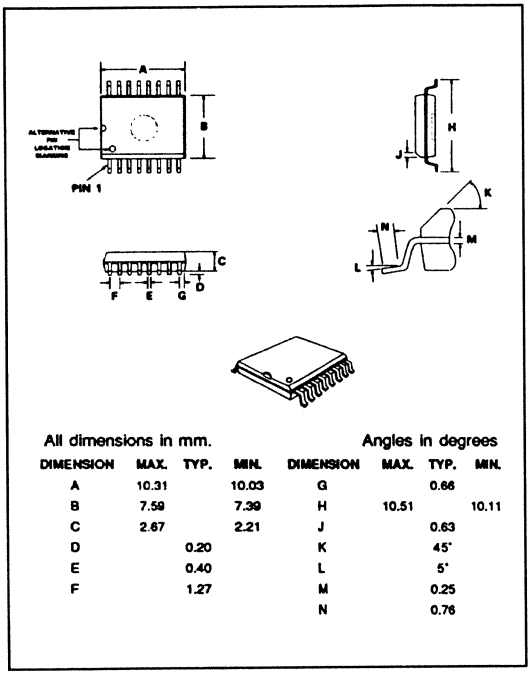
## Package Outlines

The FX631DW, the S.O.I.C. package is shown in Figure 7, the 'P' version in Figure 8.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX631 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

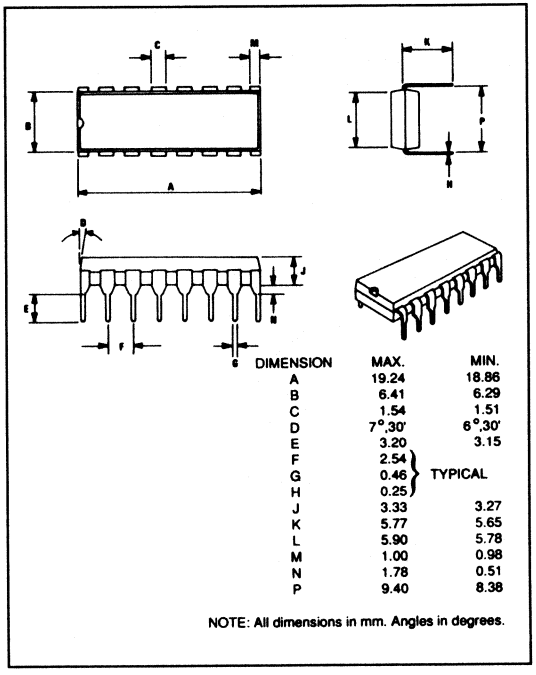
*Fig.7* ***FX631DW*** *S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.31 | | 10.03 | G | | 0.66 | |
| B | 7.59 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.8* ***FX631P*** *plastic Package*




| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.24 | 18.86 |
| B | 6.41 | 6.29 |
| C | 1.54 | 1.51 |
| D | 7°,30' | 6°,30' |
| E | 3.20 | 3.15 |
| F | 2.54 | TYPICAL |
| G | 0.46 | TYPICAL |
| H | 0.25 | TYPICAL |
| J | 3.33 | 3.27 |
| K | 5.77 | 5.65 |
| L | 5.90 | 5.78 |
| M | 1.00 | 0.98 |
| N | 1.78 | 0.51 |
| P | 9.40 | 8.38 |

NOTE: All dimensions in mm. Angles in degrees.

## Ordering Information

**FX631DW** 16-pin surface mount S.O.I.C.

**FX631P** 16-pin plastic DIL

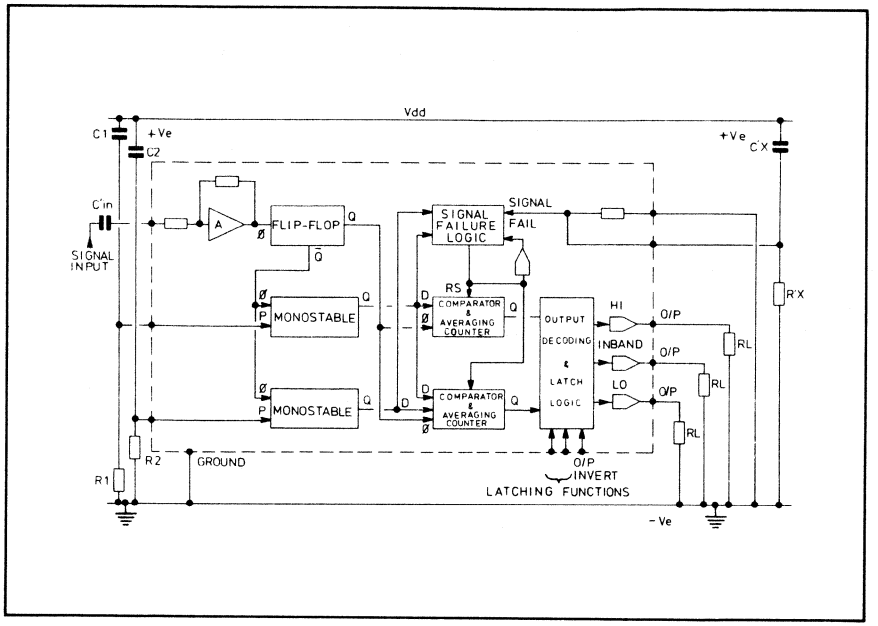
# CML Semiconductor Products

PRODUCT INFORMATION

# FX701P

## Dual Datum Frequency Sensitive Switch

**Publication D/156/2/119**




# FX-701P

## DUAL DATUM FREQUENCY SENSITIVE SWITCH

### GENERAL DESCRIPTION

The FX-701P is a monolithic microcircuit housed in a 14 pin plastic D.I.L. package. It functions as a frequency sensitive switch. Monitoring of a frequency input is made very simple by having HI/IN LIMIT/and LO switch output functions.

The device is purpose designed for analogue frequency monitoring applications, such as remote control and tachometry, where switching operations must be performed when a signal frequency reaches pre-determined levels.

This LSI circuit is the basis of a fully operational sub-system. The only external components required are a few resistors and capacitors which enable the user to programme the switch operating frequencies, hysterisis and signal cutoff fail safe delay.

TYPICAL APPLICATIONS

**PROCESS MONITORING**

**REMOTE SWITCHING**

**TACHOMETRY**

**FREQUENCY ALARMS**

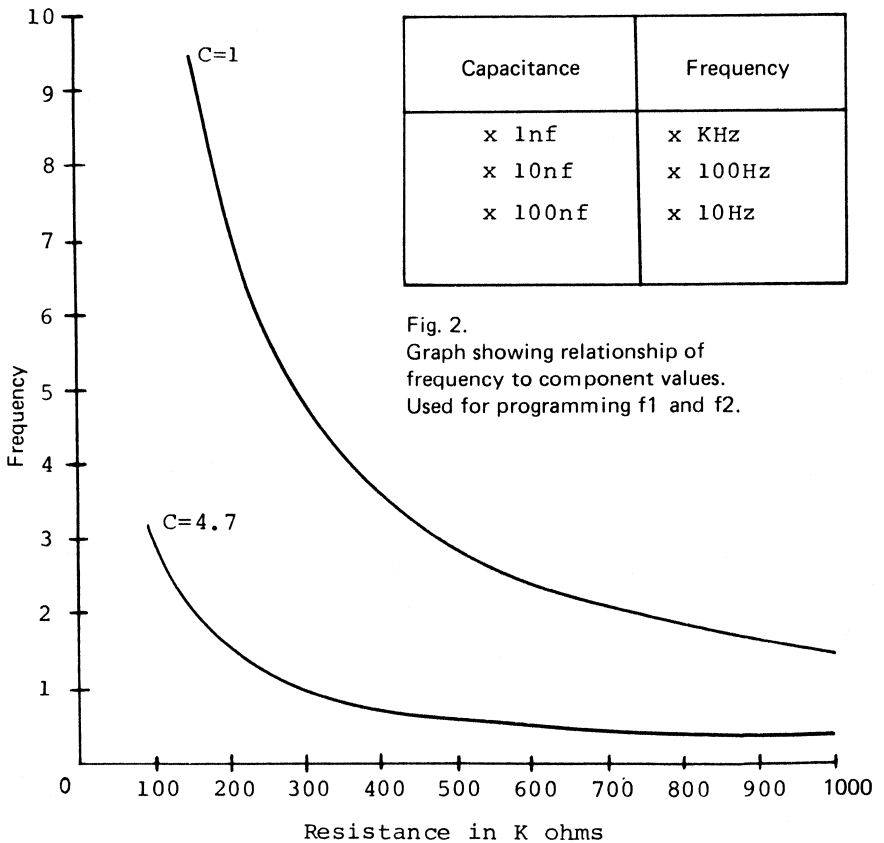
## GENERAL OPERATION

The frequency recognition system employed by the FX-701P, is based on a period sampling technique. Input signals are amplified and shaped to provide clock signals to the bistable flip-flop, the output of which is a square wave having a period equal to the interval between successive input wave form 'zero crossings'. The flip-flop output triggers a dual monostable, which generates reference periods corresponding to set-point f1 and set point f2. These periods are determined by R1/C1 and R2/C2.

The reference periods are compared against the signal input period in two comparators, the outputs of which control a special counter/storage system. This counting system discriminates against random/spurious noise information and delivers an output only when a true set point frequency is received. Gating circuits are incorporated which prevent false operation when harmonics of the set point frequencies are applied.

This frequency discrimination system yields extremely sharp set point definition coupled with a fast response time, and a positive 'chatter-free' switch action. As the device monitors all signals applied, care should be taken to ensure that the input does not include noise signals having a frequency lying above the switch set point levels.

FIG. 2. FREQUENCY CALCULATIONS




| Capacitance | Frequency |
|---|---|
| x 1nf | x KHz |
| x 10nf | x 100Hz |
| x 100nf | x 10Hz |

Fig. 2.
Graph showing relationship of frequency to component values.
Used for programming f1 and f2.

FIG. 3. TRUTH TABLES FX-701P

| CONTROL INPUT | OUTPUT SWITCHES | | |
|---|---|---|---|
| | HI | INBAND | LO |
| PIN 1 | PIN 9 | PIN 10 | PIN 11 |
| 0 | 1 | 1 | 0 * |
| 1 | 0 | 0 | 1 * |

*Showing the active switch for an input signal below $f_2$.

LOGIC 1 = +ve SUPPLY  LOGIC 0 = GROUND

| CONTROL INPUTS | | OUTPUT SWITCH FUNCTIONS |
|---|---|---|
| PIN 13 | PIN 14 | |
| 0 | 0 | LATCH OUTBAND |
| 0 | 1 | LATCH HI |
| 1 | 0 | LATCH LO |
| 1 | 1 | UNLATCHED |

## LATCHING FUNCTIONS

Two latching inputs allow various latching functions to be performed. With both inputs at logic '1' the output switches are 'UNLATCHED' and operate at the relevant set point frequencies, thus reflecting the present value of the signal input frequency. With both inputs at logic '0' 'LATCH OUTBAND' mode, the Hi or Lo output switch will latch if the input signal deviates outside the Inband zone, i.e. over f1 or below f2. Latch Hi mode is obtained by applying a logic '0' to Pin 13 and a logic '1' to Pin 14 this latches the output Hi switch when the signal input lies above f1. Latch Lo mode requires a logic '1' on Pin 13 and a logic '0' on Pin 14 thus latching the signal Lo switch when the signal lies below f2 (see fig. 3).

Once latched, a switch remains in the ON condition regardless of further input signal changes. To unlatch or reset an output switch the signal input must be returned to a non-latch value and a momentary '1' applied to both control pins.

## OUTPUT INVERT

Normally this pin is at a logic '0', if it is pulled to positive the polarity of the three output switches are reversed.

Each control input (pins 1, 13, 14) is provided with an internal pull-down resistor which automatically places a '0' level (–ve) on the pin when the pin is open circuit.

## FREQUENCY CALCULATIONS F1 & F2

Figure 2 illustrates the component values required for setting f1 and f2, f1 should always be set to a higher frequency than f2, if the component values chosen yield f2 to be higher than f1 the inband zone disappears and the output switches change directly from Lo to Hi at the frequency determined by the components used for set point f1. The formula for calculating f1(R1C1) and f2(R2C2) is 1/0.7RC Hz.

## OUTPUT SWITCH CHARACTERISTICS

The standard output switch used in all devices is a MOS driver transistor connected between the output pin and the positive pin. No internal load is provided, therefore the only potentials present at the output pins, are those provided by the external load. Low current loads may be directly connected between the output pin and +ve supply, high current loads should be operated through a buffer transistor.

FIG. 4. TIMING DIAGRAM

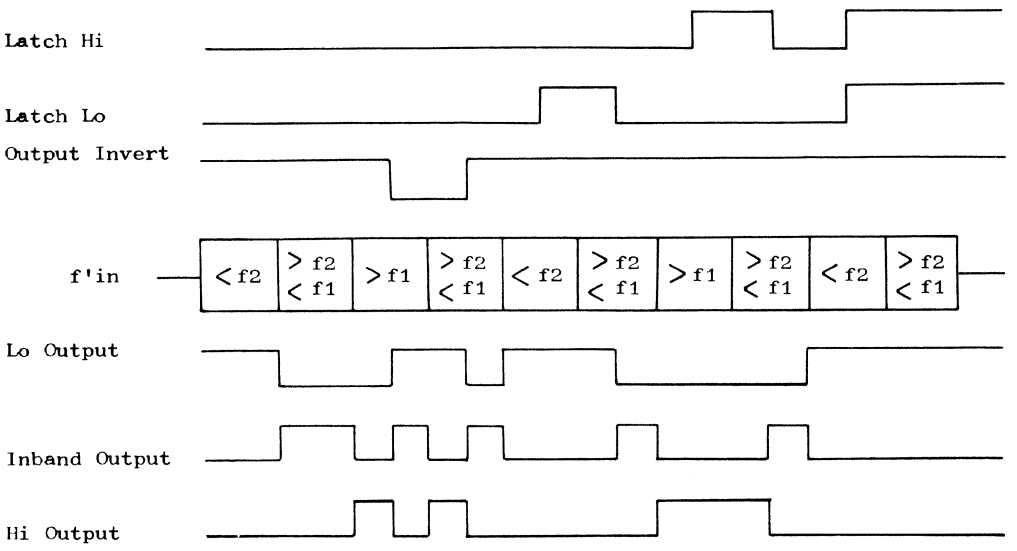



Fig. 4. Timing diagram showing output changes for a typical signal input. Control functions are also shown.

N.B. f1 > f2

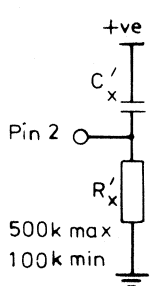
## SIGNAL FAILURE RECOGNITION

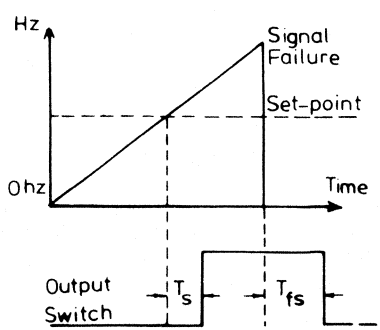
As the FX-701P is essentially a digital device the input circuits come to rest when no input signals are present. If therefore, an instantaneous signal cut-off occurs while the switch is in the Hi state it will remain in this condition until a low frequency input signal is restored. By suitable connection of Pin 2 however, the reaction of the switch to a failure of input signals can be pre-determined according to user requirements.

With Pin 2 directly connected to the positive supply, the switch ignores signal interruptions and will turn ON or OFF only in response to defined input signal frequencies.

FIG. 5. SIGNAL FAILURE RECOGNITION TIME

$T_{fs}$ = 0.6RC Seconds
Where 0.6 is a design constant & subject to production tolerances of ± 10% (0.54 to 0.66)
R = Meg ohms C = Mfd



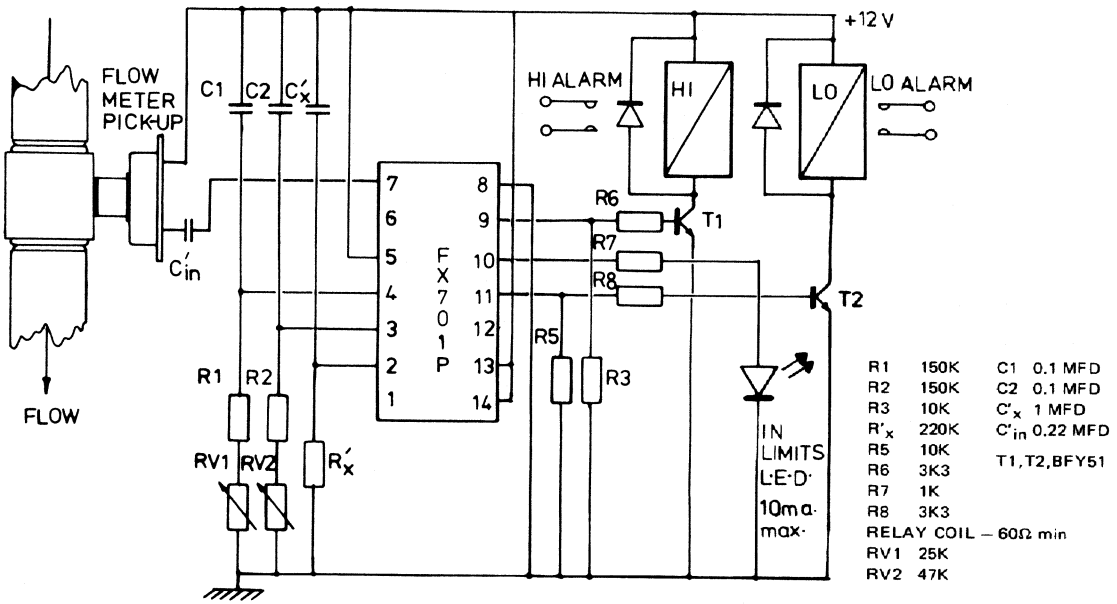

$T_s$ – Response Time
$T_{fs}$ – Signal Failure Time

To obtain automatic switch to Lo should input signals fail, Pin 2 should be connected to CR network C'x/R'x. If the output switch is in the Hi state and signals fail, the capacitor changes to a preset level and forces the output switch to Lo. The capacitor is then automatically discharged. The failure recognition time Tfs can be adjusted to allow phased signal breaks to be ignored, but ensures that the switch adopts the Lo state if a true signal failure occurs.

For general purpose applications a convenient value of Tfs is 10/f2(Hz)seconds, which yields a period Tfs equal to the normal response time Ts. Whilst Tfs can be set to almost any required longer delay time, it should never be made less than 2/f2(Hz) seconds; if it is too short, the interval between successive input signal samples may be mistaken for 'Lo signal' and the switch will be held Lo permanently.

Pin 2 may also be used as a direct reset which switches the outputs to the Lo state, over-riding the input signal. If the pin is open-circuited, the internal pull-up resistor applies a reset voltage to the output switch stages. This resets the switch to Lo state in a maximum time 1/f2(Hz) seconds. Note that the output switch will be permanently Lo if Pin 2 is left open-circuit. See Fig. 5.

FIG. 6. HI/LO/IN-LIMITS FLOWRATE MONITORING




## CIRCUIT APPLICATION

Fig. 6 shows how the FX-701P is used to monitor the state of flow of a fluid in a pipe. By means of a flow rate transducer, a signal of varying frequency is obtained. The circuit then processes this information to indicate when the flowrate is within pre-set limits or whether it is above or below them.

In the example shown, when the frequency from the transducer is between f2 and f1, (80Hz and 90Hz) the IN-LIMITS LED is illuminated. When the frequency rises over f1 the HI alarm relay operates and if it falls below f2 the LO alarm relay operates. Only one output is on at a time and the set point thresholds are very sharp (0.1% differential typical). With pins 13 and 14 connected to the positive rail this gives an unlatched mode of operation. If pin 1 is connected to the positive rail, this causes the outputs to reverse, i.e. the LED is on only for outband signals and both relays operate for any signal between f2 and f1. If there is a signal failure, R'x/C'x ensures that the switches adopt a LO state.

# SPECIFICATIONS

MAX. RATINGS

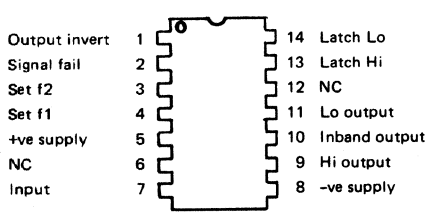
| | |
|---|---|
| Max. voltage between any pin and negative supply | 20V & -0.3V |
| Operating Temperature Range | -10°C to 60°C |
| Storage Temperature Range | -40°C to 85°C |
| Max. Output Switch Load Current | 10mA each switch |
| Max. Device Dissipation at 20°C (T'amb) | 200mW |

CHARACTERISTICS

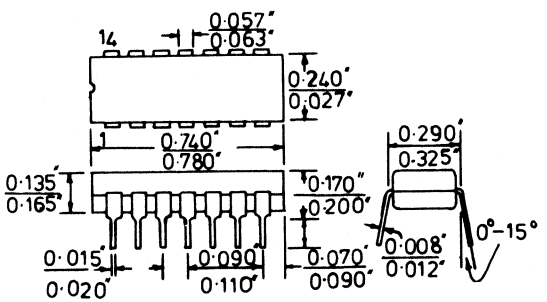
(T'amb = 20°C, Vdd = 12V ±2V, Set Point Frequencies 1Hz to 3KHz (unless specified)

| SYMBOL | PARAMETER | CONDITIONS & NOTES | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Vdd | Supply voltage | Operating range | | 8 | 12 | 15 | V |
| Idd | Supply current | Total excluding switch load current | | | 3.5 | | mA |
| V'in | Signal Amplitude range | Sine or square wave AC coupled | | | 0.1 | 15 | V pk-pk |
| f1/f2 | Adjustment limits | Max & min set point frequencies | | 1Hz | | 10KHz | |
| | Frequency ratio | Permitted ratio adjustment (f2% below f1) | | 1 | | 95 | % |
| Δf | Set point stability | Set point deviation versus supply volts & T'amb. External component coeff excluded | Supply | | 0.05 | 0.08 | %/% |
| | | | T'amb | | 0.005 | 0.02 | %/°C |
| Tr | Response time | Overall switching time following receipt of 'switch' value frequency | | $\frac{8}{f'o}$ | | | Secs. |
| R'on | Switch 'ON' resistance | Internal resistance between output pin and ground switch 'ON' (Switch 'OFF' resistance ⩾ 10M Ω) | | | 0.3 | 1 | KΩ |
| '1' | Logic High | External logic levels to control inputs. (Internal 300KΩ pull-down resistors give logic '0' when open circuit) | '1' | 6 | | 15 | V |
| '0' | Logic Low | | '0' | 0 | | 1.5 | V |

PIN CONNECTIONS




PACKAGE DETAILS: 14 LEAD D·I·L·



# Integrated Circuits Data Book

Section 7

# Paging

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX013 HSC Tone Decoder for 'Pagers

Publication D/013/1 February 1993
Provisional Issue

## Features

- 'N'-Tone HSC Decoding
- EIA and CCIR Tonesets
- 4-Bit Parallel (HEX) Data Output
- µProcessor Interface
- Auxiliary 23.33kHz Clock Output
- Low-Power (2.5V @ 500µA$_{MIN}$) Requirement
- Radiopaging, PMR Selcall and Remote Signalling Applications
- Selectable 560kHz or 4.48MHz Xtal/Clock Operation
- Automatic Power-Up Reset Facility
- 24-Pin/Lead Package Versions

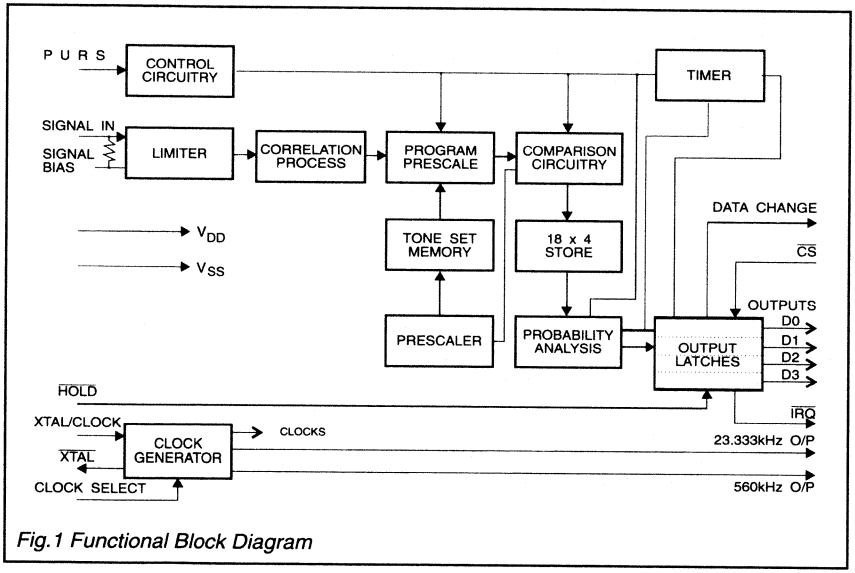



*Fig.1 Functional Block Diagram*

**FX013**

## Brief Description

The FX013 is a very low-voltage continuous "N"-Tone EIA and CCIR HSC tone decoder which is ideal for tone-paging applications.

From an analogue signal input the FX013 will produce a representative 4-bit (HEX) parallel output word for either toneset. Hold, Data Change and Interrupt features combined with the 4-bit data output enable µProcessor interface and control. Alternatively, the FX013 may be used in a simple passive system using the Data Change and Data Outputs

This device can be used with a customer specified µProcessor or with a pre-programmed address decoder/display driver.

The FX013 has on-chip automatic Power-Up Reset circuitry, which with selected time-constant components ensures the correct start-up settings for most supply conditions, making this device ideal for installation within radiopaging units.

Operating at 2.5 volts with a minimum current requirement of 500µA, the FX013 is available in two toneset versions to decode either EIA (A) or CCIR (C) tones.

To cater for variations in design requirements the FX013 is produced in both 24-pin cerdip DIL and plastic quad packages.

| Pin Number FX013J/LG | Function |
|---|---|
| 3 | **Signal In:** HSC input tones are a.c. coupled to this pin; dc bias of the internal high gain limiter is set up by an internal 3MΩ bias resistor connected between this pin and the Signal Bias pin. Neither pin should be loaded with any other circuitry. |
| 5 | **Signal Bias:** See Signal In. |
| 7 | **23.33kHz** Clock **Out:** A 23.333kHz buffered squarewave logic output directly derived from the oscillator frequency (nominally 560.0kHz). This pin may be used for auxiliary functions, e.g. external timing of received tone periods and for other '03 series devices. |
| 8 | $\overline{\text{Xtal}}$: Output from on-chip inverter. |
| 9 | **Xtal/Clock:** Input to on-chip inverter. May be used in conjunction with the $\overline{\text{Xtal}}$ O/P and a 560kHz ceramic resonator/trimming capacitor, or a 4.48MHz Xtal Circuit. May also be used with a buffered input from an externally derived 560kHz or 4.48MHz clock. |
| 10 | **560kHz** Buffered **O/P:** A buffered 560kHz signal is output from this pin. |
| 11 | **Clock** Frequency **Select:** Normally at logic "1" if a 560kHz resonator is being used. If held at logic "0," a divide by 8 function is switched in after the oscillator circuit to divide down the 4.48MHz frequency to 560kHz. This pin has an internal 1MΩ pullup resistor. |
| 12 | $V_{SS}$: Negative Supply (GND). |
| 13 | $\overline{\text{Hold}}$ **I/P:** If taken to $V_{SS}$ and a tone is input, the resulting Data Change output latches to logic "1" and the Data lines output the code for the detected tone regardless of subsequent changes to the input tone, until Hold is returned to $V_{DD}$. This facilitates interrupt/handshake routines for µProcessors when used in conjunction with the Data Change O/P. This pin has an internal 1MΩ pullup resistor. |
| 14 | **Power-Up Reset (P U R S):** To reset internal circuitry on power-up, a logic "1" is required at this pin for a duration of at least 1.0ms after clock is applied. For slow-rising supplies the time constant recommended by the components in Figure 2 should be increased accordingly. |
| 15 | $\overline{\text{IRQ}}$: Interrupt Request. This output, is latched to logic "0" when a tone is detected and the CS pin is at $V_{DD}$, i.e. chip disabled. This pin is reset to logic "1," enabling its for use in wire-ORing with similar outputs from other peripherals. This pin has internal 1kΩ pulldown and 100kΩ pullup resistors on-chip. |
| 16 | $\overline{\text{CS}}$: Chip Select. When this pin is at $V_{DD}$, the chip is disabled and the data outputs D0 - D3 and Data Change output go open circuit. When at $V_{SS}$ the chip is enabled and the IRQ output is reset to logic "1." |
| 17 | **Data Change:** A 1.0 ms pulse is generated at this pin upon detection of a valid tone and new data is presented to the D0 - D3 outputs. The signal from this pin can be latched at a logic "1" after detection of a tone (see Hold input). This output is tri-state. |
| 19<br>20<br>22<br>23 | **D3 Data Outputs:** A 4-bit word, that represents the HEX value of the decoded tone **D2** frequency, is output from these pins after a successful decode. **D1** These outputs are tri-state. See Table 1. **D0** |
| 24 | $V_{DD}$: Positive Supply |
| 1, 2, 4, 6, 18, 21 | Not connected. Leave open-circuit. |

## Application Information

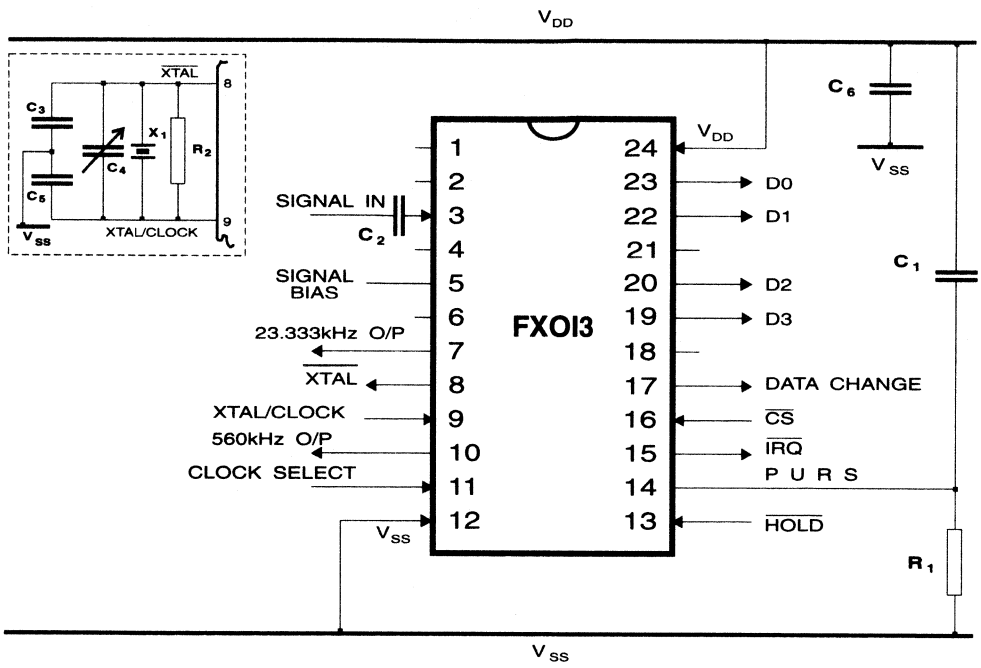



*Fig. 2 Recommended External Components*

| Component | Value | | |
|---|---|---|---|
| $R_1$ | 1MΩ | $C_3$ | 47.0pF |
| $R_2$ | 1MΩ | $C_4$ | 5 - 65pF |
| $C_1$ | 0.01µF | $C_5$ | 47.0pF |
| $C_2$ | 0.001µF | $C_6$ | 1.0µF |
| | | $X_1$ | 560kHz |

*Tolerance: R = ±10% C = ±20%*

| Input Tone Frequencies (Hz) FX013 A (EIA) | FX013 C (CCIR) | Binary Coded Output D3 | D2 | D1 | D0 | Quadradecimal Data Character |
|---|---|---|---|---|---|---|
| 600 | 1981 | 0 | 0 | 0 | 0 | 0 |
| 741 | 1124 | 0 | 0 | 0 | 1 | 1 |
| 882 | 1197 | 0 | 0 | 1 | 0 | 2 |
| 1023 | 1275 | 0 | 0 | 1 | 1 | 3 |
| 1164 | 1358 | 0 | 1 | 0 | 0 | 4 |
| 1305 | 1446 | 0 | 1 | 0 | 1 | 5 |
| 1446 | 1540 | 0 | 1 | 1 | 0 | 6 |
| 1587 | 1640 | 0 | 1 | 1 | 1 | 7 |
| 1728 | 1747 | 1 | 0 | 0 | 0 | 8 |
| 1869 | 1860 | 1 | 0 | 0 | 1 | 9 |
| 2151 | 2400 | 1 | 0 | 1 | 0 | A |
| 2433 | 930 | 1 | 0 | 1 | 1 | B |
| 2010 | 2247 | 1 | 1 | 0 | 0 | C |
| 2292 | 991 | 1 | 1 | 0 | 1 | D |
| 459 | 2110 | 1 | 1 | 1 | 0 | E |
| NOTONE | NOTONE | 1 | 1 | 1 | 1 | F |

*Table 1 Decode Frequency Tonesets*

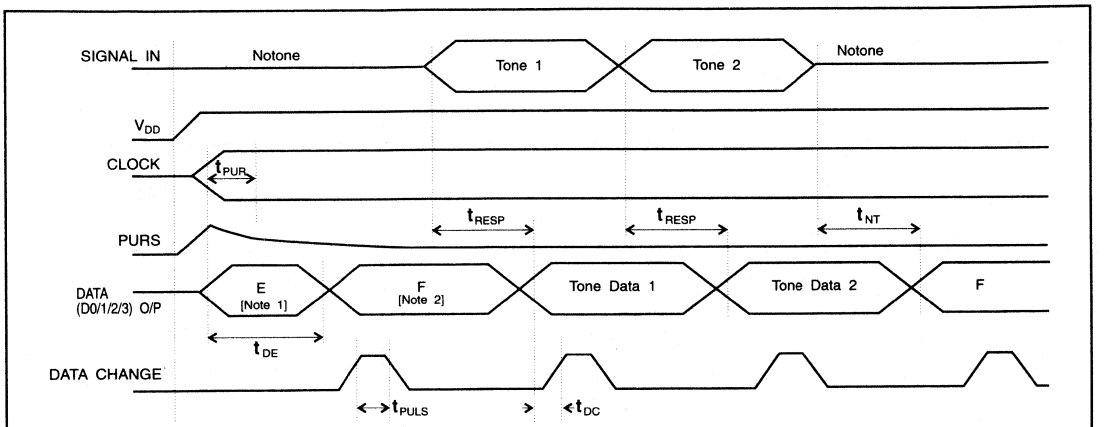



*Fig.3 Normal Timing Operation [not to scale]*

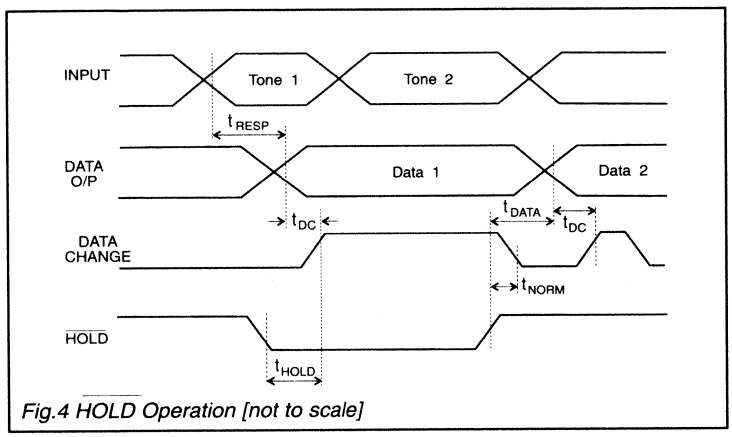



*Fig.4 $\overline{HOLD}$ Operation [not to scale]*

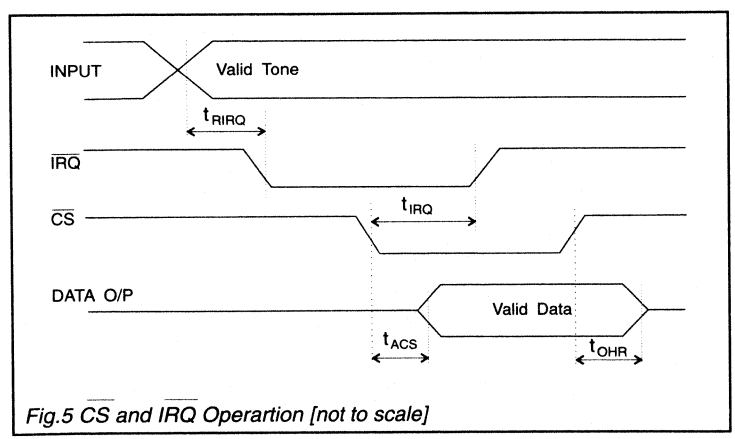



*Fig.5 $\overline{CS}$ and $\overline{IRQ}$ Operartion [not to scale]*

## Timing Specification

| | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $t_{PUR}$ | 2.0 | - | - | ms |
| $t_{DE}$ | - | 33.0 | - | ms |
| $t_{PULS}$ | - | 1.0 | - | ms |
| $t_{DC}$ | 0.5 | - | 1.0 | ms |
| $t_{RESP}$ | 20.0 | - | 33.0 | ms |
| $t_{NT}$ | 33.0 | - | 53.0 | ms |
| $t_{DATA}$ | - | - | 2.0 | ms |
| $t_{NORM}$ | - | - | 120 | µs |
| $t_{HOLD}$ | 50.0 | - | - | µs |
| $t_{IRQ}$ | - | - | 250 | ns |
| $t_{RIRQ}$ | 20.5 | - | 34.0 | ms |
| $t_{ACS}$ | - | - | 250 | ns |
| $t_{OHR}$ | - | - | 100 | ns |

Notes:

1. 'E' is the start-up (power-up reset) condition.
2. The state of D0/1/2/3 will represent the input frequency present during and after Power-Up Reset (F [NOTONE] in the Figure 3 example).

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating Temperature ($T_{OP}$): | **FX013J/LG** | -40°C to +85°C |
| Storage temperature range ($T_{ST}$): | **FX013J/LG** | -55°C to +125°C |

| **Functional Limits .....** | **Min.** | **Max.** | **Unit** | |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | 2.5 | 5.5 | V | at 25°C |

All device characteristics are measured under the following conditions unless otherwise specified:
$V_{DD}$ = 5.0V $T_{OP}$ = -40 to +85 °C. Xtal/Clock or 'Clock In' Frequency = 560kHz.

| **Characteristics** | **See Note** | **Min.** | **Typ.** | **Max.** | **Unit** |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| **Supply Voltage** ($V_{SS}$=0V) | | 2.5 | - | 5.5 | V |
| **Supply Current** | | - | 500 | - | µA |
| Logic "1" Output (Source = 1 mA) | 1 | 4.5 | - | - | V |
| Logic "0" Output (Sink = 1 mA) | 1 | - | - | 0.5 | V |
| Logic "1" Input Level | 2 | 3.5 | - | - | V |
| Logic "0" Input Level | 2 | - | - | 1.5 | V |
| Oscillator Output Level | | | | | |
| **Input Impedances** | | | | | |
| Signal In | | - | 1.0 | - | MΩ |
| Clock Select | | - | 1.0 | - | MΩ |
| Hold I/P | | - | 1.0 | - | MΩ |
| Chip Select | | - | 10.0 | - | MΩ |
| **Output Impedances** | | | | | |
| D0 - D3 | | - | 1.0 | - | kΩ |
| Data Change | | - | 1.0 | - | kΩ |
| Oscillator Outputs | | - | 10.0 | - | kΩ |
| **Dynamic Values** | | | | | |
| **Signal Input Range** | 3 | 35.0 | - | $V_{DD}$/2 | mVrms |
| **Decode Bandwidth** when P>0.995 | | | | | |
| QA | 4 | ±20.0 | - | - | Hz |
| QC | 4 | ±1.0 | - | - | % |
| **Not-Decode Bandwidth** when P<0.03 | | | | | |
| QA | 5 | - | - | ±60.0 | Hz |
| QC | 5 | - | - | ±3.0 | % |
| **Noise Response Rate** (hours per F - F : F single character response with no input tone). | | | | | |
| QA | 6 | - | 0.15 | - | /hour |
| QC | 6 | - | 40.0 | - | /hour |
| **Decode Response Time:** | | | | | |
| NOTONE to Tone (F - F) | 7 | 20.0 | 25.0 | 33.0 | ms |
| Tone to NOTONE, Tf (F - F) | 7 | 33.0 | - | 53.0 | ms |
| Minimum inter-tone gap for "F" | 8 | 15.0 | - | 28.0 | ms |

**Notes:**

1. Pins 7, 8, 17 and 19, 20, 22 and 23.
2. Pins 13,14 and 16.
3. An ac coupled sine/squarewave.
4. With minimum tone period (Tp) specified for toneset. P = Decode Probability. (QA) SNR = 3dB. (QC) SNR = 0dB.
5. All conditions of input SNR and amplitude with maximum Tp specified for the toneset.
6. Gaussian input noise, bandwidth 6.0kHz, maximum input level corresponds to 1-digit code falsing rate. F = random single character.
7. Delay from change of input (tone applied/removed) to change at Q0-Q3 outputs.
8. Included in $t_{NT}$. Minimum tone gap requirement for "NOTONE" recognition. Outputs = F after delay.

## Package Outlines

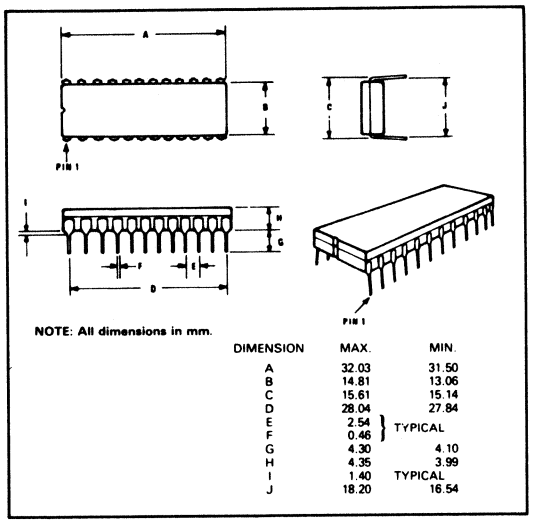
The FX013J, the cerdip package is shown in Figure 6 and the 'LG' quad plastic version in Figure 7.

Pin 1 identification marking is shown on the relevant diagram and pins on both package styles number anti-clockwise when viewed from the top (marked side).

## Handling Precautions

The FX013 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

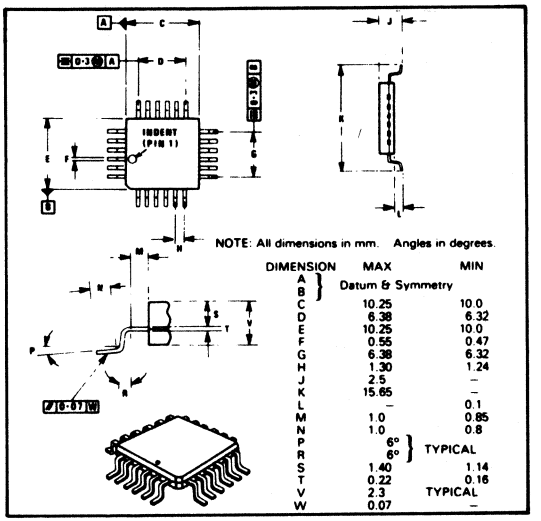
*Fig.6* ***FX013J 24-pin cerdip Package***




NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 32.03 | 31.50 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 } | TYPICAL |
| F | 0.46 } | |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 | TYPICAL |
| J | 18.20 | 16.54 |

*Fig.7* ***FX013LG quad plastic Package***




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A } | Datum & Symmetry | |
| B } | | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° } | TYPICAL |
| R | 6° } | |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

## Ordering Information

The FX013 is available in two tonesets and two package styles: 'A' = EIA Tones
'C' = CCIR Tones
Please order the correct toneset in the correct package.

**FX013J 'A' / 'C'**
24-pin cerdip DIL

**FX013LG 'A' / 'C'**
24-pin plastic encapsulated bent and cropped

# Integrated Circuits Data Book

Section 8

# Modems for Radio and Data Comms

## CML Modem Guide ..... .....

| Modem Type | Baud Rate | Duplex | C. Detect Available On Chip | µP Interface | Powersave Modes | Xtal (MHz) | Protocols Standards | Additional Features | Page No |
|---|---|---|---|---|---|---|---|---|---|
| **FX439** | 1200 FFSK | FULL | YES | NO | YES FULL 650µA typ. | 4,032 or 1,008 | Gen. Data Trunked Radio Band III ZVEI/BOS/R2000 NMT 450/900 | On-Chip Rx and TX Bandpass Filters<br>On-Chip Clock Recovery<br>Pin-Selectable Xtal/Clock Frequencies | 8-23 |
| **FX429** | 1200 FFSK | FULL | YES | 8-bit PARALLEL | YES FULL 1.0mA typ | 4,032 | Trunked Radio Band III MPT 1317/1327 | High Intelligence<br>Error Checking in Receive<br>Error Check Word Generation<br>Frame SYNC/SYNT Detection | 8-3 |
| **FX529** | 1200 FFSK | FULL | YES | 8-bit PARALLEL | YES FULL 1.0mA typ. | 4,032 | Trunked Radio PAA 1382 ETSI/EBSS 1200 | High Intelligence<br>Error Checking in Receive<br>Error Check Word Generation<br>Frame SYNC/SYNT Detection<br>Pin/Function Compatible with FX429 | 8-17 |
| **FX809** | 1200 FFSK | HALF | NO | SERIAL "C-BUS" | YES FULL 2.0mA typ. | 4,032 | Universal Trunked Radio Modem | High Intelligence<br>Software Selectable Checksum Generation<br>Error Checking iaw MPT 1327<br>Uncommitted Amplifier<br>Programmable SYNC/SYNT Word | 2-145 |
| **FX469** | 1200 or 2400 (4800) FFSK | FULL | YES | NO | YES FULL 650µA typ. | 4,032 or 1,008 | Gen. Data Trunked Radio Band III ZVEI/BOS/R2000 NMT 450/900 | On-Chip Rx and TX Bandpass Filters<br>On-Chip Clock Recovery<br>Pin-Selectable Xtal/Clock Frequencies<br>Pin/Function compatible with FX439 | 8-29 |
| **FX489** | 4 to 19.2 (kbps) GMSK | FULL | NO | NO | YES FULL 1.0mA typ. | 4.096<br>4.9152<br>2.048<br>2.4576 | High-Speed Data RAM-Mobitex Universal Data Functions | Rx and Tx Data Clock Generation<br>Serial Rx and Tx Data Interfaces<br>Selectable BT (0.3 or 0.5) | 8-37 |
| **FX589** | **New High-Speed/Low-Voltage (40kbps) GMSK Modem** | | | | | | Pin/Function Compatible with FX489<br>4 to 40kbps (5 Volt Operation)<br>4 to 20kbps (3 Volt Operation) | | See FX489 |

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX429 Band III FFSK Modem for Trunked Radio Systems

Publication D/429/5 February 1993
Provisional Issue

## Features/Applications

- Band III and General Purpose Trunked Radio Applications
- Full-Duplex 1200 Baud Operation
- High Intelligence
- Error Checking in Receive
- Error Check Word Generation
- Frame SYNC and SYNT Detection
- Preamble Generation
- µProcessor Compatible Interface
- Carrier Detection On-Chip
- Low Power Consumption
- General Purpose Timer

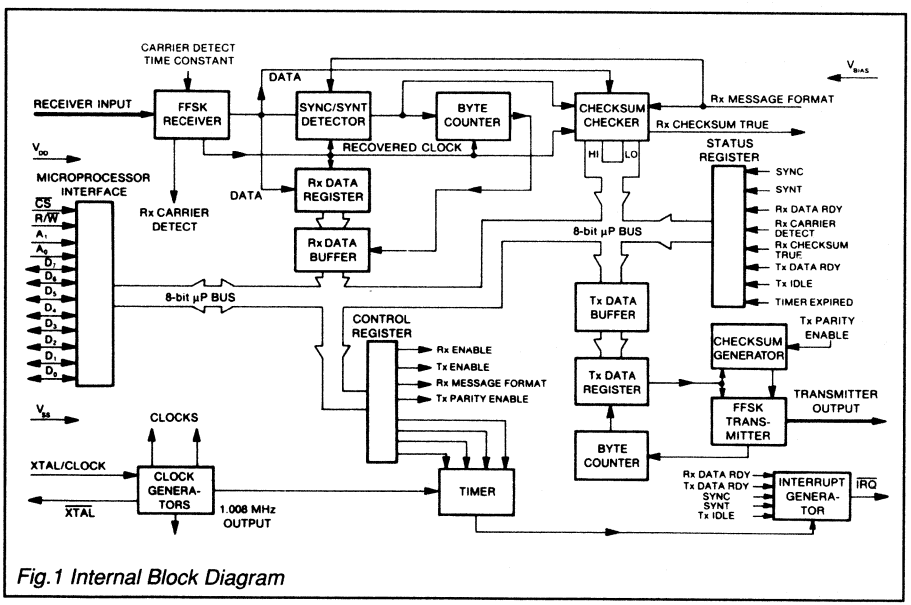



*Fig.1 Internal Block Diagram*

FX429

## Brief Description

The FX429 is a single-chip CMOS 1200 baud FFSK Modem, designed primarily for use in trunked radio systems but may also be employed in other general purpose radio or line data communication applications.

The device has been designed to conform to the UK Band III trunked radio protocols MPT 1317/1327.

The FX429 is full duplex at 1200 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of 8 to 120 bits.

Preamble and an error-check word are automatically generated in the transmit mode.

Error checking is performed and the 16-bit SYNC or SYNT words are detected in the receive mode.

An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides all microcircuit filter sampling clocks and modem timings whilst also supplying a "Clock ÷ 4" output (1.008MHz).

The FX429, which has a powersaving facility, requires a single 5-volt power supply and is available in both cerdip DIL and plastic SMD packages.

| Pin Number DIL FX429J | Pin Number Quad FX429LG/LS | Function |
|---|---|---|
| 1 | 1 | **$V_{BIAS}$ :** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to $V_{SS}$ by capacitor $C_4$, see Figure 3. **Warning Note** – In order to reduce current consumption, the potential at this pin is lowered to $V_{SS}$ when both Tx and Rx are disabled. |
| 2 | 2 | **Transmit Output :** The 1200 baud, 1200Hz/1800Hz FFSK Tx output. When not enabled by the Control Register ( $D_0$) its output impedance is set high. |
| 3 | 4 | **Receiver Input :** The 1200 baud received FFSK signal input. The 1200Hz/1800Hz audio to this pin must be a.c. coupled via capacitor $C_3$, see Figure 3. |
| 5 | 5 | **$V_{DD}$ :** Positive Supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to $V_{SS}$ by capacitor $C_6$, see Figure 3. |
| 6 | 6 | **Carrier Detect Time Constant :** The on-chip Carrier Detect integration function requires two external components on this pin. A capacitor, $C_5$, to $V_{SS}$, together with a resistor, $R_2$, to $V_{DD}$. See Figure 3. |
| 7 | 7 | **Xtal/Clock :** The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here. See Figure 3. |
| 8 | 8 | **$\overline{\text{Xtal}}$ :** The output of the 4.032 MHz clock oscillator. |
| 9 | 9 | **$D_0$ :** **Microprocessor Data Interface** |
| 10 | 10 | **$D_1$ :** |
| 11 | 11 | **$D_2$ :** |
| 12 | 12 | **$D_3$ :** These 8 lines are used by the device to communicate with a microprocessor |
| 13 | 13 | **$D_4$ :** with the $A_2$, $A_0$ and $A_1$ inputs determining register selection. |
| 14 | 14 | **$D_5$ :** |
| 15 | 15 | **$D_6$ :** |
| 16 | 16 | **$D_7$ :** |
| 17 | 17 | **$A_0$ : Register Selection.** These inputs, with the $A_2$ input, select the required register to |
| 18 | 18 | **$A_1$ :** the data bus as shown in Table 1 (below). |
| 19 | 19 | **$\overline{\text{Strobe}}$ :** Performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating high-order address bits with a read/write clock. The FX429 is selected when Strobe = logic "0." See Figure 5. |
| 20 | 20 | **$A_2$ :** Used in conjunction with $A_1$ and $A_0$ to determine which internal registers are connected to the data interface pins ($D_0$ – $D_7$) during $\overline{\text{Strobe}}$ (see Table 1 and Figure 5). |
| 21 | 21 | **$\overline{\text{IRQ}}$ :** Interrupt Request. This line will go to a logic '0' when an interrupt occurs. This output can be "wire OR'd" with other active low components (100kΩ pullup to $V_{DD}$). The conditions that cause the interrupts are indicated at the Status Register and are as follows: *Timer Expired*, *Rx Data Ready*, *Tx Data Ready*, *Tx Idle*, *Rx SYNC Detect*, *Rx SYNT Detect* |
| 23 | 22 | **$V_{SS}$ :** Negative Supply (GND). |
| 24 | 23 | **Clock ÷ 4 :** A 1.008 MHz ($X_1 \div 4$) clock is available at this output for external circuit use, note the source impedance and source current limits. |
| 4, 22 | 3, 24 | These pins are not connected internally, leave open circuit. |

**Table 1**

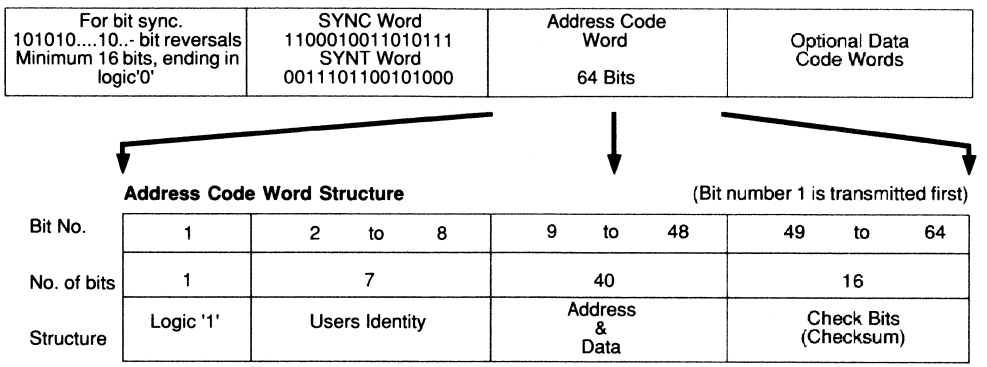
| Register | $A_2$ | $A_0$ | $A_1$ |
|---|---|---|---|
| Control | 0 | 1 | 1 |
| Status | 1 | 1 | 1 |
| Rx Data | 1 | 0 | 1 |
| Tx Data | 0 | 0 | 1 |
| Syndrome Low | 1 | 0 | 0 |
| Syndrome High | 1 | 1 | 0 |

# Modems in Mobile Data Signalling ..... An Introduction

## Digital Code Format

The recommended Digital Code Format for use over Land Mobile Radio Systems is detailed in the Department of Trade and Industry, Radio Regulatory Division's publications MPT 1317 and MPT 1327, and is as described briefly below.

*Fig. 2 The Data stream – Rx and Tx at 1200baud, the minimum, overall transmission length is 96 bits.*




## Operation

The FX429 can be used for Full-Duplex operation with the host microprocessor only having to operate on the data whilst the modem (FX429) handles all other signalling routines and requirements.

In the **Tx** mode the FX429 will :-

(1) Internally generate and transmit a preamble – bit reversals, for system bit synchronization.
(2) Accept from the host, and transmit, a 16-bit 'SYNC' or 'SYNT' word.
(3) Accept from the host, and transmit, 6 bytes of data (Address Code Word).
(a) Upon a software command, internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes.
– or –
(b) Upon a software command, disable internal checksum generation and allow continuous data transmission.
(4) Transmit 1 'hang bit' and go idle when all loaded data traffic has been sent (followed by a "Tx Idle" interrupt).

In the **Rx** mode the FX429 will :-

(1) Detect and achieve bit synchronization within 16 bits.
(2) Search for and detect the 16-bit 'SYNC'/'SYNT' word.
(3) Output all received data after 'SYNC/SYNT,' in byte form.
(4) Upon a software command (Rx Message Format), use the received checksum to calculate the presence (if any) of errors, and advise the host with an interrupt and a 16-bit Syndrome word.

**Note** – In Rx a software command is used to determine whether a 'SYNC'/'SYNT' word is required after every 8 (6 data + 2 checksum ) received bytes, or "data" is received continually.
Normally the 'SYNC' word is used on the Control data channel and the 'SYNT' word is used on the Traffic data channel.

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## Non MPT Application – Full-Duplex

The functions described in this section, to allow the FX429 modem to operate as a general purpose device, are obtained using the commands and indications detailed in the "Register Instructions" pages.

**Tx** – When enabled the device transmits a "101010.....10" preamble until data for transmission is loaded by the host microprocessor.
Transmits 6 bytes of the loaded data followed by a 2-byte checksum based on that data. As long as Tx data is loaded the transmitter will transmit, the 2-byte checksum being produced after every 6 bytes (8 byte packages).
Automatic checksum generation can be inhibited by a software command to allow transmission of continuous data streams.

**Rx** – When enabled requires the16-bit SYNC or SYNT word (see notes) before outputting data bytes. The modem receiver will then output continuous bytes of data, after every 6 bytes received a 2-byte checksum word will be output and can be ignored or used for error checking.

## Control Register $A_1 = 1$ $A_0 = 1$ $A_2 = 0$ Write Only

The Control Register, when selected, directs the modem's operation as described below.

| Bit | Description | Function | Set = logic '1' (High) Clear = logic '0' (Low) |
|---|---|---|---|
| **Bit 0** $D_0$ | **Tx Enable *** | **Set** – $D_0$ enables the transmitter for operation. A '0 – 1' transition causes bit synchronization and the start of 1010.....10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the Tx Data Buffer before one byte has been sent then that data will follow, otherwise whole bytes of preamble will continue until data is loaded. **Clear** – The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced. | |
| **Bit 1** $D_1$ | **Tx Parity Enable** | **Set** – $D_1$ indicates to the transmitter that 2–byte checksums are to be generated by the modem. A '0 – 1' transition starts checksum generation on the next six bytes loaded from the Tx Data Buffer into the Tx Data Register. Checksum generation continues for every 6 bytes loaded until this bit is cleared. The transmitter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded checksum generation will abort, the transmission will cease after one 'hang' bit has been sent and Bit 4 in the Status Register (Tx Idle) will be set. No checksum will be transmitted. **Clear** – No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written". | |
| **Bit 2** $D_2$ | **Rx Enable *** | **Set** – $D_2$ enables the receiver for operation. No data is produced (i.e. No Rx Data Ready interrupts) until a 'SYNC' or 'SYNT' word is found in the received bit stream. **Clear** – The receiver is disabled and all interrupts caused by the receiver are inhibited. | |
| **Bit 3** $D_3$ | **Rx Message Format** | **Set** – $D_3$ is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If 'set' the receiver will assume that the next 6 bytes are data and will start error checking accordingly. **Clear** – The receiver will stop data transfer to the host after the 2 checksum bytes until another 'SYNC' or 'SYNT' frame word is received. | |
| **Bit 4** $D_4$ | **Timer LSB** | These four bits control the timer as follows :- | |
| **Bit 5** $D_5$ | **Timer** | | |
| **Bit 6** $D_6$ | **Timer** | | |
| **Bit 7** $D_7$ | **Timer MSB** | | |

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Reset counter and disable timer interrupts | |
| 0 | 0 | 0 | 1 | Count and interrupt every - | 8 bits |
| 0 | 0 | 1 | 0 | " " " | 16 bits |
| 0 | 0 | 1 | 1 | " " " | 24 bits |
| 0 | 1 | 0 | 0 | " " " | 32 bits |
| 0 | 1 | 0 | 1 | " " " | 40 bits |
| 0 | 1 | 1 | 0 | " " " | 48 bits |
| 0 | 1 | 1 | 1 | " " " | 56 bits |
| 1 | 0 | 0 | 0 | " " " | 64 bits |
| 1 | 0 | 0 | 1 | " " " | 72 bits |
| 1 | 0 | 1 | 0 | " " " | 80 bits |
| 1 | 0 | 1 | 1 | " " " | 88 bits |
| 1 | 1 | 0 | 0 | " " " | 96 bits |
| 1 | 1 | 0 | 1 | " " " | 104 bits |
| 1 | 1 | 1 | 0 | " " " | 112 bits |
| 1 | 1 | 1 | 1 | " " " | 120 bits |

If a new timer value is written to these inputs within 1 byte period of the last timer interrupt then the next timer period will be correct without first having to reset the timer, otherwise the timer must be reset to zero and then set to the new time.

***Note* –**

**Enabling Times**

*The time taken to enable one section (receiver or transmitter) when both sections are initially disabled is 16 bit periods. If one section (receiver or transmitter) is already enabled this time is reduced to "one-half" of a bit period.*

**Tx Enable**

*If using the internal Tx Preamble generation facility, e.g. with the internal timer setting the preamble length, the device may occasionally produce a Tx Data Ready interrupt immediately after a Tx Enable command. User software should handle this occurrence by either:*

*(a) Detecting that the Timer interrupt Status Bit is not set and that it is not appropriate to load Tx data at this time. or,*

*(b) Not using the Timer. i.e. immediately after Tx enable, reading the Status Register and loading a byte of preamble. This resets any interrupt. The length of preamble transmitted is now controlled by the number of bytes loaded.*

## Status Register $A_1 = 1$ $A_0 = 1$ $A_2 = 1$ Read Only

When an interrupt is generated the $\overline{IRQ}$ Output goes Low with the Status Register bits indicating the sources of the interrupt.

| Bit | Description | Function | Set = logic '1' (High) Clear = logic '0' (Low) |
|---|---|---|---|
| **Bit 0** $D_0$ | **Rx Data Ready** | $D_0$ when set, causes an interrupt indicating that received data is ready to be read from the Rx Data Buffer. This data must be read within 8 bit periods. **Set** – when a byte of data is loaded into the Rx Data Buffer, if a frame (SYNC/SYNT) word has been received. **Bit and Interrupt Cleared** – (i) by a read of the Status Register followed by a read of the Rx Data Buffer or (ii) by Rx Enable going Low. | |
| **Bit 1** $D_1$ | **Rx Checksum True** | $D_1$ when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the Rx Data Ready bit ($D_0$) is set for the second byte of the received checksum, does not cause an interrupt. **Set** – by a correct comparison between the received and generated checksums. **Cleared** – (i) by a read of the Status Register followed by a read of the Rx Data Buffer, or (ii) by Rx Enable going Low. | |
| **Bit 2** $D_2$ | **Rx Carrier Detect** | $D_2$ is a " Real Time " indication from the modem receiver's carrier detect circuit and does not cause an interrupt. When FFSK tones are present at the receiver input this bit goes High, for no FFSK input this bit goes Low. When the Rx Enable bit ($D_2$– Control Register) is Low Rx Carrier Detect will go Low. | |
| **Bit 3** $D_3$ | **Tx Data Ready** | $D_3$ when set, causes an interrupt to indicate that a byte of data should be written to the Tx Data Buffer within 8 bit periods. **Set** – (i) when the contents of the Tx Data Buffer are transferred to the Tx Data Register, or (ii) when the Tx Enable is set – No interrupt is generated in this case. **Bit Cleared** – (i) by a read of the Status Register followed by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. **Interrupt Cleared** – (i) by a read of the Status Register, or (ii) by Tx Enable going Low. | |
| **Bit 4** $D_4$ | **Tx Idle** | $D_4$ causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. **Set** – one bit period after the last byte is transmitted. This last byte could be either "checksum" or " loaded data" depending upon the Tx Parity Enable state (Control Register $D_1$). **Bit Cleared** – (i) by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. **Interrupt Cleared** – (i) by a read of the Status Register, or (ii) by Tx Enable going Low. | |
| **Bit 5** $D_5$ | **Timer Interrupt** | $D_5$, when set, causes an interrupt to indicate that the set timer period has expired. (Control Register $D_4$ — $D_7$). **Set** – by the timer. **Bit and Interrupt Cleared** – by a read of the Status Register. | |
| **Bit 6** $D_6$ | **Rx SYNC Detect** * | $D_6$, when set, causes an interrupt to indicate that a 16-bit 'SYNC' word (1100010011010111) has been detected in the received bit stream. **Set** – on receipt of the 16th bit of a 'SYNC' word. **Bit and Interrupt Cleared** – (i) By a read of the Status Register, or (ii) by Rx Enable going Low. | |
| **Bit 7** $D_7$ | **Rx SYNT Detect** * | $D_7$, when set, causes an interrupt to indicate that a 16-bit 'SYNT' word (0011101100101000 ) has been detected in the received bit stream. **Set** – on receipt of the 16th bit of a 'SYNT' word. **Bit and Interrupt Cleared** – (i) By a read of the Status Register, or (ii) by Rx Enable going Low. | |
| ***Note** – | | *'SYNC' and 'SYNT' Detection is disabled whilst the checksum checker is running.* | |

## Rx Data Buffer — $A_1 = 1$ — $A_0 = 0$ — $A_2 = 1$ — Read Only

These 8 bits are the last byte of data received with bit 7 being received first. *Note the relative positions of the **MSB** and **LSB** presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.*

| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
|---|---|---|---|---|---|---|---|
| LSB | - | - | - | - | - | - | MSB |

## Tx Data Buffer — $A_1 = 1$ — $A_0 = 0$ — $A_2 = 0$ — Write Only

These 8 bits loaded to the Tx Data Buffer are the next byte of data that will be transmitted, with bit 7 being transmitted first. *Note the relative positions of the **MSB** and **LSB** presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.* If the the Tx Parity Enable bit (Control Register $D_1$ ) is set, a 2–byte checksum will be inserted and transmitted by the modem after every 6 transmitted " message " bytes.

| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
|---|---|---|---|---|---|---|---|
| LSB | - | - | - | - | - | - | MSB |

# The Syndrome Word

This 16-bit word (both **Low** and **High** bytes) may be used to correct errors.
Bits $S_1$ to $S_{15}$ are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of " received message." For a correct message all 15 bits ($S_1$ to $S_{15}$) will be zero.
The 2 Syndrome bytes are valid when the Rx Data Ready bit (Status Register $D_0$) is set for the second byte of the receivedchecksum and should be read, if required, before 8 byte periods.

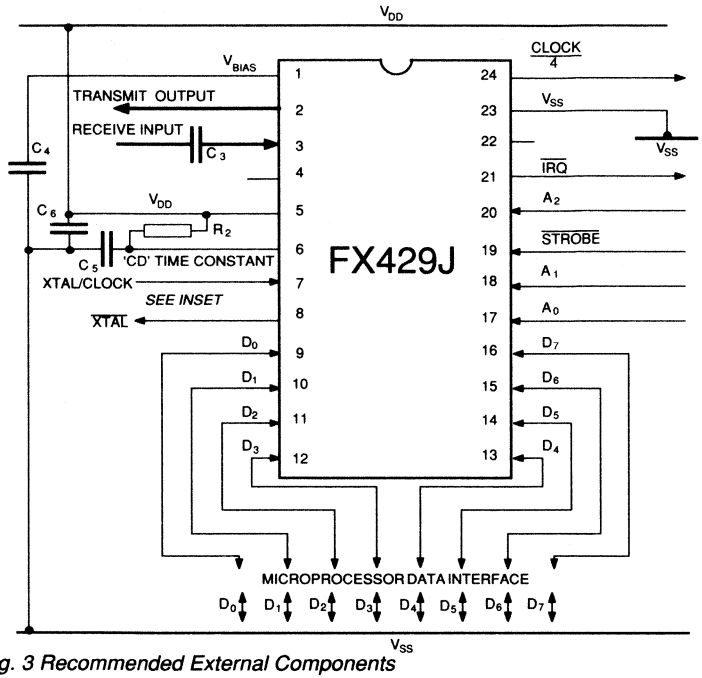
## Syndrome Low Byte — $A_1 = 0$ — $A_0 = 0$ — $A_2 = 1$ — Read Only

| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
|---|---|---|---|---|---|---|---|
| S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |

## Syndrome High Byte — $A_1 = 0$ — $A_0 = 1$ — $A_2 = 1$ — Read Only

| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
|---|---|---|---|---|---|---|---|
| S9 | S10 | S11 | S12 | S13 | S14 | S15 | PARITY ERROR |

$D_7$ – This is a "Parity Error Bit" – Indicating an error between the received parity bit and the parity bit internally generated from the incoming message. Thus for a correctly received message all 16 bits of the Syndrome Word ($S_1$ to $S_{15}$ and Parity Error) will be zero.




**Component References**

| Component | Unit Value |
|---|---|
| $R_1$ | 1.0M |
| $R_2$ | 1.0M |
| $C_1$ | 33p |
| $C_2$ | 33p |
| $C_3$ | 0.1µ |
| $C_4$ | 1.0µ |
| $C_5$ | 1.0µ |
| $C_6$ | 1.0µ |
| $X_1$ | 4.032MHz |

Tolerances. Resistors ± 10%
Capacitors ± 20%

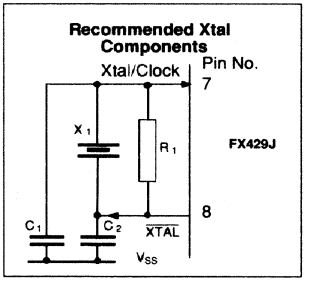



*Fig. 3 Recommended External Components*

### Carrier Detect Time Constant

The value of the Carrier Detect capacitor, $C_5$, determines the carrier detect time constant. A long time constant (larger value $C_5$), results in improved noise immunity but increased response time. $C_5$ may be varied to optimise noise immunity/ reponse time.

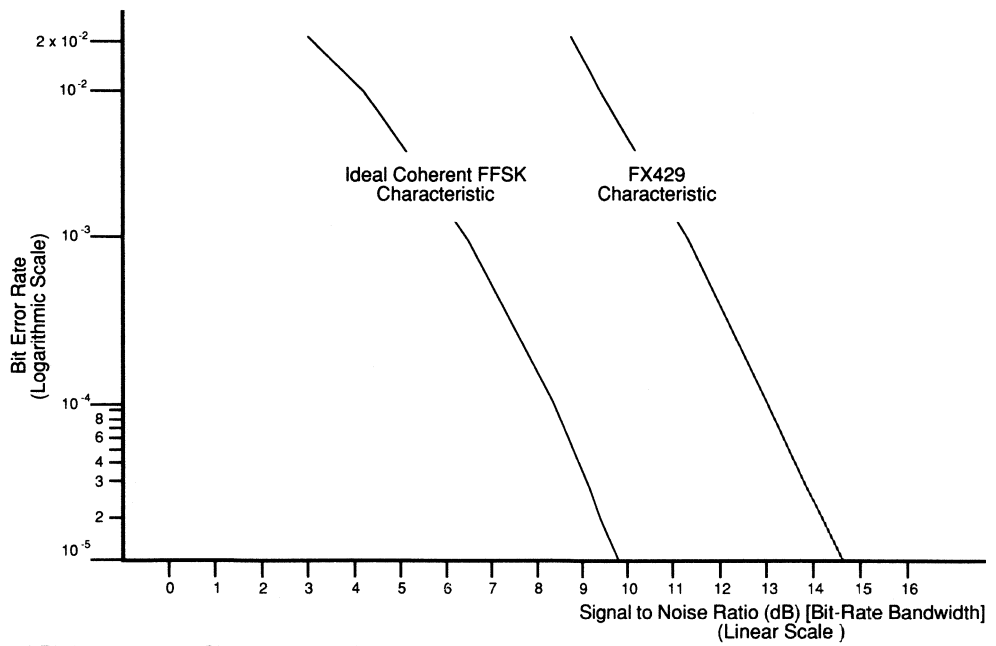
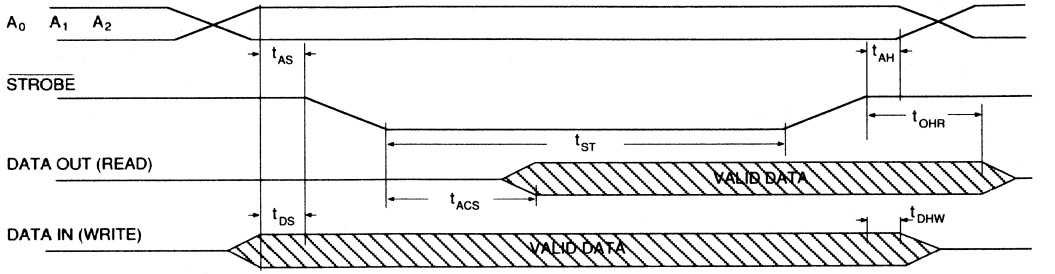



*Fig. 4 Bit Error Rate vs Signal to Noise Ratio*

# Timing Information




$t_{ACS}$ – Access Time
$t_{AS}$ – Address Setup Time
$t_{AH}$ – Address Hold Time
$t_{DS}$ – Data Setup Time
$t_{DHW}$ – Data Hold Time (Write)
$t_{OHR}$ – Output Hold Time (Read)
$t_{ST}$ – Strobe Time

*Fig. 5 Read and Write Timing Diagram*

## Operation – Rx

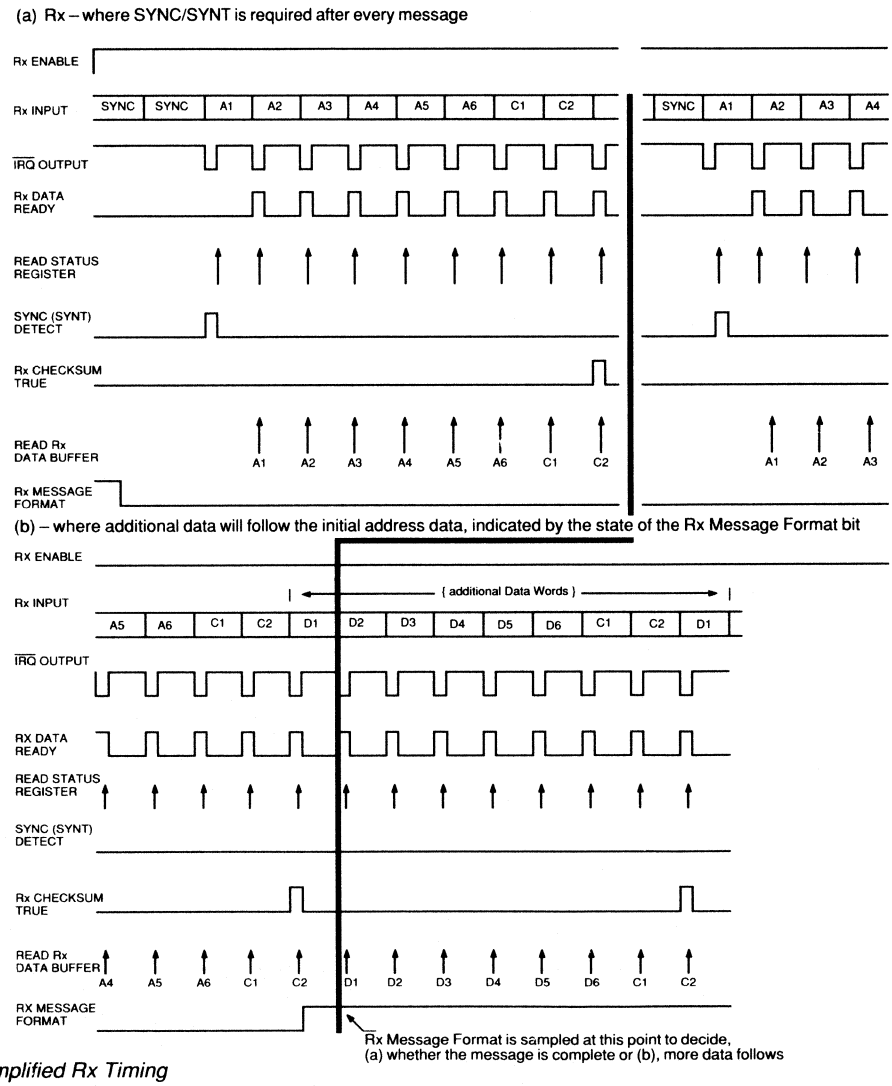



*Fig. 6 Simplified Rx Timing*

# Operation – Tx

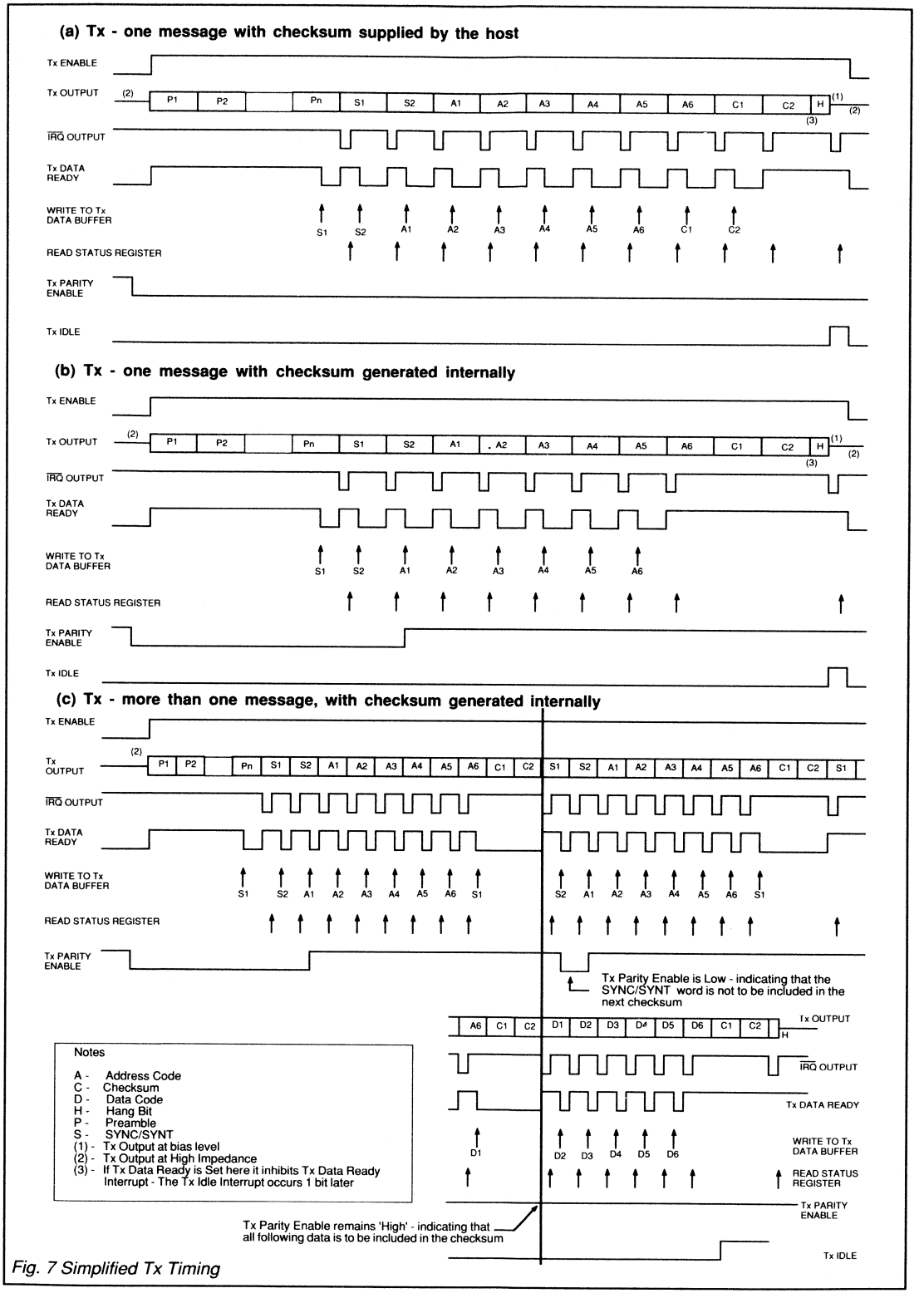



*Fig. 7 Simplified Tx Timing*

## Basic Power-Up Software

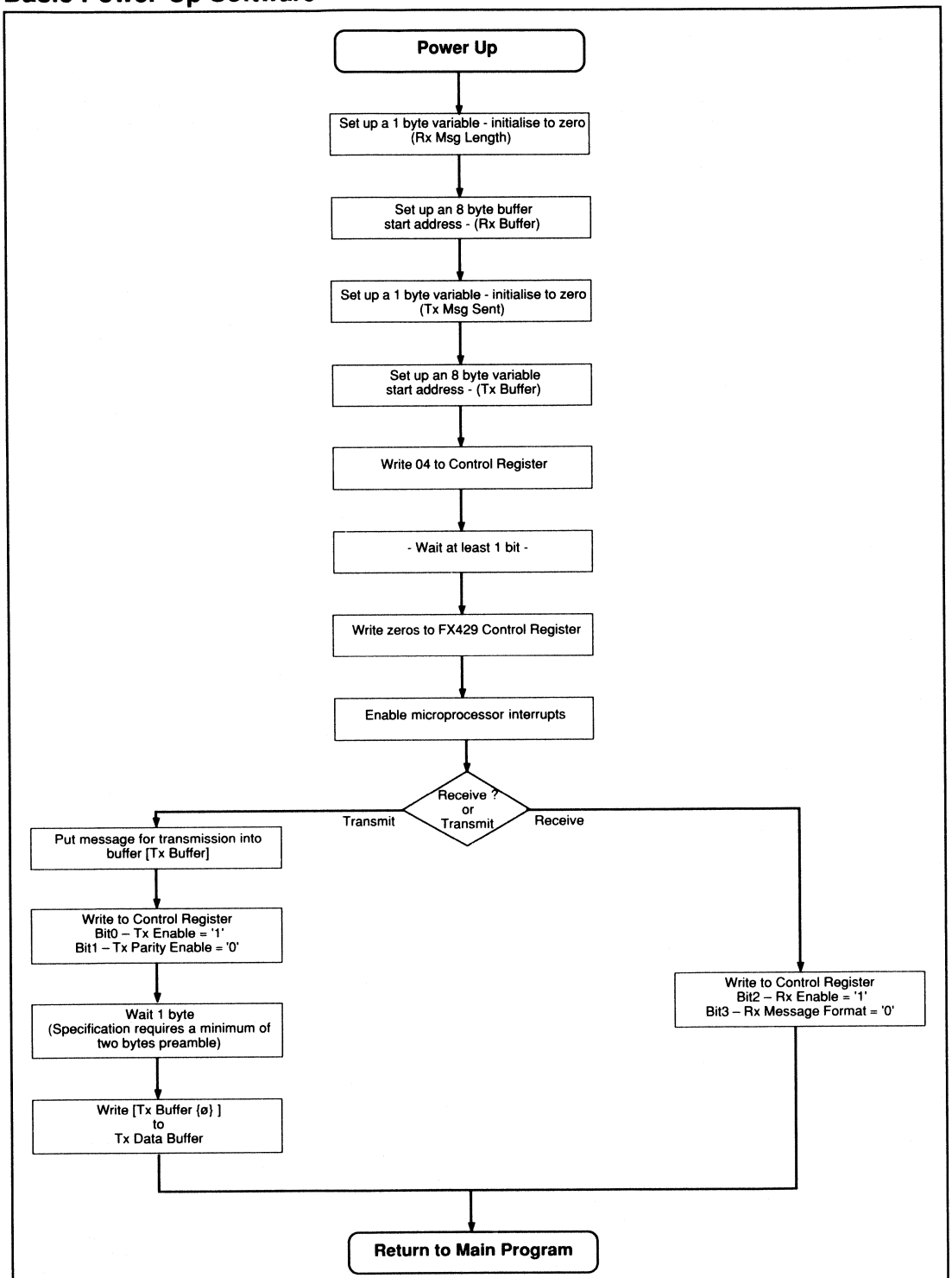



*Fig. 8 Power–Up Flow*

## Basic Software Interrupt Flow

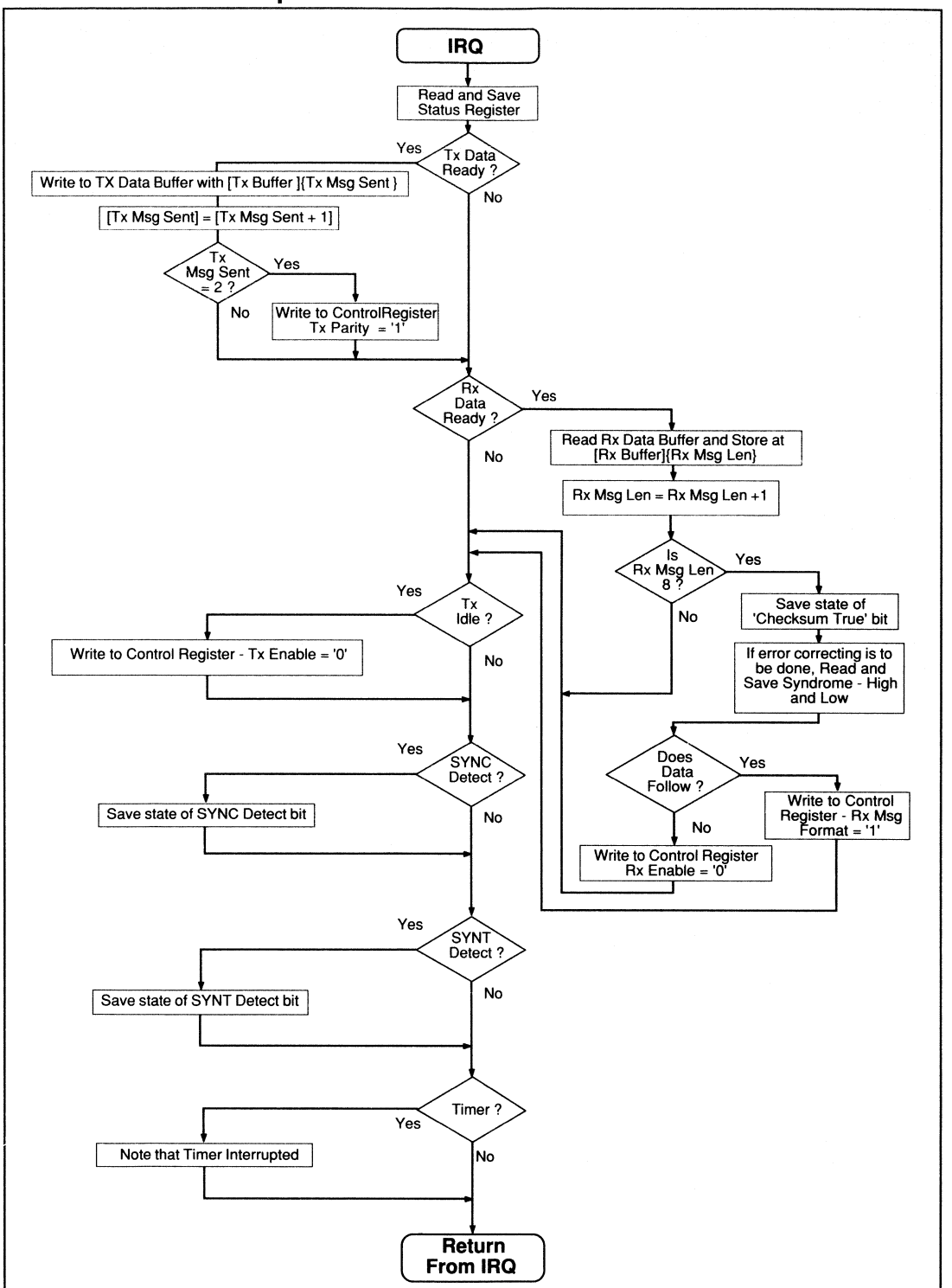



*Fig. 9 Interrupt Flow*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX429J** | -30°C to +85°C (ceramic) |
| | **FX429LG/LS** | -30°C to +70°C (plastic) |
| Storage temperature range: | **FX429J** | -55°C to +125°C (ceramic) |
| | **FX429LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Xtal/Clock $f_0$ = 4.032 MHz. Audio level 0dB ref: = 300mV rms.

Bit Rate Bandwidth = 1200Hz.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | – | 5.5 | V |
| Supply Current Ranges | | | | | |
| Rx and Tx Enabled | | – | – | 7.0 | mA |
| Rx Enabled, Tx Disabled | | – | 4.0 | 6.0 | mA |
| Rx Disabled, Tx Enabled | | – | – | 7.0 | mA |
| Rx and Tx Disabled | 10 | – | 1.5 | 2.5 | mA |
| **Dynamic Values** | | | | | |
| Modem Internal Delay | | – | 1.5 | – | ms |
| **Interface Levels** | | | | | |
| Output Logic '1' Source Current | 2 | – | – | 120 | µA |
| Output Logic '0' Sink Current | 3 | – | – | 360 | µA |
| Three State Output Leakage Current | | – | – | 4.0 | µA |
| **$D_0$ – $D_7$ Data In/Out** | 1 | | | | |
| Logic '1' Level | | 3.5 | – | – | V |
| Logic '0' Level | | – | – | 1.5 | V |
| **$A_1$, $A_0$, $A_2$, $\overline{\text{STROBE}}$, $\overline{\text{IRQ}}$** | 4 | | | | |
| Logic '1' Level | | 4.0 | – | – | V |
| Logic '0' Level | | – | – | 1.0 | V |
| **Analogue Impedances** | | | | | |
| Rx Input | | 100 | – | – | kΩ |
| Tx Output (Enabled) | | – | 10 | – | kΩ |
| Tx Output (Disabled) | | – | 5 | – | MΩ |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10 | – | – | MΩ |
| $R_{OUT}$ | 5 | 5.0 | – | 15 | kΩ |
| Oscillator Gain | | – | 15 | – | dB |
| Xtal frequency | | – | 4.032 | – | MHz |
| **Timing** – (Fig. 5) | | | | | |
| Access Time – ($t_{ACS}$) | | – | – | 135 | ns |
| Address Hold Time – ($t_{AH}$) | | 0 | – | – | ns |
| Address Set-up Time – ($t_{AS}$) | | 0 | – | – | ns |
| Data Hold Time (Write) – ($t_{DHW}$) | | 85 | – | – | ns |
| Data Set-up Time (Write) – ($t_{DS}$) | | 0 | – | – | ns |
| Output Hold Time (Read) – ($t_{OHR}$) | | 15 | – | 105 | ns |
| Strobe Time – ($t_{ST}$) | | 140 | – | – | ns |

# Specification .....

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Dynamic Values.....** | | | | | |
| **Receiver** | | | | | |
| Signal Input Levels | 6 | –9.0 | –2.0 | +10.5 | dB |
| Bit Error Rate | 7 | | | | |
| @ 12dB Signal/Noise Ratio | | – | 7.0 | – | $10^{-4}$ |
| @ 20dB Signal/Noise Ratio | | – | 1.0 | – | $10^{-8}$ |
| Synchronization @ 12dB Signal/Noise Ratio | 8 | | | | |
| Probability of Bit16 being correct | | – | 99.5 | – | % |
| Carrier Detect Response Time | 8 | – | 13.0 | – | ms |
| **Transmitter** | | | | | |
| Output Level | | – | 8.25 | – | dB |
| Output Level Variation | | -1.0 | – | +1.0 | dB |
| Output Distortion | | – | 3.0 | 5.0 | % |
| 3rd Harmonic Distortion | | – | 2.0 | 3.0 | % |
| Logic '1' Frequency | 9 | – | 1200 | – | Hz |
| Logic '0' Frequency | 9 | – | 1800 | – | Hz |
| Isochronous Distortion | | | | | |
| 1200Hz – 1800Hz | | – | 25 | 40 | µs |
| 1800Hz – 1200Hz | | – | 20 | 40 | µs |

**Notes**

1. With each data line loaded as, C = 50pf and R = 10kΩ.
2. $V_{OUT}$ = 4.6V.
3. $V_{OUT}$ = 0.4V
4. Sink/Source currents ≤ 0.1mA.
5. Both Xtal and Xtal ÷ 4 Outputs.
6. With 50dB Signal/Noise Ratio.
7. See Figure 3, Bit Error Rate.
8. This Response Time is measured using a 10101010101....01 pattern input signal at a level of 230mV rms (-2.3dB) with no noise.
9. Dependent upon Xtal tolerance.
10. Powersave is only active when both Rx and Tx functions are disabled.

## Checksum Generation and Checking

**Generation** – The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
This 16–bit word is used as the "Checksum."

**Checking** – The checksum checker does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

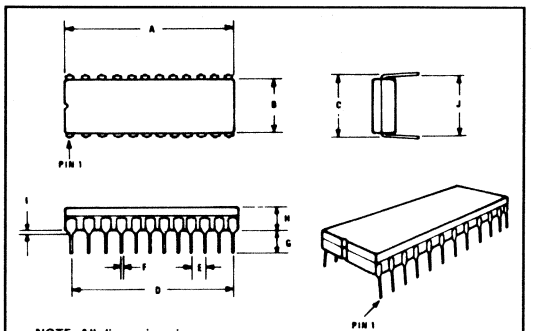
$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero.
Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).
If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (SR $D_1$) bit is set.

## Package Outlines

The FX429J, the cerdip package is shown in Figure 10, the 'LG' version in Figure 11 and the 'LS' version in Figure 12.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all package styles number anti-clockwise when viewed from the top (indent side).

*Fig.10* ***FX429J DIL Package***



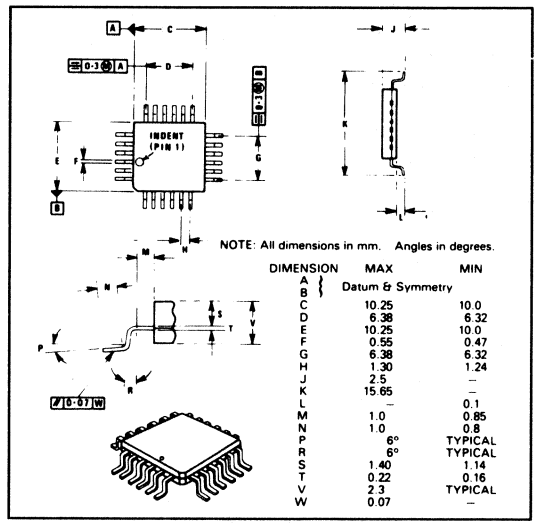

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 32.03 | 31.50 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 } | TYPICAL |
| F | 0.46 } | |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 | TYPICAL |
| J | 18.20 | 16.54 |

## Handling Precautions

The FX429 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

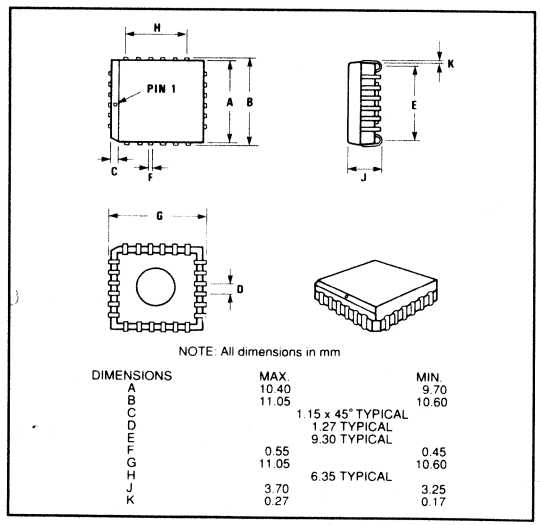
*Fig.11* ***FX429LG Package***




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A } | Datum & Symmetry | |
| B } | | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig.12* ***FX429LS Package***




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

## Ordering Information

| | |
|---|---|
| **FX429J** | **24-pin cerdip DIL** |
| **FX429LG** | **24-pin quad plastic encapsulated, bent and cropped** |
| **FX429LS** | **24-lead plastic leaded chip carrier** |

# CML Semiconductor Products

PRODUCT INFORMATION

# FX529 FFSK Modem for Trunked Radio Systems

Publication D/529/1 December 1991
Provisional Issue

## Features

- PAA 1382 and General Purpose Trunked Radio Applications
- Meets Draft ETSI EBSS 1200 Signalling Specification
- Full-Duplex 1200 Baud Operation
- High Intelligence
- Error Checking in Receive
- Frame SYNC/SYNT Detection
- Preamble Generation
- µProcessor Compatible Interface
- Carrier Detection On-Chip
- General Purpose Timer
- Error Check Word Generation

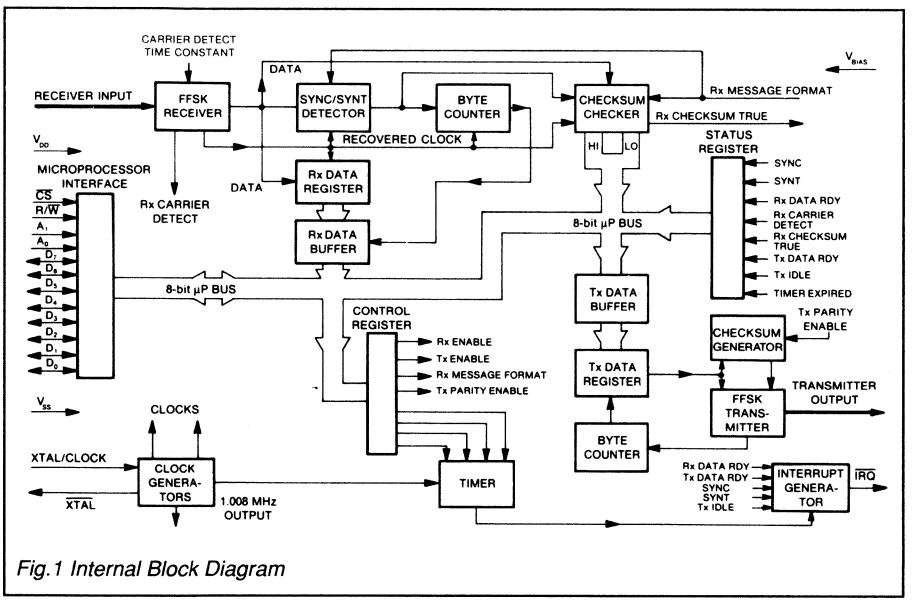



*Fig.1 Internal Block Diagram*

FX529

## Brief Description

The FX529 is a single-chip CMOS 1200 baud FFSK Modem, designed primarily for use in trunked radio systems but may also be employed in other general purpose radio or line data communication applications.

The device has been designed to conform to the French trunked radio protocol PAA 1382

The FX529 is full duplex at 1200 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of between 8 and 120 bits.

Preamble data and an error-check word are automatically generated in the transmit mode.

Error checking is performed and the 16-bit SYNC word is detected in the receive mode.

An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides all microcircuit filter sampling clocks and modem timings whilst also supplying a "Clock ÷ 4" output (1.008MHz).

The FX529, which has a powersaving facility, requires a single 5-volt power supply and is available in both cerdip DIL and plastic SMD packages.

Publication D/Signalling/1 May 1988

# *DIGITAL SIGNALLING FORMAT FOR MOBILES*

*A step towards standardization of the digital transmission over mobile radio has been made with the UK recommendation of a new format. It specifies a binary format for general purpose use in applications such as selective calling and vehicle identification through to mobile printers and computer terminals. This article, written by P.J. Mabey of Philips Research Laboratories, and published in "Communications International", describes how the format has been tailored to mobile radio requirements, presents the results of performance measurements, and discusses the application of the format which has been submitted to the CCIR for consideration.*

## Introduction

Data transmission in mobile radio is becoming increasingly important for easing channel congestion and for the new facilities that is enables. Unfortunately it has to operate under extremely unfavourable conditions, suffering from the combined impairments of ignition noise interference from nearby vehicles, signal fading caused by multi-path propagation and shadowing, and co-channel interference which results from sharing the radio channel locally and re-using the channel in another part of

## Data Format

In order to ease and encourage the introduction of data transmission in the UK the Electronic Engineering Association (EEA), an association of manufacturers, and the Home Office radio regulatory department, in consultation with mobile radio users, have recommended the binary data format illustrated in Figs.1 and 2 for mobile data communication.

This format provides a high reliability, high falsing immunity and a high throughput. It is designed for variable length messages, being suitable for short message applications such as status reporting and vehicle identification through to text transmission for mobile printers and terminals. Various data formats are already in use for specific applications of data transmission over mobile radio, for example in mobile telephony and radiopaging, but none of these formats were considered suitable as a standard for the wide range of applications expected for mobile data transmission.

Maximum benefit will be obtained by widespread use of the recommended format, and hopefully it will become established outside the UK. The format has been considered by CCIR and has now been included in a CCIR Report.

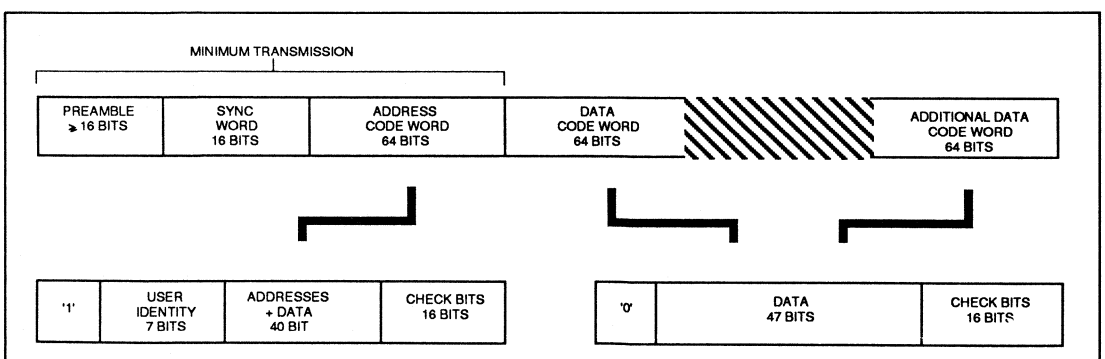



*Fig. 1 Binary data format and code word structure as standardised by the EEA, for high reliability, high falsing immunity and high throughput*

## High Level Data Link Control (HDLC)

When choosing a data format to use on mobile radio an obvious candidate to consider is h.d.l.c. which is an international standard. We will discuss the differences between the EEA and the h.d.l.c. formats and show how the former is better suited to mobile radio. The h.d.l.c. frame is illustrated in Fig. 2. A frame comprises an eight bit start flag, a variable length code word, and an eight bit terminating flag. The terminating flag can also act as the start flag for the next frame. Each code word contains an address and control field. Because the frame length is variable, a bit stuffing scheme is used in which an extra bit is inserted whenever necessary to ensure that the flag sequence is not simulated in the transmitted data.

The error rates encountered on the mobile radio channel are so high that code words should be kept short to ensure an acceptable chance of being received error free. Consequently, many code words may be necessary to accommodate a message. With short words, the address, control and flag bytes for each word would be a severe overhead on throughput, in a medium where a high throughput is important. In contrast the EEA format puts the address and control information into only the first code word of a message, and uses a fixed length code word, which avoids the flag between words. The code words may be decoded independently and a retransmission protocol used to recover corrupted words.

The overhead of a terminating flag byte might be compensated by the reduced quantization waste of variable length code words, but variable length words with delimiting flags and bit stuffing have other disadvantages. Because the h.d.l.c. flag acts as both a frame terminator and an opener for the next frame, corruption of the flag results in the loss of two frames. If error correction is applied, a variable length code word would complicate the decoder. Further, channel errors can cause a decoder to fail to remove stuffing bits, and also mistake data for stuffing bits and wrongly remove them. As a result the decoded code word may be the wrong length, in which case the error correction procedures will be unsuccessful.

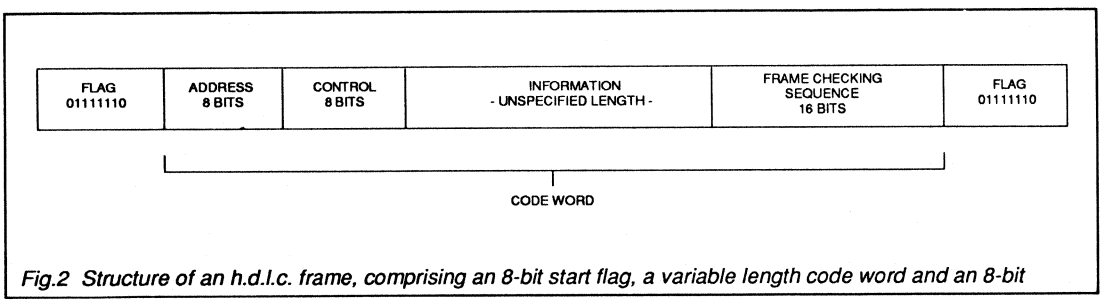



*Fig.2 Structure of an h.d.l.c. frame, comprising an 8-bit start flag, a variable length code word and an 8-bit*

## Flag Sequence

The code used for the h.d.l.c. format ensures that code words all differ in at least four bit positions, so guaranteeing detection of up to three bit errors in a word. The EEA code guarantees detection of up to five errors, which gives it better scope for error correction.

Finally, in mobile radio where a decoder can be exposed to random bits between transmissions, an eight bit flag sequence for word synchronization would be too short for a fixed word length format without terminating flags. A simple decoder can spuriously recognize the synchronization sequence in the bits preceding a message, enter a message decoding algorithm, and so miss the real message. The probability of this is $(s + n)2^{-s} = 0.28$ for an s bit synchronization sequence ($s = 8$) and n bit code word ($n = 64$), which evidently would lead to serious degradation of the message success rate. To summarize, the EEA format is expected to have a significantly higher throughput and success rate than the h.d.l.c. format. This is important for spectrum efficiency. The format specification defines only a basic framework for sending data messages, leaving scope for flexibility in application. Decoding methods are not prescribed. An error detecting decoder can be realized quite simply, for example an encoder, decoder plus a modem have been implemented in one single chip microcomputer, and yet is sufficient for a good performance. The application of error correction will enhance the performance.

The recommended data format is illustrated in Figs. 1 and 2. A full definition is given in the EEA report. Transmissions begin with a preamble of bit reversals 1010.....10 so that the receiver data demodulator can acquire bit synchronization. Every message begins with a 16-bit synchronization word to enable the decoder to establish code word framing. The synchronization word was chosen for a high probability of detection, good correlation properties and infrequent spurious detection.

## Error Detecting

Messages are transmitted in 64-bit code words comprising 48 information bits and 16 error check bits. These check bits are determined by a powerful error detecting code. The first code word of a message contains addressing information and some data, and is sufficient for short message applications such as status reporting. The suggested allocation of the 40 bits available for addresses and data, (Fig. 2) is 12 bits for address identity, 12 bits for address or identity, and 16 bits for data. For longer messages with more data such as text, additional data code words are appended as required to accommodate the message.

In order to avoid false calls, it is important not to mistake a data code word for an address code word. Therefore the format distinguishes address and data code words by a one bit flag. Address code words are partly distinguished by being always preceded by the synchronization word. However, without the flag, a data code word may be mistaken for an address code word when the check bits of the preceding code word match the synchronization word. Although only 1 in $10^5$ code words are in this category, falsing could become a problem should a system send these code words frequently.

## Exclusive Use

Mobile radio users commonly share a radio channel with other organizations because there are insufficient radio channels to permit exclusive use. It is important that different organizations do not accept each others' messages, so the format provides for every message to be labelled with the user's identity in shared channel operation. This identity is normally the organization's or licence holder's identity, not an individual mobile identity. The user identity occupies seven bits, but does not impose a limit of 128 users per channel, or set of channels. Different organizations operating on a common radio channel can have the same user identity if they are spaced geographically far enough apart not to interfere. Therefore, the user identities must be allocated according to a national plan; in the UK, this will be done by the Home Office. It is important to realize that co-channel interference in the form of data messages from different users sharing the same user identity can result in false calls being made.

Measurements have been made of the chance of receiving a message successfully Fig. 3 shows the message success rate when short messages without data code words were transmitted over conventional f.m. mobile radio equipment with 1200 bit/s fast frequency shift key (f.f.s.k.) data modulation and a simple error detecting decoder. The steady signal level curves were measured in the laboratory and apply to a stationary vehicle. The moving vehicle curves were measured during field tests under typical fading conditions. The EIA land mobile signalling standard RS374A specifies that a message success rate of 80% should require a steady signal level of ≤3dB, relative to the 12dB SINAD level, and that the degradation with a fading signal should be less than 20dB. The EEA format is well within these targets requiring 1dB with a steady signal and a mean level of 9dB at v.h.f (14dB at u.h.f.) with fading.

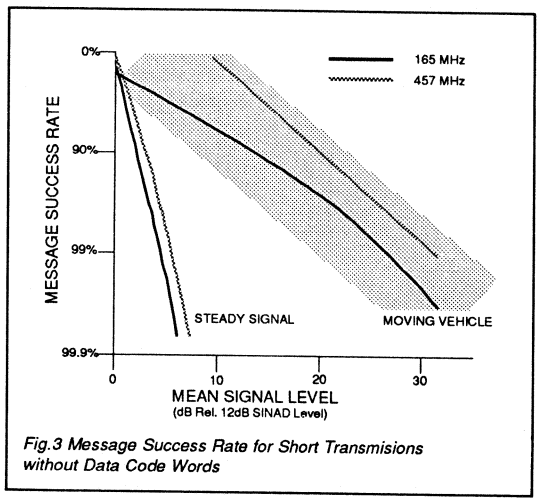



*Fig.3 Message Success Rate for Short Transmisions without Data Code Words*

The difference in performance between moving and stationary vehicles is not as dramatic as it may seem initially. Because there is a chance that a vehicle may park where the signal is faded, a mean level of 8dB (rel. 12dB SINAD) is required to ensure that stationary vehicles have an average success rate of 80%. Further, moving vehicles benefit significantly from retransmissions, and can readily have a superior success rate to stationary vehicles.

## Falsing Immunity

The falsing immunity required will depend on the particular application, and the false rates experienced will depend on the decoding method. Whatever decoding method is used there are several falsing mechanisms which must be evaluated:

*False address word.* Errors can corrupt an address code word into another address word, resulting in a false call.

*False data word.* Errors can corrupt a data code word into another data word, resulting in a false message.

*Spurious calls.* A call can be spuriously decoded from noise, speech or interference, when no calls is, in fact, in the process of being transmitted.

*Misframed calls.* Errors may corrupt the synchronization word which is then simulated in the received data, and an address code word is formed misframed, resulting in a false call.

*Bit slip.* A burst of noise or interference may cause bit slip in the data demodulator and data code words are decoded misframed, resulting in a false message.

*Interference.* Another transmission can overlap in time and substitute part of a message, so that the decoded call is a composite of wanted and interfering data words, resulting in a false message.

## False Probability

The format design ensures that a simple error detecting decoder can achieve a very low false probability. For example, Fig. 3 shows the probability that a synchronization word and address code word will be decoded as a synchronization word and a different address code word. As the signal level is reduced the false rate peaks and then becomes very small at low signal levels because failure to synchronize prevents decoding. The peak false is $10^{-6}$ per transmitted call.

Such low false rates are impractical to measure, and so these curves are predictions from calculations and the analysis of bit error patterns recorded during mobile data transmission experiments.

The RS374A standard suggests that the level of falsing immunity is specified in one of four categories: low, medium, high and secure. The EEA format is adequate for the most stringent category, where 'secure' is defined as a false rate less than $10^{-5}$.

## Optimization

Addressing and handshake protocols will further reduce falsing, whereas the application of error correction will tend to increase falsing. Clearly there is much scope for optimizing decoders for specific applications and it is up to designers to demonstrate that their implementation has adequate falsing capabilities. Analysis has shown that the geographical range of mobile data systems which use the EEA format will be at least as good as the range for speech communication. A good combined high reliability and high throughputs obtained by the use of an efficient code in the format, with only 25% error check bits, and a retransmission protocol which repeats messages, but only when necessary as most vehicles will receive the initial transmission of a message.

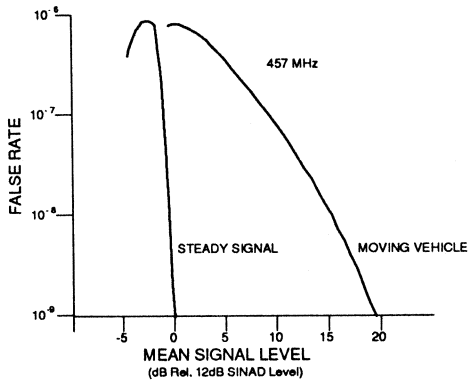



*Fig.4 False Rate for Moving and Fixed Signals*

Selective retransmission of only the corrupted code words is particularly efficient.

Both moving and stationary vehicles were considered in the analysis. Moving vehicles were found to have a lower throughput (e.g. 0.46 for a short text of 67 characters) than stationary vehicles (correspondingly 0.6) because they require more retransmissions. These throughputs include all the overheads of transmitter turn-on time, synchronizing and obtaining an acknowledgement. Careful application of error correction to the format will reduce the amount of retransmission and will, consequently, increase the throughput for moving vehicles.

## *Conclusions*

*The recommended binary format is the result of a desire by mobile radio manufacturers and users for digital signalling standards. For manufacturers, standardization minimizes the variety of signalling schemes to be supported, while customers can have confidence in a system which is approved and supported by several manufacturers. The format has been designed specifically to suit the characteristics of mobile radio and is flexible for a wide range of mobile applications. It is efficient, offering a good throughout. It has good falsing immunity. A simple decoder is sufficient, yet there is scope to optimize the decoder for specific applications. Reliable data communications will be possible throughout existing mobile radio service areas which were designed originally for speech communication.*

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# CML Semiconductor Products

PRODUCT INFORMATION

# FX439 FFSK Modem

Publication D/439/5 February 1993
Provisional Issue

## Features/Applications

- 1200 Baud FFSK Modem
- Meets Cellular and Trunked Radio Specifications
- Full-Duplex 1200 Baud
- On-Chip Rx and Tx Bandpass Filters
- Clock Recovery and Carrier Detect Facilities
- Pin Selectable Xtal/Clock Frequencies (1.008MHz or 4.032MHz Input)
- Mobile and Cellular Radio Data Signalling
- NMT 450/900
- Band III
- Radiocom 2000
- ZVEI
- Personal Radio
- Portable Data Terminals
- General Purpose Applications

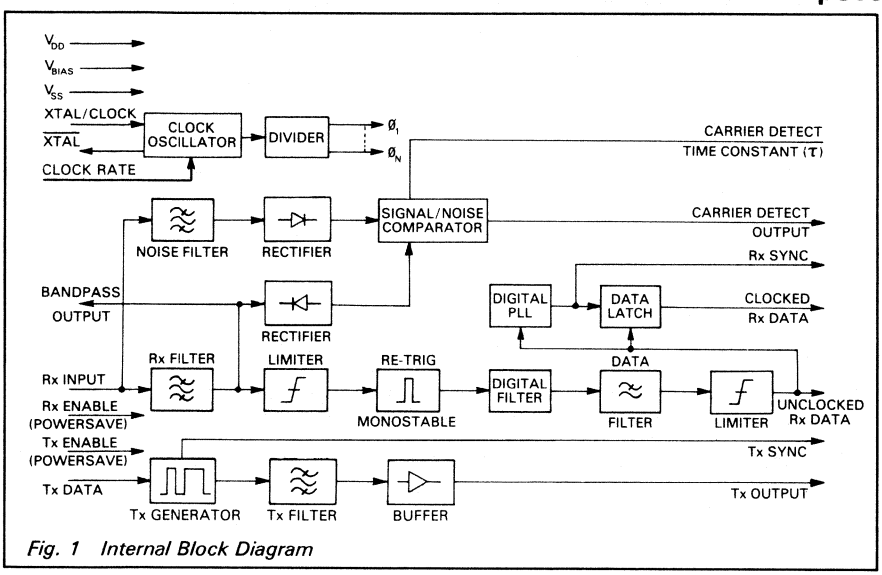



*Fig. 1 Internal Block Diagram*

FX439

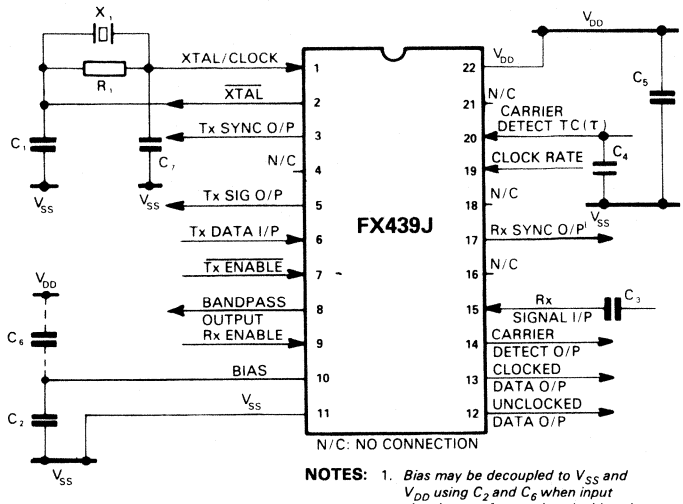
## Brief Description

The FX439 is a single-chip CMOS LSI circuit which operates as a 1200 baud FFSK modem. The mark and space frequencies are 1200Hz and 1800Hz phase continuous and the frequency transitions occur at the zero crossing point. The transmitter and receiver will work independently, thus providing full-duplex operation at 1200 baud. The baud rate, transmit mark and space frequencies, Tx and Rx synchronization are all derived from a highly stable Xtal oscillator. The on-chip oscillator is capable of working at one of two input frequencies, from a 1.008MHz or 4.032MHz external Xtal/clock input, frequency being pin selectable with the 'Clock Rate' logic input. The device includes circuitry for carrier detect and facility for the Rx clock recovery. An on-board switched capacitor 900Hz – 2100Hz bandpass filter provides optimum carrier filtering. The use of switched capacitor analogue filters and digital signal processing results in excellent dynamic performance with few external components, the CMOS process and current saving techniques offer low standby supply current for portable battery powered applications.

## Pin Number Function

| FX439 DW | FX439 J | FX439 LG/LS | Function |
|---|---|---|---|
| 1 | 1 | 1 | **Xtal/Clock:** The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. |
| 2 | 2 | 2 | **$\overline{\text{Xtal}}$:** Output of the on-chip inverter (See Figure 2). |
| 3 | 3 | 3 | **Tx Sync O/P:** A 1200Hz squarewave used to synchronize the input of logic data and transmission of the FFSK signal (See Figure 5). |
| 4 | 5 | 5 | **Tx Signal O/P:** When the transmitter is enabled, this pin outputs the 1200/1800Hz (140-step pseudo sinewave) FFSK signal (See Figure 5). With the transmitter disabled, this output is set to a high-impedance state. |
| 5 | 6 | 7 | **Tx Data I/P:** Serial logic data to be transmitted is input to this pin. |
| 6 | 7 | 8 | **$\overline{\text{Tx Enable}}$:** A logic '0' will enable the transmitter (See Figure 5). A logic '1' at this input will put the transmitter into powersave whilst forcing the "Tx Sync O/P" to a logic '1' and "Tx Signal O/P" to a high-impedance state. This pin is internally pulled to $V_{DD}$. |
| 7 | 8 | 9 | **Bandpass O/P:** The output of the Rx 900Hz-2100Hz bandpass filter. This output impedance is typically 10kΩ and may require buffering prior to use. |
| 8 | 9 | 10 | **Rx Enable:** The control of the Rx function. The control of other outputs is given below.<br>**Rx Enable = Rx Function — Clock Data O/P — Carrier Detect — Rx Sync Out**<br>"1" = Enabled — Enabled — Enabled — Enabled<br>"0" = Powersave — "0" — "0" — 1" or "0"<br>When both Tx and Rx functions are disabled, the bias voltage is switched internally to $V_{SS}$ (via ≈25kΩ). Bias line $R_{OUT}$ ≈12.5kΩ. With the Bias line decoupled by a 1.0µF capacitor ($C_2$) the FX439 may take approximately 25 milli-seconds to establish correct operation when enabling the Rx facility. This period may be minimized by either: reducing the value of $C_2$, lowering the bias line impedance externally or adopting a different powersaving strategy (such as using $C_2$ and $C_6$ and supplying $V_{DD}$ via a series switch). This pin is internally pulled to $V_{DD}$. |
| 9 | 10 | 11 | **Bias:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to $V_{SS}$ by a capacitor ($C_2$). (See Figure 2 and *Rx Enable* notes). |
| 10 | 11 | 12 | **$V_{SS}$:** Negative supply rail (GND). |
| 11 | 12 | 13 | **Unclocked Data O/P:** The recovered asynchronous serial data output from the receiver. |
| 12 | 13 | 14 | **Clocked Data O/P:** The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "Rx Sync O/P," (See Figure 6). |
| 13 | 14 | 15 | **Carrier Detect O/P:** When an FFSK signal is being received this output is a logic '1.' |
| 14 | 15 | 16 | **Rx Signal I/P:** The FFSK signal input for the receiver. This input should be coupled via a capacitor, $C_3$. |
| 15 | 17 | 18 | **Rx Sync O/P:** A flywheel 1200Hz squarewave output. This clock will synchronize to incoming Rx FFSK data (See Figure 6). |
| 18 | 19 | 21 | **Clock Rate:** A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz). |
| 19 | 20 | 22 | **Carrier Detect Time Constant (τ ):** Part of the carrier detect integration function. The value of $C_4$ connected to this pin will affect the carrier detect response time and hence noise performance (See Figure 2, Note 3). |
| 20 | 22 | 24 | **$V_{DD}$:** Positive supply rail. A single 5-volt supply is required. |
| 16, 17 | 4, 16,18, 21 | 4, 6, 17,19, 20, 23 | No Internal Connection, do not use. |

*Note: Output Loading. Large capacitive loads would cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of typically 100Ω put in series with the load should minimise this effect.*




**NOTES:**

1. *Bias may be decoupled to $V_{SS}$ and $V_{DD}$ using $C_2$ and $C_6$ when input signals are referenced to the bias pin. For input signals referenced to $V_{SS}$, decouple Bias to $V_{SS}$ using $C_2$ only.*
2. *Use $C_5$ when input signals are referenced to $V_{SS}$, to decouple $V_{DD}$.*
3. *The value of $C_4$ determines the carrier detect time constant. A long time constant results in improved noise immunity but increased response time. $C_4$ may be varied to trade-off response time for noise immunity.*
4. *The value of $C_7$ reduces xtal voltage overshoot. Refer to CML Xtal Oscillator application note D/XT/1 APRIL 1986.*
5. *$X_1$ can be either a 1.008MHz or 4.032MHz Xtal, dependant upon the 'Clock Rate' setting.*

**Component References**

| Component | Unit Value | Tolerance % |
|---|---|---|
| $R_1$ | 1M | ±10 |
| $C_1$ | 33p | |
| $C_2$ | 1.0µ | ±20 |
| $C_3$ | 0.1µ | |
| $C_4$ | 0.1µ | ±10 |
| $C_5$ | 1.0µ | ±20 |
| $C_6$ | 1.0µ | |
| $C_7$ | 33p | |
| $X_1$ | 1.008MHz or 4.032MHz | See 'Clock Rate' Pin |

*Fig. 2 External Component Connections*

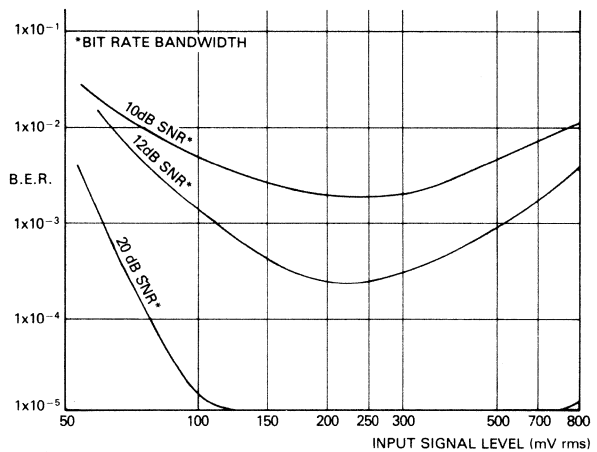



*Fig. 3 Typical Variation of 'B.E.R.' with Input Signal Level*

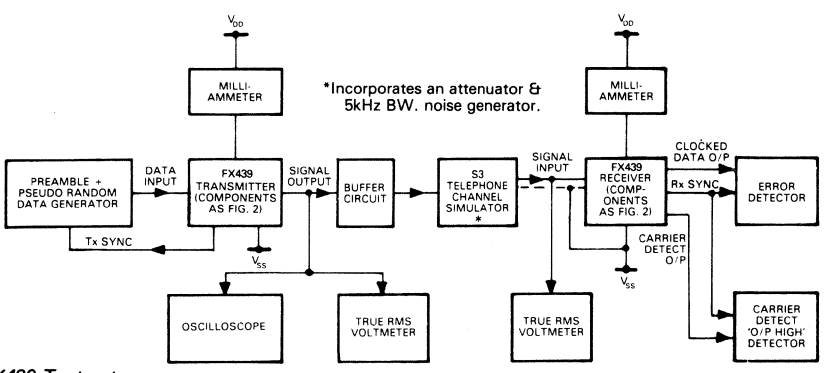



*Fig. 4 FX439 Test set-up.*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX439J | -30°C to +85°C (cerdip) |
| | FX439DW/LG/LS | -30°C to +70°C (plastic) |
| Storage temperature range: | FX439J | -55°C to +125°C (cerdip) |
| | FX439DW/LG/LS | -40°C to +85°C (plastic) |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |

## Operating Limits

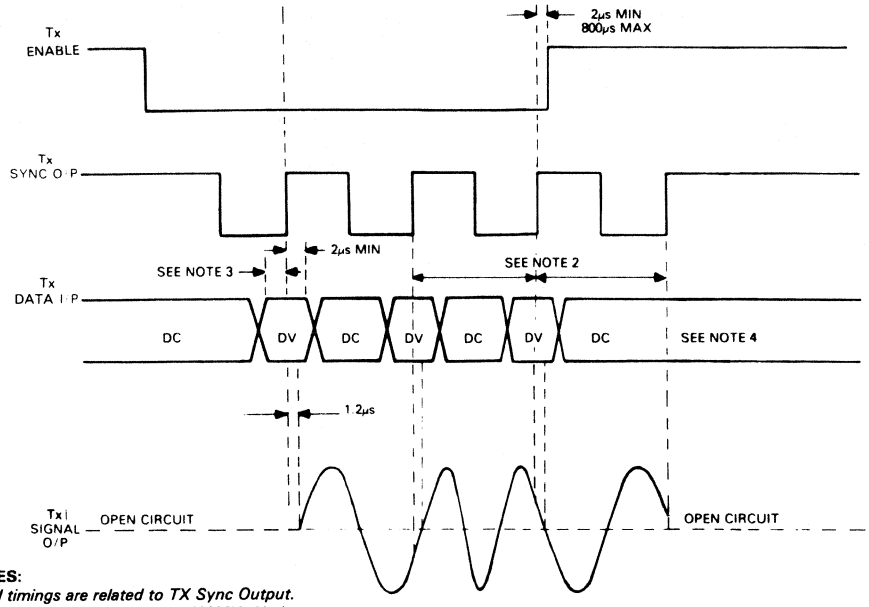
All characteristics measured using the standard test circuit *(Figure 4)* with the following test parameters and is valid for all tests unless otherwise stated:
$V_{DD}$ = +5V, $T_{amb}$ = 25°C, Xtal ($X_1$) Frequency: 1.008MHz

| | |
|---|---|
| 0dB reference | 300mV rms |
| Noise | (band limited 5kHz gaussian white noise) |

SNR ratio measured in bit rate bandwidth (1200Hz)

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Characteristics** | | | | | |
| Supply Volts | | 4.5 | 5.0 | 5.5 | V |
| Supply Current: Rx (Enabled) Tx (Disabled) | | — | 3.6 | — | mA |
| Rx (Enabled) Tx (Enabled) | | — | 4.5 | — | mA |
| Rx (Disabled) Tx (Disabled) | | — | 650 | — | µA |
| Logic '1' level | | 80%$V_{DD}$ | — | — | V |
| Logic '0' level | | — | — | 20%$V_{DD}$ | V |
| Digital Output Impedance | | — | 4 | — | kΩ |
| Analogue and Digital Input Impedance | | 100 | — | — | kΩ |
| Tx Output Impedance | | — | 10 | — | kΩ |
| On-Chip Crystal Oscillator: | | | | | |
| $R_{in}$ | | 10 | — | — | MΩ |
| $R_{out}$ | | 5 | — | 15 | kΩ |
| Inverter Gain | | 10 | — | 20 | dB |
| Gain Bandwidth Product | | $3 \times 10^6$ | — | — | |
| Crystal Frequency | 1 | — | 1.008 | — | MHz |
| Crystal Frequency | 1 | — | 4.032 | — | MHz |
| **Dynamic Characteristics** | | | | | |
| **Receiver:** | | | | | |
| Signal Input: Dynamic Range (50dB SNR) | 2, 3 | 100 | 230 | 1000 | mV rms |
| Bit Error Rate: 12dB SNR | 3 | — | 7.0 | — | $10^{-4}$ |
| 20dB SNR | 3 | — | 1.0 | — | $10^{-8}$ |
| **Receiver Synchronization 12dB SNR:** | 6 | | | | |
| Probability of Bit 8 being correct | | | 0.99 | | |
| Probability of Bit 16 being correct | | | 0.995 | | |
| **Carrier Detect** | 4 | | | | |
| Sensitivity | 6, 7 | — | — | 150 | mV rms |
| Probability of Carrier Detect being high: | | | | | |
| 12dB SNR after Bit 8 | 4, 8 | — | 0.98 | — | |
| 12dB SNR after Bit 16 | 4, 8 | — | 0.995 | — | |
| 0dB Noise (No Signal) | 8 | — | 0.05 | — | |
| **Transmitter Output** | | | | | |
| Tx Output Level | | — | 775 | — | mV rms |
| Output Level Variation 1200/1800Hz | | 0 | — | ±1.00 | dB |
| Output Distortion | | — | 3 | 5 | % |
| 3rd Harmonic Distortion | | — | 2 | 3 | % |
| Logic '1' Carrier Frequency | 5 | — | 1200 | — | Hz |
| Logic '0' Carrier Frequency | 5 | — | 1800 | — | Hz |
| Isochronous Distortion | | | | | |
| 1200Hz – 1800Hz | | — | 25 | 40 | µs |
| 1800Hz – 1200Hz | | — | 20 | 40 | µs |

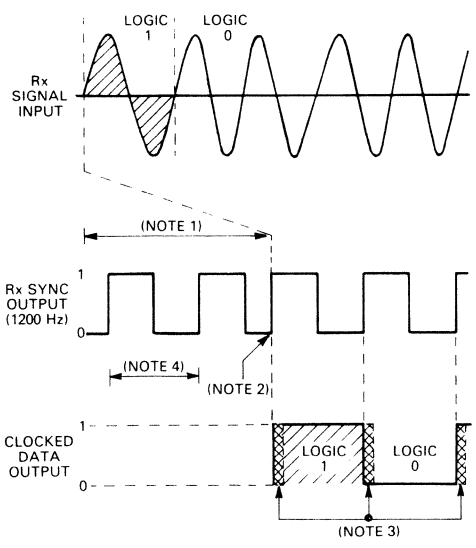
**Notes:** *1. Crystal frequency, type and tolerance depends on system requirements.*
*2. See Figure 3.*
*3. SNR (Bit Rate Bandwidth).*
*4. See Figure 2 Note 3.*
*5. Depending on crystal tolerance.*
*6. 10101010101 . . . pattern.*
*7. Measured with 150mV rms signal (No noise).*
*8. 0dB level for CD probability measurements is 230mV rms.*




**NOTES:**

1. *All timings are related to TX Sync Output.*
2. *0.833ms for 1.008MHz or 4.032MHz Xtal.*
3. *2μs Min + Crystal tolerance.*
4. *DC = Don't Care. DV = Data Valid.*

*Fig. 5 Transmitter Timing Diagram*




**NOTES:**

1. *Internal Delay-typ 1.5ms.*
2. *From freely running to Sync in 8 data bits (See spec).*
3. *Undetermined state—2μs max.*
4. *Min. 800μs—Max. 865μs.*

*Fig. 6 Receiver Timing Diagram*

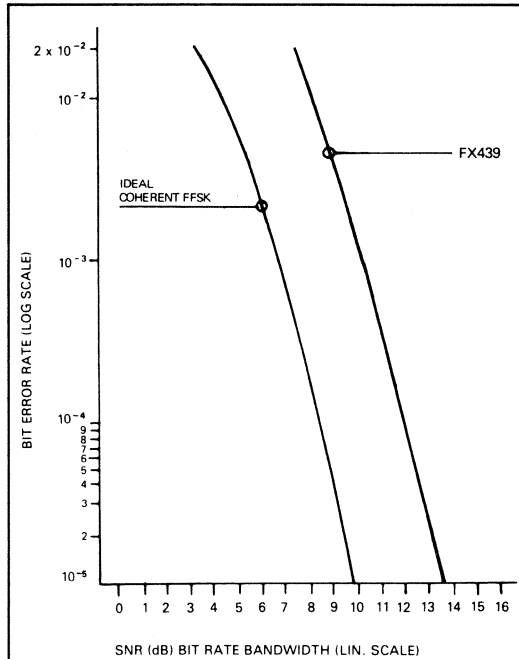
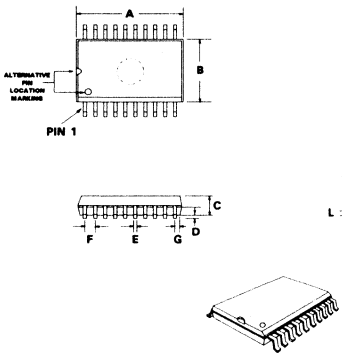



*Fig. 7 Receiver B.E.R. Vs SNR*

## Package Outlines

The FX439DW, the S.O.I.C. package is shown in Figure 8, the 'J' version in Figure 9, the 'LG' version in Figure 10 and the 'LS' version in Figure 11.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top (indent side).

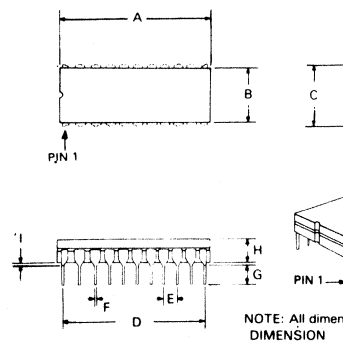
Fig.8 **FX439DW** *S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 12.85 | | 12.62 | G | | 0.66 | |
| B | 7.59 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.9* ***FX439J*** *Package*



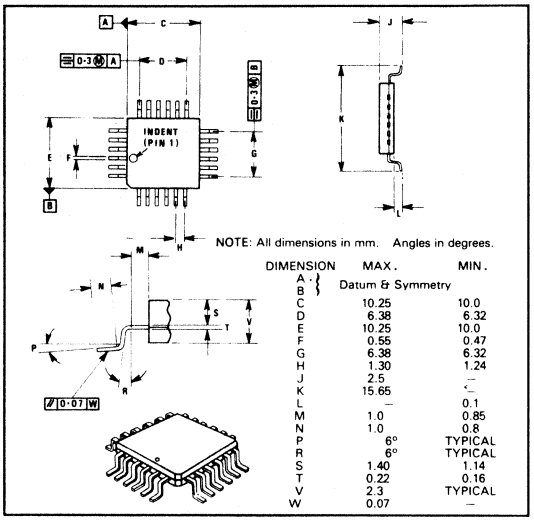

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 | TYPICAL |
| F | 0.46 | DIMENSION |
| G | 4.30 | 4.10 |
| H | 4.27 | 3.99 |
| I | 1.4 | TYPICAL |

## Handling Precautions

The FX439 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

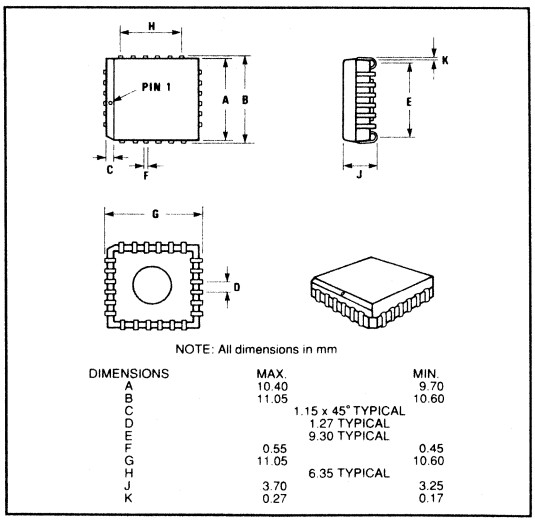
*Fig.10* ***FX439LG*** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | — |
| K | 15.65 | — |
| L | — | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | — |

*Fig.11* ***FX439LS*** *Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

## Ordering Information

| | |
|---|---|
| **FX439DW** | 20-pin surface mount S.O.I.C. |
| **FX439J** | 22-pin cerdip DIL |
| **FX439LG** | 24-pin quad plastic encapsulated, bent and cropped |
| **FX439LS** | 24-lead plastic leaded chip carrier |

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX469 1200 and 2400 Baud FFSK Modem

Publication D/469/2 February 1993
Provisional Information

## Features

- **Selectable Data Rates** ***1200 and 2400 Baud***
- **Full-Duplex FFSK**
- **Rx and Tx Bandpass Filters**
- **Clock Recovery and Carrier Detect Facilities**
- **Rx and Tx Enable Functions**
- **Pin Selected Xtal/Clock Inputs** ***1.008MHz or 4.032MHz***
- **Radio and General Applications**
  - **Data-Over-Radio**
  - **PMR and Cellular Signalling**
  - **Portable Data-Terminals**
  - **Personal/Cordless Telephone**

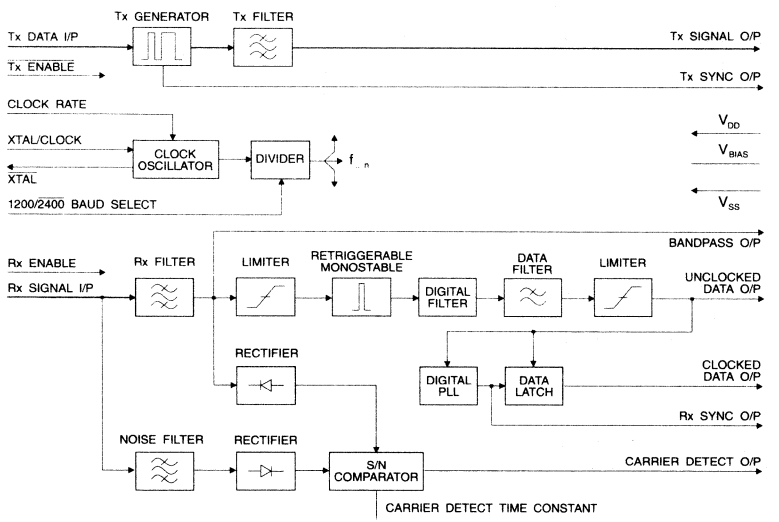



*Fig.1 Functional Block Diagram*

**FX469**

## Brief Description

The FX469 is a single-chip CMOS LSI circuit which operates as a full-duplex pin-selectable 1200 or 2400 baud FFSK Modem. The mark and space frequencies are 1200/1800 and 1200/2400Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point.

Employing a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) to provide baud-rate, transmit frequencies, and Rx and Tx synchronization, the transmitter and receiver operate entirely independently including individual section powersave functions.

The FX469 includes on-chip circuitry for Carrier Detect and Rx Clock Recovery, both of which are made available at output pins.

Rx, Tx and Carrier Detect paths each contain a bandpass filter to ensure the provision of optimum signal conditions both in the modem and for the Tx modulation circuitry.

The FX469 demonstrates a high sensitivity and good bit-error-rate under adverse signal conditions; the carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high-noise environments.

This low-power device requires few external components and is available in small outline (S.O.I.C) or quad plastic surface mount and cerdip DIL packages.

## Pin Number Function

| FX469 DW | FX469 J | FX469 LG/LS | Function |
|---|---|---|---|
| 1 | 1 | 1 | **Xtal/Clock:** The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. The selection of this frequency will affect the operational Data Rate of this device. Refer to Baud Selection information on the next page. Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast-reaction fuse). |
| 2 | 2 | 2 | **$\overline{\text{Xtal}}$:** Output of the on-chip inverter. |
| 3 | 3 | 3 | **Tx Sync O/P:** A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the FFSK signal (See Figure 4). |
| 4 | 5 | 5 | **Tx Signal O/P:** When the transmitter is enabled, this pin outputs the (140-step pseudo sinewave) FFSK signal (See Figure 4).<br>With the transmitter disabled, this output is set to a high-impedance state. |
| 5 | 6 | 7 | **Tx Data I/P:** Serial logic data to be transmitted is input to this pin. |
| 6 | 7 | 8 | **$\overline{\text{Tx Enable}}$:** A logic '0' will enable the transmitter (See Figure 4). A logic '1' at this input will put the transmitter into powersave whilst forcing "Tx Sync Out" to a logic '1' and "Tx Signal Out" to a high-impedance state. This pin is internally pulled to $V_{DD}$. |
| 7 | 8 | 9 | **Bandpass O/P:** The output of the Rx Bandpass Filter. This output impedance is typically 10kΩ and may require buffering prior to use. |
| 8 | 9 | 10 | **Rx Enable :** The control of the Rx function. The control of other outputs is given below. |
| 9 | 10 | 11 | **$V_{BIAS}$:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to $V_{SS}$ by a capacitor ($C_2$). See Figure 2.<br>This bias voltage is maintained under all powersave conditions. |
| 10 | 11 | 12 | **$V_{SS}$:** Negative supply rail (GND). |

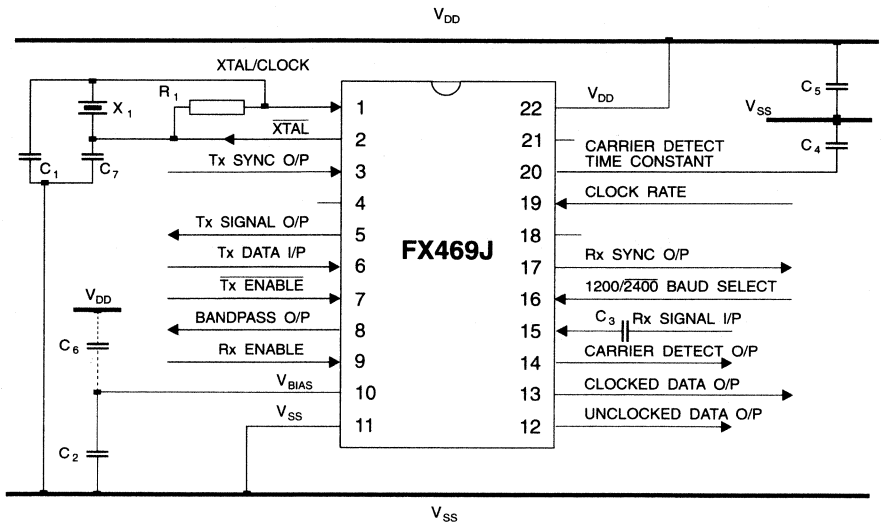
| Rx Enable | = | Rx Function | Clock Data O/P | Carrier Detect | Rx Sync Out |
|---|---|---|---|---|---|
| "1" | = | Enabled | Enabled | Enabled | Enabled |
| "0" | = | Powersave | "0" | "0" | "1" or "0" |

## Pin Number Function

| FX469 DW | FX469 J | FX469 LG/LS | Function |
|---|---|---|---|
| 11 | 12 | 13 | **Unclocked Data O/P:** The recovered asynchronous serial data output from the receiver. |
| 12 | 13 | 14 | **Clocked Data O/P:** The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "Rx Sync O/P", (See Figure 5). |
| 13 | 14 | 15 | **Carrier Detect O/P:** When an FFSK signal is being received this output is a logic '1'. |
| 14 | 15 | 16 | **Rx Signal I/P:** The FFSK signal input for the receiver. This input should be coupled via a capacitor, $C_3$. |
| 15 | 17 | 18 | **Rx Sync O/P:** A flywheel squarewave output. This clock will synchronize to incoming Rx FFSK data (See Figure 5). |
| 16 | 16 | 19 | **1200/$\overline{2400}$ Baud Select:** A logic '1' on this pin selects the 1200 baud option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one-and-a-half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 baud option. Tone frequencies are: one-half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pullup resistor. **Operational Data Rate Configurations** are illustrated in the table below. |
| 17 | 18 | 20 | Internally connected, leave open circuit. |
| 18 | 19 | 21 | **Clock Rate:** A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz). |
| 19 | 20 | 22 | **Carrier Detect Time Constant :** Part of the carrier detect integration function. The value of $C_4$ connected to this pin will affect the carrier detect response time and hence noise performance (See Figure 2, Note 3). |
| 20 | 22 | 24 | $V_{DD}$: Positive supply rail. A single 5-volt supply is required. |
| | 4, 21 | 4, 6, 17, 23 | No internal connection, do not use. |

| **Xtal/Clock Frequency** | **1.008MHz** | | **4.032MHz** | |
|---|---|---|---|---|
| **Clock Rate** pin | 0 | 0 | 1 | 1 |
| **1200/2400 Select** pin | 1 | 0 | 1 | 0 |
| **Baud Rate** | **1200** | **2400** | **1200** | **2400** |

# Application Information




| Component | Value | Tolerance |
|---|---|---|
| $R_1$ | 1.0MΩ | ±10% |
| $C_1$ | 33pF | |
| $C_2$ | 1.0µF | ±20% |
| $C_3$ | 0.1µF | |
| $C_4$ | 0.1µF | ±10% |
| $C_5$ | 1.0µF | ±20% |
| $C_6$ | 1.0µF | |
| $C_7$ | 33pF | |
| $X_1$ | 1.008MHz or 4.032MHz | See 'Clock-Rate' Pin |

*Fig.2 External Components*

**Notes**

1. $V_{BIAS}$ may be decoupled to $V_{SS}$ and $V_{DD}$ using $C_2$ and $C_6$ when input signals are referenced to the $V_{BIAS}$ pin. For input signals referenced to $V_{SS}$, decouple $V_{BIAS}$ to $V_{SS}$ using $C_2$ only.
2. Use $C_5$ when input signals are referenced to $V_{SS}$, to decouple $V_{DD}$.
3. The value of $C_4$ determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. $C_4$ may be varied to trade-off response time for noise immunity.
4. $C_7$ reduces Xtal voltage overshoot. Refer to CML Xtal Application Note D/XT/1 April 1986.

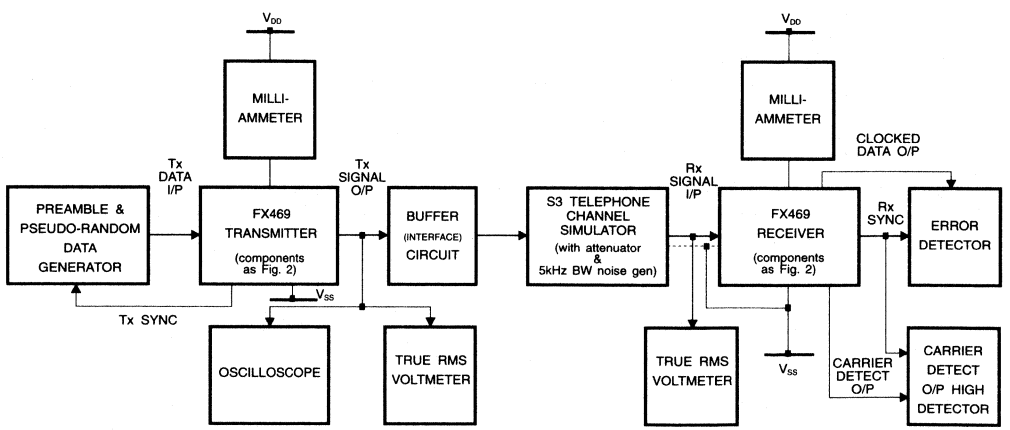



*Fig.3 Suggested FX469 Test Set-Up*

## Application Information .....

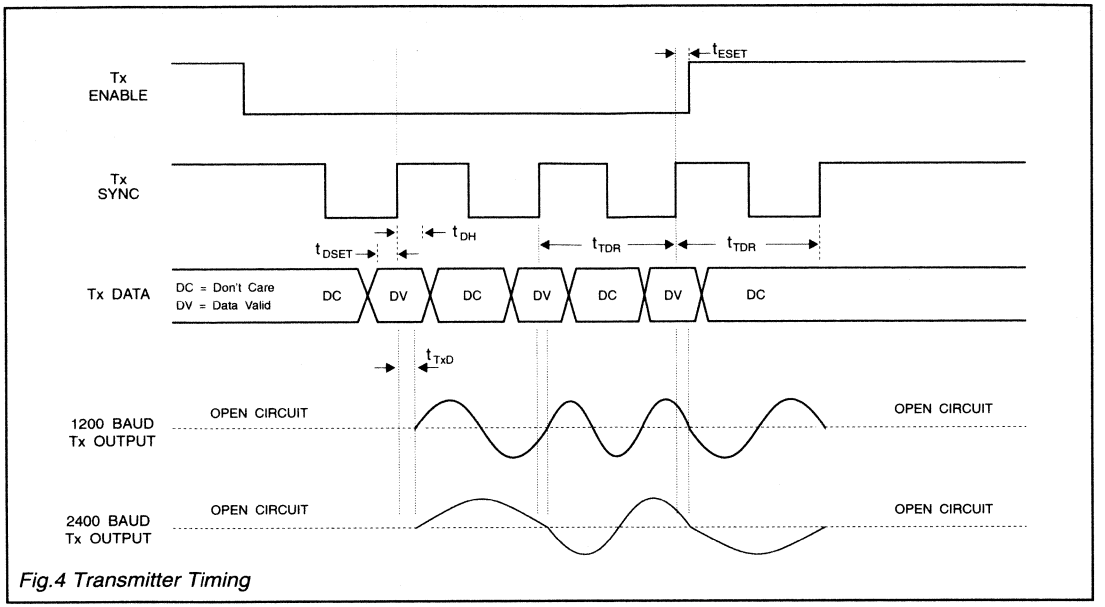



*Fig.4 Transmitter Timing*

| Characteristics | | Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Tx Delay, Signal to Disable Time | $t_{ESET}$ | 3 | 2.0 | - | 800 | µs |
| Data Set-Up Time | $t_{DSET}$ | 1 | 2.0 | - | - | µs |
| Data Hold Time | $t_{DH}$ | | 2.0 | - | - | µs |
| Tx Delay to O/P Time | $t_{TxD}$ | | - | 1.2 | - | µs |
| Tx Data Rate Period | $t_{TDR}$ | 3 | - | 833 | - | µs |
| Rx Data Rate Period | $t_{RDR}$ | 3 | 800 | - | 865 | µs |
| Undetermined State | | | - | - | 2.0 | µs |
| Internal Rx Delay | $t_{ID}$ | | - | 1.5 | - | ms |

1. Consider the Xtal/Clock tolerance.
2. All Tx timings are related to the Tx Sync Output.
3. 1200 baud example.

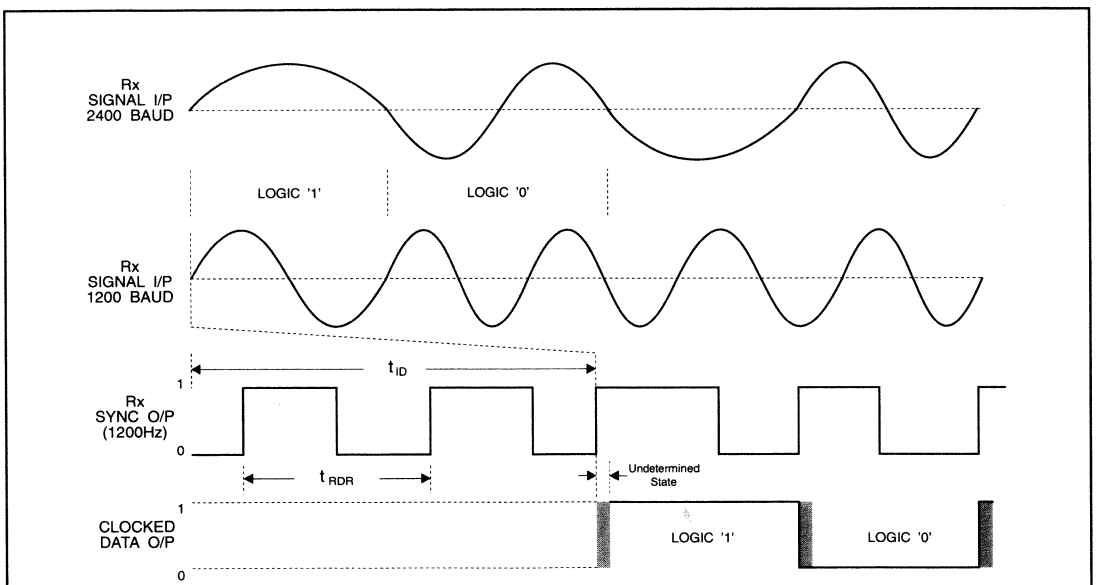



*Fig.5 Rx Timing Diagram*

## Application Information .....

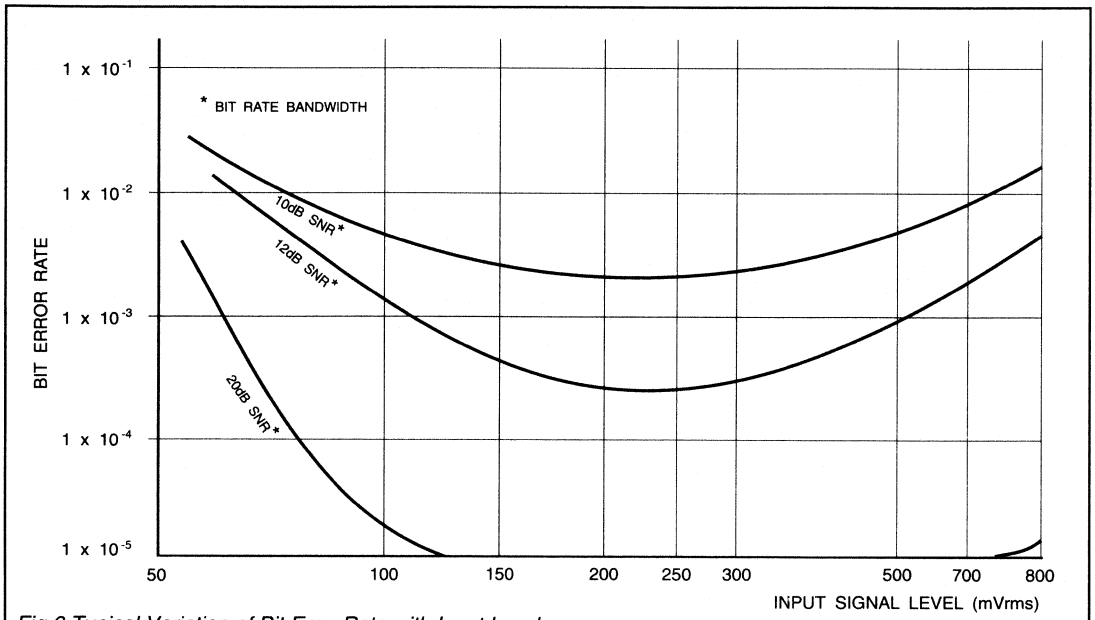



*Fig.6 Typical Variation of Bit Error Rate with Input Level*

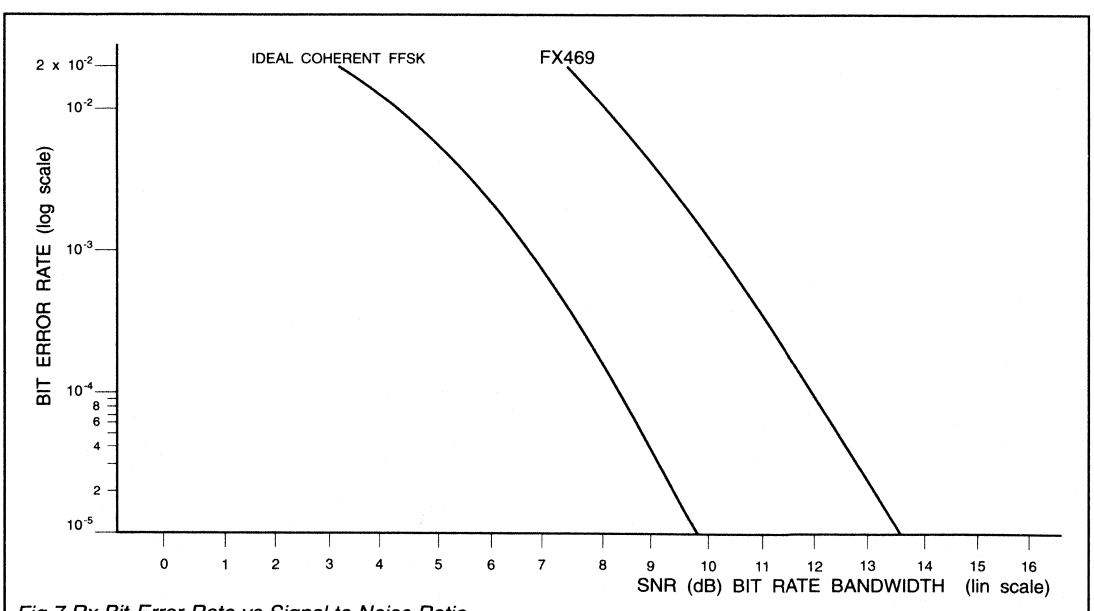



*Fig.7 Rx Bit-Error-Rate vs Signal-to-Noise Ratio*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX469DW/LG/LS** | -30°C to +70°C (plastic) |
| | **FX469J** | -30°C to +85°C (cerdip) |
| Storage temperature range: | **FX469DW/LG/LS** | -40°C to +85°C (plastic) |
| | **FX469J** | -55°C to +125°C (cerdip) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Audio Level 0dB ref: = 300mVrms. Xtal/Clock = 4.032MHz.
Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth

| Characteristics | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Values** | | | | | | |
| Supply Voltage | | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | Rx Enabled, Tx Disabled | | - | 3.6 | - | mA |
| | Rx and Tx Enabled | | - | 4.5 | - | mA |
| | Rx and Tx Disabled | | - | 650 | - | µA |
| Logic '1' Level | | 1 | 4.0 | - | - | V |
| Logic '0' Level | | 1 | - | - | 1.0 | V |
| Digital Output Impedance | | | - | 4.0 | - | kΩ |
| Analogue and Digital Input Impedance | | | 100 | - | - | kΩ |
| Tx Output Impedance | | | - | 10.0 | - | kΩ |
| On-Chip Xtal Oscillator | | | | | | |
| | $R_{IN}$ | | 10.0 | - | - | MΩ |
| | $R_{OUT}$ | | - | 10.0 | - | kΩ |
| Inverter d.c. Voltage Gain | | | - | 10.0 | - | V/V |
| Gain Bandwidth Product | | | - | 10.0 | - | MHz |
| Xtal Frequency | | 2 | - | 1.008 or 4.032 | - | MHz |
| **Dynamic Values** | | | | | | |
| **Receiver** | | | | | | |
| Signal Input Dynamic Range | SNR = 50dB | 3, 4 | 100 | 230 | 1000 | mVrms |
| Bit Error Rate | SNR = 12dB | 4 | - | 7.0 | - | $10^{-4}$ |
| | SNR = 20dB | 4 | - | 1.0 | - | $10^{-8}$ |
| **Receiver Synchronization** | **SNR = 12dB** | 7 | | | | |
| Probability of Bit 8 Being Correct | | | - | 0.99 | - | |
| Probability of Bit 16 Being Correct | | | - | 0.995 | - | |
| **Carrier Detect** | | 5 | | | | |
| Sensitivity | | 7, 8 | - | - | 150 | mVrms |
| Probabilty of C.D. Being High | | | | | | |
| After Bit 8 (1200 Baud) | SNR = 12dB | 5, 9 | - | 0.98 | - | |
| After Bit 16 | SNR = 12dB | 5, 9 | | 0.995 | | |
| 0dB Noise | No Signal | 9 | | 0.05 | | |
| **Transmitter Output** | | | | | | |
| Tx Output Level | | | - | 775 | - | mVrms |
| Output Level Variation | | | | | | |
| 1200/1800Hz or 1200/2400Hz | | | 0 | - | ±1.0 | dB |
| Output Distortion | | | - | 3.0 | 5.0 | % |
| 3rd Harmonic Distortion | | | - | 2.0 | 3.0 | % |
| Logic '1' Carrier Frequency | 1200 Baud | 6 | - | 1200 | - | Hz |
| | 2400 Baud | 6 | - | 1200 | - | Hz |
| Logic '0' Carrier Frequency | 1200 Baud | 6 | - | 1800 | - | Hz |
| | 2400 Baud | 6 | - | 2400 | - | Hz |
| Isochronous Distortion | | | | | | |
| 1200Hz - 1800Hz | | | - | 25.0 | 40.0 | µs |
| 1800Hz - 1200Hz | | | - | 20.0 | 40.0 | µs |
| 1200Hz - 2400Hz/2400Hz - 1200Hz | | | - | 15.0 | - | µs |

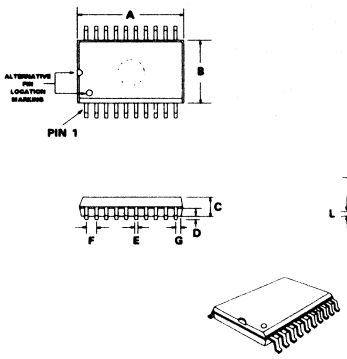
**Notes**

1. With reference to $V_{DD}$ = 5.0 volts.
2. Xtal frequency (ref. Clock Rate pin), type and tolerance depends upon system requirements.
3. See Figure 5 (variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise in the Bit-Rate Bandwidth.
5. See Figure 2.
6. Dependent upon Xtal tolerance.
7. 10101010101 ...01 pattern.
8. Measured with a 150mVrms input signal (no noise).
9. Reference (0dB) level for C.D. probability measurements is 230mVrms.

## Package Outlines

The FX469DW, the S.O.I.C. package is shown in Figure 8, the 'J' version in Figure 9, the 'LG' version in Figure 10 and the 'LS' version in Figure 11.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top (indent side).

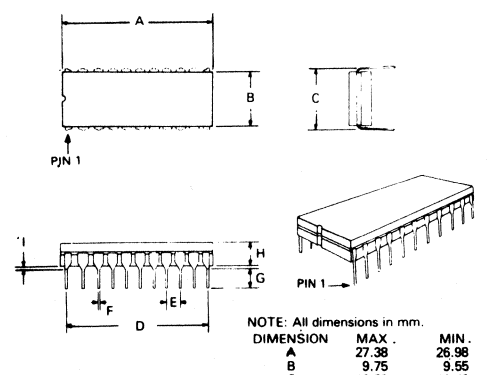
*Fig.8* ***FX469DW*** *S.O.I.C. Package*




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 12.85 | | 12.62 | G | | 0.66 | |
| B | 7.59 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

*Fig.9* ***FX469J*** *Package*



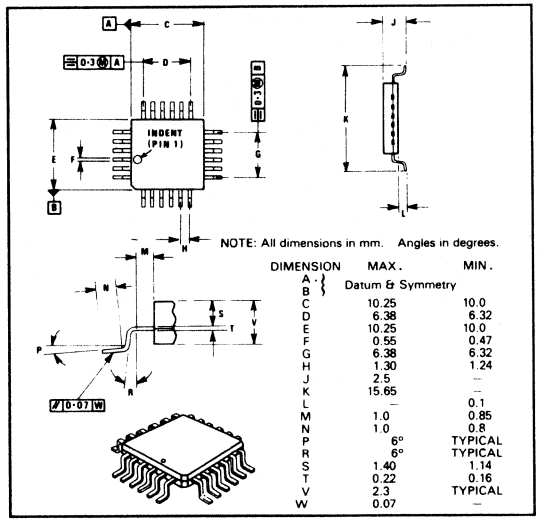

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 | TYPICAL |
| F | 0.46 | DIMENSION |
| G | 4.30 | 4.10 |
| H | 4.27 | 3.99 |
| I | 1.4 | TYPICAL |

## Handling Precautions

The FX469 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

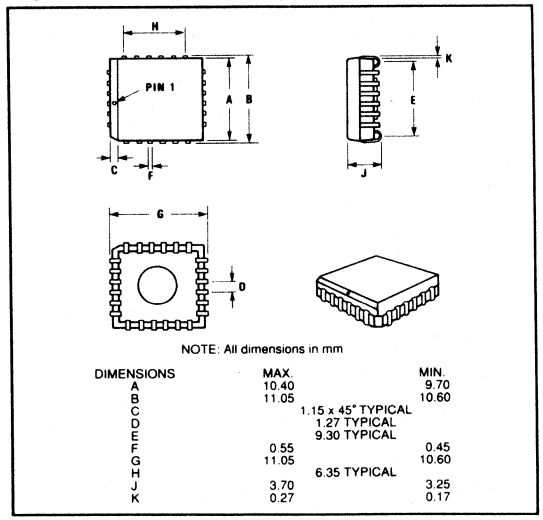
*Fig.10* ***FX469LG*** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | — |
| K | 15.65 | — |
| L | — | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | — |

*Fig.11* ***FX469LS*** *Package*




NOTE: All dimensions in mm

| DIMENSIONS | MAX. | MIN. |
|---|---|---|
| A | 10.40 | 9.70 |
| B | 11.05 | 10.60 |
| C | 1.15 x 45° TYPICAL | |
| D | 1.27 TYPICAL | |
| E | 9.30 TYPICAL | |
| F | 0.55 | 0.45 |
| G | 11.05 | 10.60 |
| H | 6.35 TYPICAL | |
| J | 3.70 | 3.25 |
| K | 0.27 | 0.17 |

## Ordering Information

| | |
|---|---|
| **FX469DW** | 20-pin surface mount S.O.I.C. |
| **FX469J** | 22-pin cerdip DIL |
| **FX469LG** | 24-pin quad plastic encapsulated bent and cropped |
| **FX469LS** | 24-lead plastic leaded chip carrier |

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX489 GMSK Modem

Publication D/489/3 February 1993
Provisional Issue

## Features

- Full-Duplex Gaussian Minimum Shift Keying
- Selectable BT (0.3 or 0.5)
- Meets RAM - MOBITEX Specification
- Data Rates From 4000bits/s to 19200bits/s
- Serial Rx and Tx Data Interfaces
- Rx and Tx Data Clock Generation
- Rx Signal Tracking Controls
- Rx S/N Indication
- Separate Rx and Tx Powersave Inputs
- Wireless Modem, Radio Telemetry and Data Terminal Applications

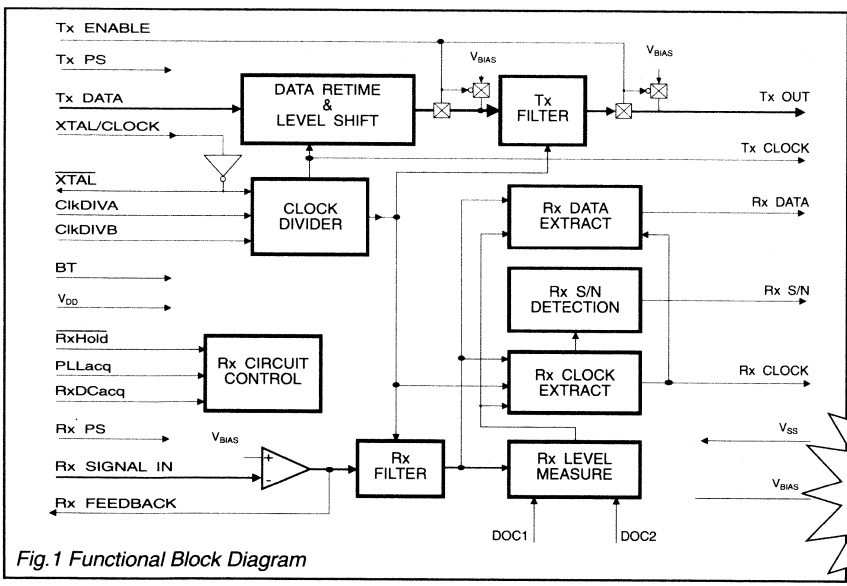



*Fig.1 Functional Block Diagram*

**FX489**

NEW 40kbps Modem **FX589** Pin/Function Compatible

## Brief Description

The FX489 is a single-chip modem employing Gaussian Minimum Shift Keying (GMSK) modulation. Having a pin selectable BT of 0.3 or 0.5, the FX489 may be employed at data rates of between 4,000bits/s and 19,200bits/s; for use in FM radio-data links and data communication systems conforming to DOC and FCC spectrum limitations for 12.5kHz and 8,000 baud at a BT of 0.3, and 12.5, 25.0, and 50.kHz channel spacing and data rates of 4800, 9600 and 19,200 baud respectively at a BT of 0.5.

The Rx and Tx digital data interfaces are bit-serial and synchronised to Rx and Tx data clocks generated by the modem. Separate Rx and Tx Powersave/Enable inputs allow for full- or half-duplex operation.

Rx input levels can be set by a suitable a.c. and d.c. level adjusting circuit built, with external components, around an on-chip Rx input amplifier.

Acquisition, lock and hold of Rx data signals is made easier and faster by the use of Rx Control Inputs to clamp, detect and/or hold input data levels and can be set by the µProcessor as required.

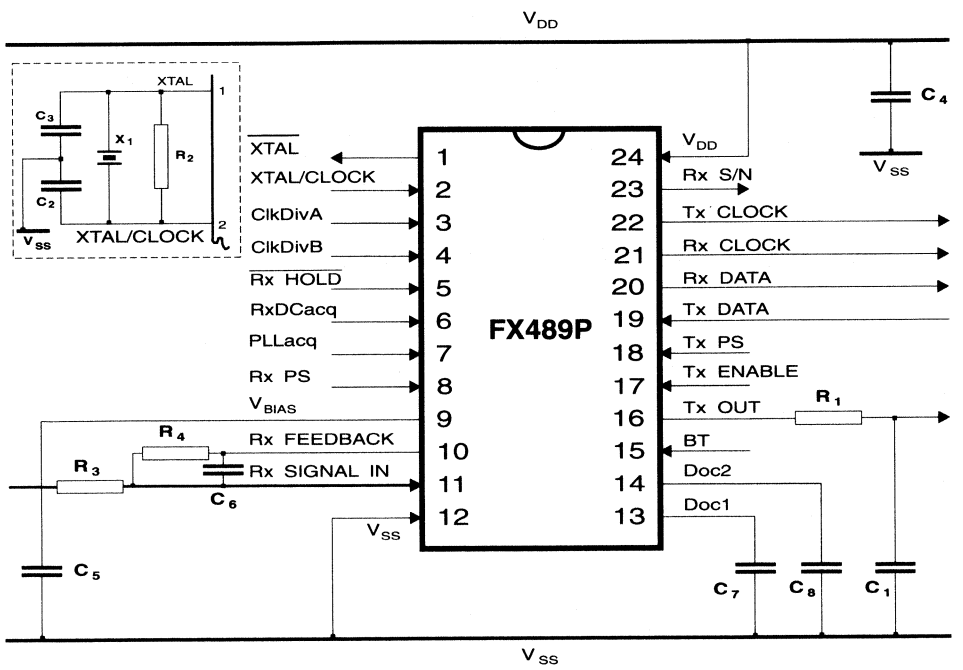
Indication is available, from the Rx S/N output, as to the quality of the received signal.

The FX489, a low-power CMOS microcircuit, is available in both 24-pin plastic Small Outline (S.O.I.C) and DIL packages.

| Pin Number FX489DW FX489P | Function |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. |
| 2 | **Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock ($f_{XTAL}$) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the "$\overline{\text{Xtal}}$" pin left unconnected. Note that operation of the FX489 without a suitable Xtal or clock input may cause device damage. |
| 3 | **ClkDivA:** Two logic level inputs that control the internal clock divider and hence the transmit and receive data rate. See Table 1. |
| 4 | **ClkDivB:** |
| 5 | **$\overline{\text{Rx Hold}}$:** A logic "0" applied to this input will 'freeze' the Clock Extraction and Level Measurement circuits unless they are in 'acquire' mode. |
| 6 | **RXDCacq:** A logic "1" applied to this input will set the Rx Level Measurement circuitry to the 'acquire' mode. |
| 7 | **PLLacq:** A logic "1" applied to this input will set the Rx Clock Extraction circuitry to 'acquire' mode (see Table 2). |
| 8 | **Rx PS:** A logic "1" applied to this input will powersave all receive circuits except for "Rx Clock " output (which will continue at the set bit-rate) and cause the "Rx Data" and "Rx S/N" outputs to go to a logic "0". |
| 9 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to $V_{SS}$ by a capacitor mounted close to the pin. |
| 10 | **Rx Feedback:** The output of the Rx Input Amplifier/The input to the Rx Filter. |
| 11 | **Rx Signal In:** The input to Rx input amplifier. |
| 12 | **$V_{SS}$:** Negative supply rail. Signal ground. |

| Pin Number FX489DW FX489P | Function |
|---|---|
| 13 | **Doc1:** Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to $V_{SS}$. |
| 14 | **Doc2:** |
| 15 | **BT:** A logic level to select the modem 'BT' (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic "1" sets the modem to a BT of 0.5, a logic "0" to a BT of 0.3. |
| 16 | **Tx Out:** The Tx signal output from the FX489 GMSK Modem. |
| 17 | **Tx Enable:** A logic "1" applied to this input enables the transmit data path through the Tx Filter to the "Tx Out pin". A logic "0" will put the "Tx Out" pin to $V_{BIAS}$ via a high impedance. |
| 18 | **Tx PS:** A logic "1" applied to this input will powersave all transmit circuits except for the Tx Clock. |
| 19 | **Tx Data:** The logic level input for the data to be transmitted. This data should be synchronous with the "Tx Clock". |
| 20 | **Rx Data:** A logic level output carrying the received data, synchronous with the "Rx Clock". |
| 21 | **Rx Clock:** A logic level clock output at the received data bit-rate. |
| 22 | **Tx Clock:** A logic level clock output at the transmit-data rate. |
| 23 | **Rx S/N:** A logic level output which may be used as an indication of the quality of the received signal. |
| 24 | **$V_{DD}$:** Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to $V_{SS}$ by a capacitor mounted close to the pin. |

# Application Information




**External Components**

| Component | Value | Tolerance | Component | Value | Tolerance |
|---|---|---|---|---|---|
| $R_1$ | Note 1 | ±5% | $C_4$ | 100nF | ±20% |
| $R_2$ | 1.0MΩ | ±10% | $C_5$ | 1.0µF | ±20% |
| $R_3$ | Note 2 | ±10% | $C_6$ | 22.0pF | ±20% |
| $R_4$ | 100kΩ | ±10% | $C_7$ | 15.0nF | ±20% |
| $C_1$ | Note 1 | ±10% | $C_8$ | 15.0nF | ±20% |
| $C_2$ | 33.0pF | ±20% | $X_1$ | Note 3 | |
| $C_3$ | 33.0pF | ±20% | | | |

*Fig.2 External Components*

**Notes**

1. The RC network formed by $R_1$ and $C_1$ is required between the Tx Out pin and the input to the modulator. This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor $C_1$ should be positioned to give maximum attenuation of high-frequency noise into the modulator. The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:
   BT of 0.3 = 0.34/bit rate (bits/second)
   BT of 0.5 = 0.22/bit rate (bits/second)
   - with suitable values for common bit rates being:

| | | $R_1$ | $C_1$ |
|---|---|---|---|
| 8000 bits/sec | BT = 0.3 | 91.0kΩ | 470pF |
| 4800 bits/sec | BT = 0.5 | 100kΩ | 470pF |
| 9600 bits/sec | BT = 0.5 | 47.0kΩ | 470pF |

   NOTE that in all cases, the value of $R_1$ should be not less than 47.0kΩ and the calculated value of $C_1$ includes calculated parasitic (circuit) capacitances.

2. $R_3$, $R_4$ and $C_6$ form the gain components for the Rx Input signal.
   $R_3$ should be chosen as required by the signal input level.

3. The FX489 can operate correctly with Xtal/Clock frequencies as detailed in Table 1.
   Operation of this device without a Xtal or Clock input may cause device damage.

## Application Information .....

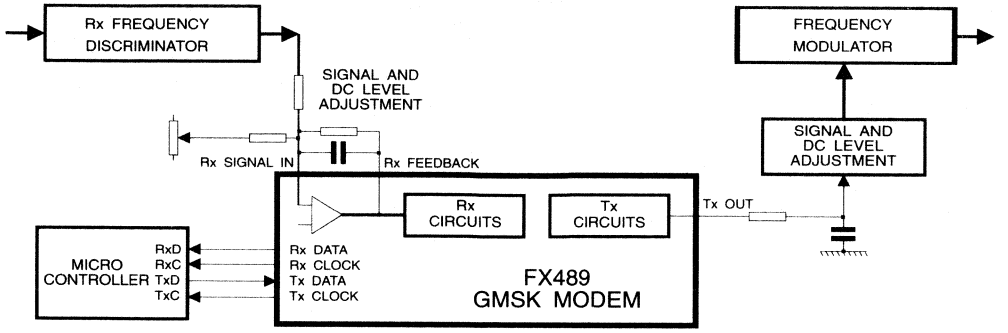



*Fig.3 External Signal Paths*

### Clock Oscillator and Dividers

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or be derived from an external source.

The division ratio is controlled by the logic level inputs on the ClkDivA/B pins, and is shown in the table below - together with an indication of how various 'standard' data rates may be derived from common µP Xtal frequencies.

| ***Note** that device operation is not guaranteed or specified above 19,200 bits/s or below 4,000 bits/s.* | | | **Xtal/Clock Frequency (MHz)** | | | |
|---|---|---|---|---|---|---|
| | | | 4.096 [12.288/3] | 4.9152 | 2.048 [6.144/3] | 2.4576 [12.288/5] |
| **ClkDiv A** | **ClkDiv B** | **Division ratio Xtal Freq/ Data Rate** | **Data Rate (bps)** | | | |
| 0 | 0 | 128 | | | 16000 | 19200 |
| 0 | 1 | 256 | 16000 | 19200 | 8000 | 9600 |
| 1 | 0 | 512 | 8000 | 9600 | 4000 | 4800 |
| 1 | 1 | 1024 | 4000 | 4800 | | |

*Table 1 Clock/Data Rates*

### Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index will be required.

To achieve optimum channel utilization, (eg. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

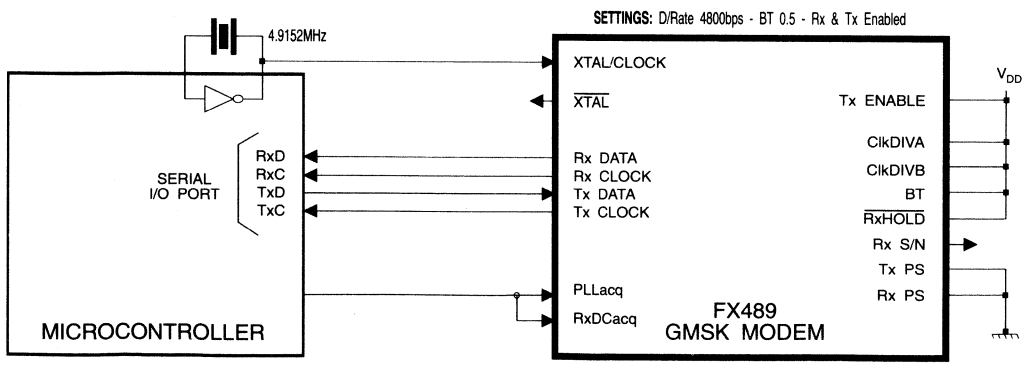



*Fig.4 Minimum µController System Connections*

# Application Information .....

## Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide d.c. level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the FX489's Rx Filter via a suitable gain and d.c. level adjusting circuit. This gain circuit can be built, with external components, around the on-chip Rx Input Amplifier, with the gain set so that the signal level at the Rx Feedback pin is nominally 1-volt peak-to-peak centred around $V_{BIAS}$ when receiving a continuous "1111000011110000 .." data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic "0" at the Rx Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors. One of which measures the amplitude of the 'positive' parts of the received signal; The other measures the amplitude of the 'negative' portions. External capacitors are used by these detectors, via the Doc 1/2 pins, to form voltage- 'hold' or 'integrator' circuits. Results of the two measurements are then processed to establish the optimum d.c. level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude, BT and any d.c. offset present.

## Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 2, by logic level inputs applied to the 'PLLacq,' 'Rx Hold' and 'RxDCacq' pins to suit a particular application, or to cope with changing reception conditions.

With reference to Figure 5, the Rx Mode Control diagram. In general, a data transmission will begin with a preamble of, for example, "1100110011001100," to allow the receive modem to establish timing- and level-lock as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the 'RxDCacq' and 'PLLacq' inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The 'Rx Hold' input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the 'Rx Hold' input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the 'RxDCacq' to a logic "1" for 10 to 20 bit periods.

'Rx Hold' has no effect on the Level Measuring circuits while 'RxDCacq' is at a logic "1," and has no effect on the PLL while 'PLLacq' is at a logic "1."

A logic "0" on 'Rx Hold' does not disable the 'Rx Clock' output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

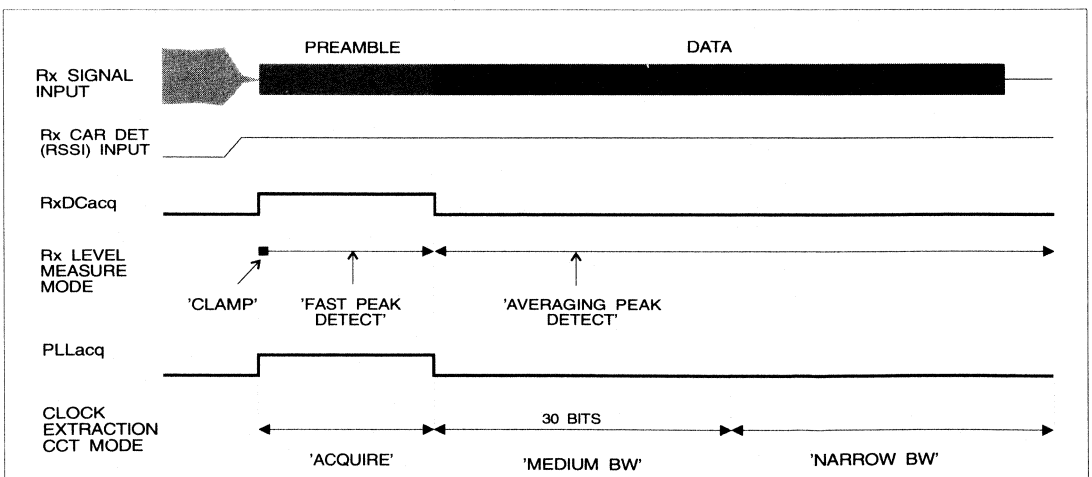



*Fig.5 Rx Mode Control Diagram*

## Application Information .....

| PLLacq | $\overline{\text{Rx Hold}}$ | PLL Action |
|---|---|---|
| "1" | X | **Acquire:** Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. The Acquire mode will operate as long as PLLacq is a logic "1". |
| "1" to "0" | "1" | **Medium Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the $\overline{\text{Rx Hold}}$ input is a logic "1". |
| "0" | "1" | **Narrow Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the $\overline{\text{Rx Hold}}$ Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation for instance). |
| "0" | "0" | **Hold:** The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods. |
| **RxDCacq** | **$\overline{\text{Rx Hold}}$** | **Rx Level Measure Action** |
| "0" to "1" | X | **Clamp:** Operates for one bit-time after a "0" to "1" transition of the RxDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and $V_{BIAS}$, with the charge time-constant being of the order of 0.5bit-time. |
| "1" | X | **Fast Peak Detect:** The voltage detectors act as peak-detectors, one capacitor is used to capture the 'positive'-going signal peaks of the Rx Filter output signal and the other capturing the 'negative'-going peaks. The detectors operate in this mode whenever the RxDCacq input is at a logic "1," except for the initial 1-bit Clamp-mode time. |
| "0" | "1" | **Averaging Peak Detect:** Provides a slower but more accurate measurement of the signal peak amplitudes. |
| "0" | "0" | **Hold:** The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000bits] towards $V_{BIAS}$). |

*Table 2 PLL and Rx Level Measurement Operational Modes*

### Rx Clock Extraction

Synchronized by a phased locked loop (PLL) circuit to zero-crossings of the incoming data, the 'Rx Clock Extraction' circuitry controls the 'Rx Clock' output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the 'Rx Circuit Control' inputs PLLacq and $\overline{\text{Rx Hold}}$ to operate in one of four PLL modes as described in Table 2.

### Rx Data Extraction

The 'Rx Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the output of the Rx Filter in the middle of each bit-period, and comparing the sampled voltage against a threshold derived from the 'Level Measuring' circuit. This threshold is varied on a bit-by-bit basis to compensate for intersymbol interference depending on the chosen BT. The extracted data is output from the 'Rx Data' pin, and should be sampled externally on the rising edge of the 'Rx Clock.'

### Rx S/N Detection

The 'Rx S/N Detector' system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the 'Rx S/N' pin.

By monitoring, and averaging, this output it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal.

# Application Information .....

## Bit Error Rate Performance

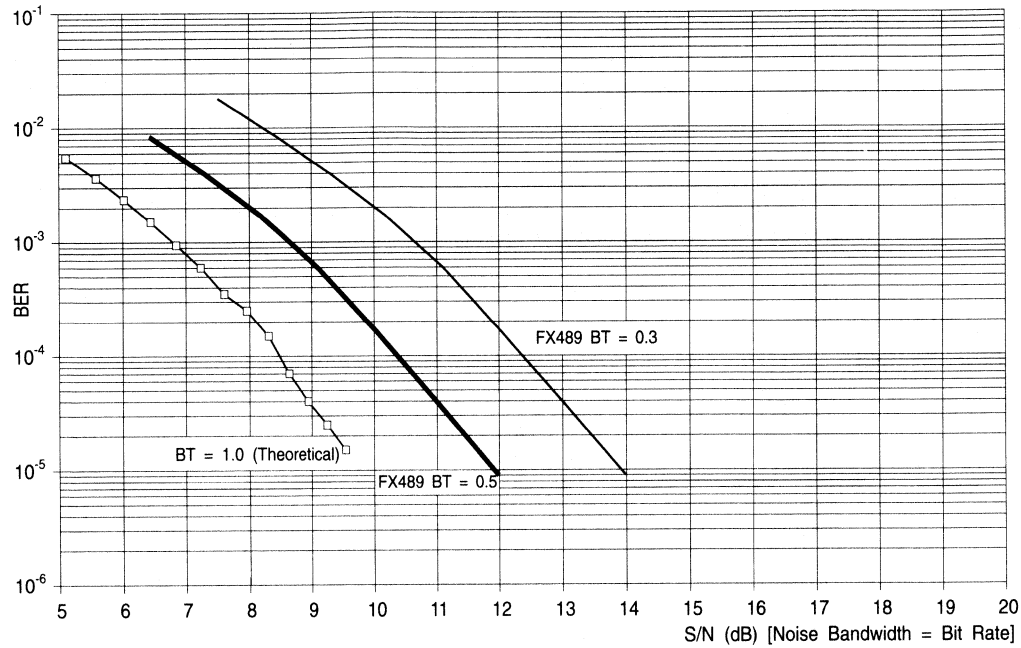



*Fig. 6 Typical Bit-Error-Rate Performance*

## Rx Signal Quality

Figure 7 shows, diagramatically, the effect of input Rx signal quality on the "Rx S/N" output.

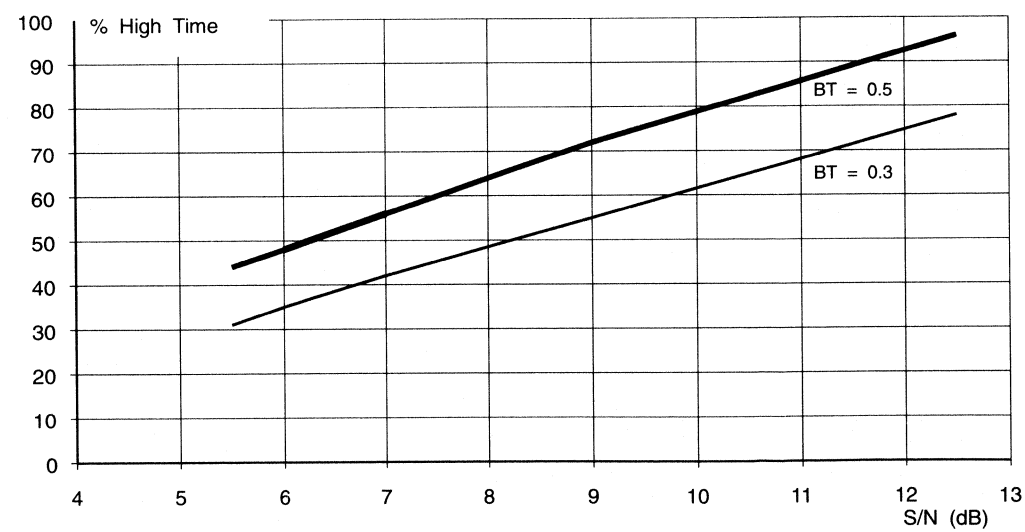



*Fig.7 Typical Rx S/N Output 'High-Time' (%) vs Input S/N*

# Application Information .....

## Tx Signal Path Description

The binary data applied to the 'Tx Data' input is retimed within the chip on each rising edge of the 'Tx Clock' and then converted to a 1-volt peak-to-peak binary signal centred about $V_{BIAS}$.

If the 'Tx Enable' input is 'high,' then this internal binary signal will be connected to the input of the lowpass Tx Filter, and the output of the filter connected to the 'Tx Out' pin.

| Tx Enable | Tx Filter Input | Tx Out Pin |
|---|---|---|
| '1' (high) | 1 volt p-p Data In | Filtered Data |
| "0" (low) | $V_{BIAS}$ | $V_{BIAS}$ via 500kΩ |

A 'low' input to the 'Tx Enable' will connect the input of the Tx Filter to $V_{BIAS}$, and disconnect the 'Tx Out' pin from the filter, connecting it instead to $V_{BIAS}$ through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimise amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the FX489 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note that an external RC network is required between the 'Tx Out' pin and the input to the Frequency Modulator (see Figures 2 and 3). This network, which can form part of any d.c. level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering, and the ground connection to the capacitor $C_1$ should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

BT of 0.3 = 0.34/bit rate (bits/second)
BT of 0.5 = 0.22/bit rate (bits/second)
with suitable values for common bit rates being:

| | R | C |
|---|---|---|
| 8000 bits/sec, BT = 0.3 | 91.0kΩ | 470pF |
| 4800 bits/sec, BT = 0.5 | 100kΩ | 470pF |
| 9600 bits/sec, BT = 0.5 | 47.0kΩ | 470pF |

The signal at 'Tx Out' is centred around $V_{BIAS}$, going positive for logic "1" (high) level inputs to the 'Tx Data' input and negative for logic "0" (low) inputs.

When the transmit circuits are put into a 'powersave' mode (by a logic "1" to the 'Tx PS' pin) the output voltage of the Tx Filter will go to $V_{SS}$.
When power is subsequently restored to the Tx Filter, its output will take several bit-times to settle. The 'Tx Enable' input can be used to prevent these abnormal voltages from appearing at the 'Tx Out' pin.

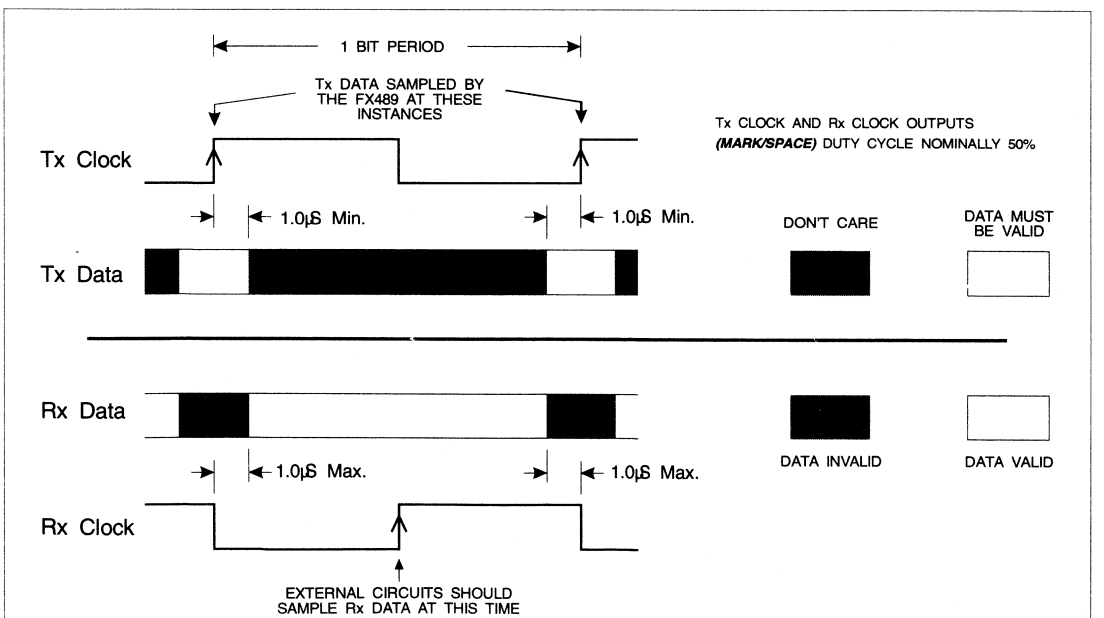



*Fig.8 Rx and Tx Clock Data Timings*

## Application Information .....

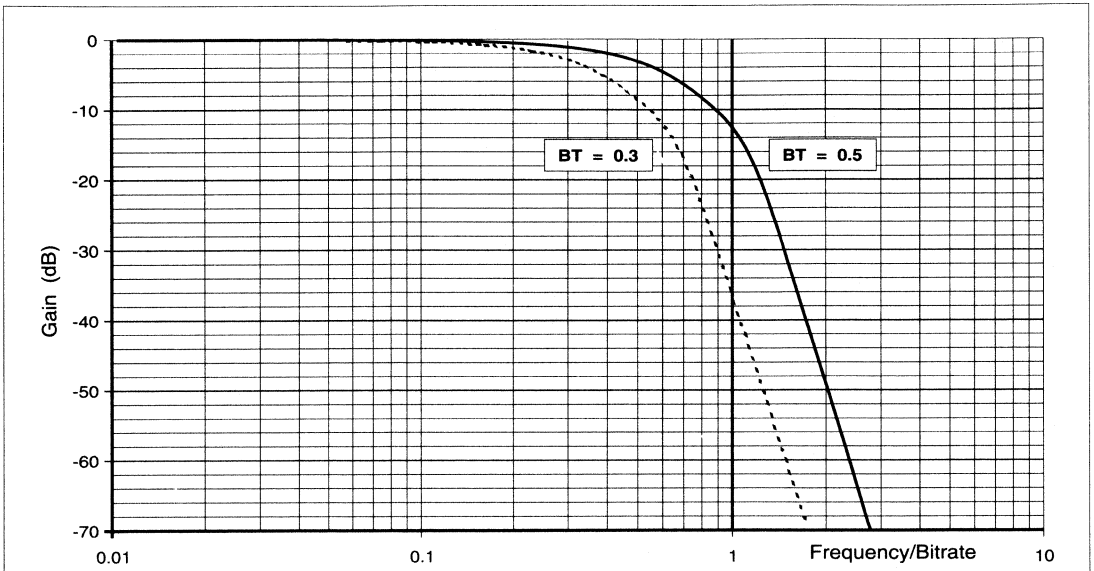



*Fig.9 Tx Filter Response*

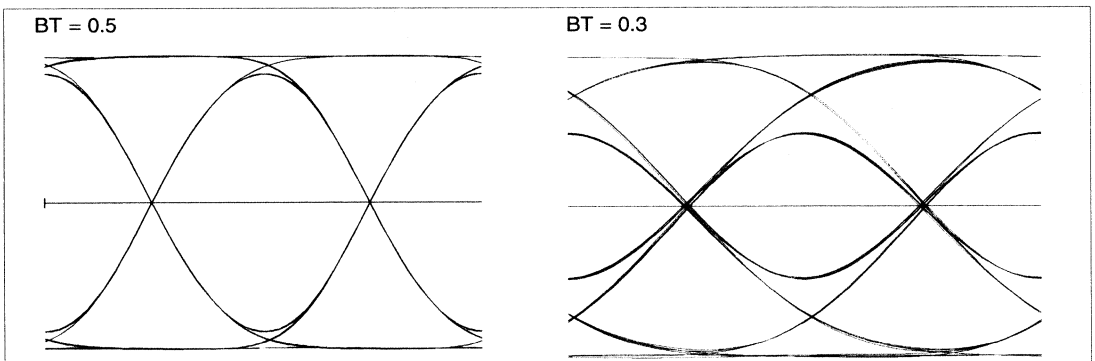



*Fig.10 Typical Transmit Eye Patterns*

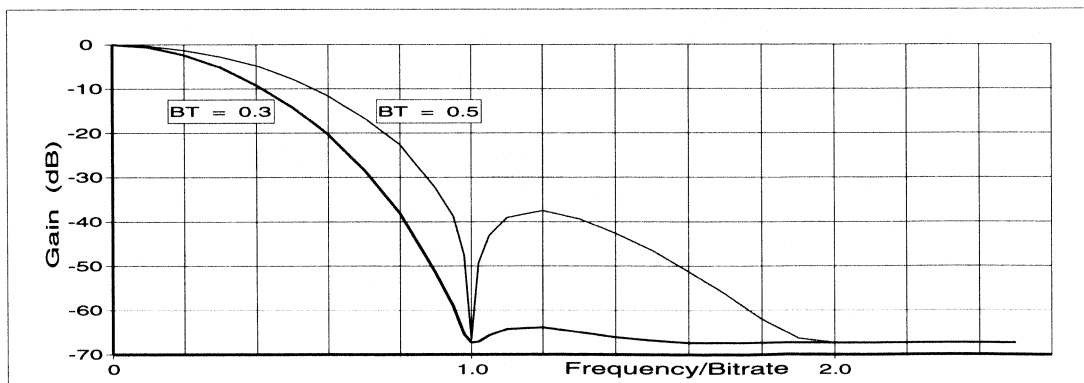



*Fig.11 Tx Output Spectrum (Random Data)*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | |
|---|---|
| Supply voltage | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | +/- 30mA |
| (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | 800mW Max. |
| Derating | 10mW/°C |
| Operating temperature range: **FX489DW/P** | -40°C to +85°C |
| Storage temperature range: **FX489DW/P** | -40°C to +85°C |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Xtal/Clock Frequency = 4.096MHz. Data Rate = 8000 bits/sec.
Noise Bandwidth = Bit Rate

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage ($V_{DD}$) | | 4.5 | 5.0 | 5.5 | V |
| Supply Current **Tx PS Rx PS** | 1 | | | | |
| 1 1 | | - | 1.0 | - | mA |
| 0 1 | | - | 3.0 | - | mA |
| 1 0 | | - | 4.0 | - | mA |
| 0 0 | | - | 7.0 | - | mA |
| Input Logic Levels | | | | | |
| Logic "1" | | 3.5 | - | - | V |
| Logic "0" | | - | - | 1.5 | V |
| Logic Input Current | 2 | -5.0 | - | 5.0 | µA |
| Logic "1"Output Level at IOH = -120µA | | 4.6 | - | - | V |
| Logic "0"Output Level at IOL = 120µA | | - | - | 0.4 | V |
| Rx, Tx Data Rate | | 4000 | | 19200 | bits/sec |
| **Transmit Parameters** | | | | | |
| Tx OUT, Output Impedance | 3 | - | 1.0 | - | kΩ |
| Tx OUT, Level | 4 | 0.8 | 1.0 | 1.2 | V p-p |
| Tx Data Delay (BT = 0.3) | 5 | - | 2.0 | 2.5 | bit-periods |
| (BT = 0.5) | 5 | - | 1.5 | 2.0 | bit-periods |
| Tx PS to Output-Stable Time | 6 | - | 4.0 | - | bit-periods |
| **Receive Parameters** | | | | | |
| Rx Amplifier - | | | | | |
| Input Impedance | | 1.0 | - | - | MΩ |
| Output Impedance | 7 | - | 10.0 | - | kΩ |
| Voltage Gain | | - | 50.0 | - | dB |
| Rx Filter Signal Input Level | 8 | 0.7 | 1.0 | 1.3 | V p-p |
| Rx Time Delay | 9 | - | - | 3.0 | bit-periods |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | - | - | MΩ |
| $R_{OUT}$ | | 5.0 | - | 15.0 | kΩ |
| Voltage Gain | | - | 15.0 | - | dB |
| Xtal/Clock Frequency | | 1.0 | – | 5.0 | MHz |
| "High" Pulse Width | 10 | 80.0 | - | - | ns |
| "Low" Pulse Width | 10 | 80.0 | - | - | ns |

**Notes**

1. Not including current drawn from the FX489 pins by external circuitry. See Absolute Maximum Ratings.
2. For $V_{IN}$ in the range $V_{SS}$ to $V_{DD}$.
3. For a load of 10kΩ or greater. Tx PS input at logic "0"; Tx Enable = "1".
4. Data pattern of "1111000011110000 .."
5. Measured between the rising edge of 'Tx Clock' and the centre of the corresponding bit at 'Tx Out.'
6. Time between the falling edge of 'Tx PS' and the 'Tx Out' voltage stabilising to normal output levels.
7. For a load of 10kΩ or greater. Rx PS input at logic "0".
8. For optimum performance, measured at the 'Rx Feedback' pin for a "1111000011110000 ..." pattern.
9. Measured between the centre of bit at 'Rx Signal In' and corresponding rising edge of the 'Rx Clock'.
10. Timing for an external clock input to the Xtal/Clock pin.

## Package Outlines

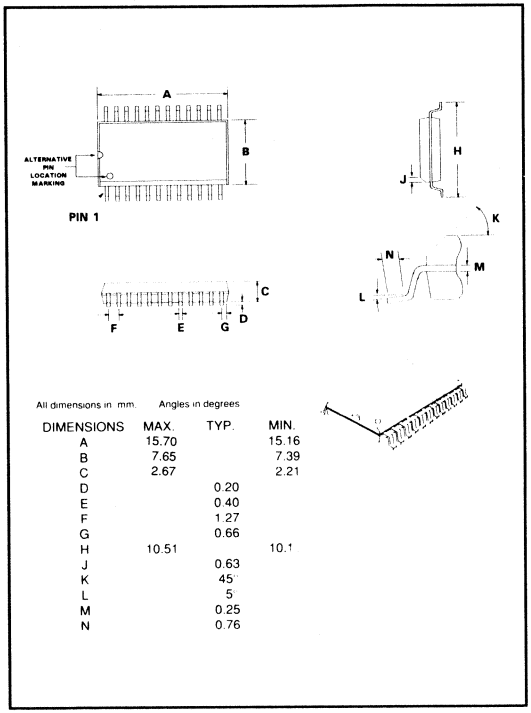
The FX489DW, the Small Outline Integrated Circuit (S.O.I.C.) package is shown in Figure 12 and the 'P' plastic version in Figure 13.

Pin 1 identification marking is shown on the relevant diagram and pins on both package styles number anti-clockwise when viewed from the top (marked side).

## Handling Precautions

The FX489 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

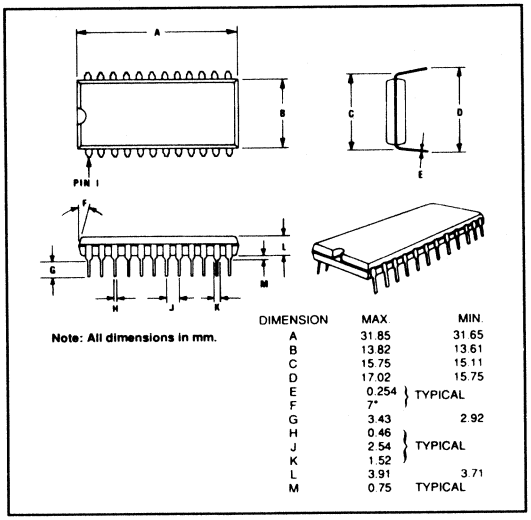
*Fig.12* ***FX489DW 24-pin S.O.I.C. Package***




All dimensions in mm. Angles in degrees

| DIMENSIONS | MAX. | TYP. | MIN. |
|---|---|---|---|
| A | 15.70 | | 15.16 |
| B | 7.65 | | 7.39 |
| C | 2.67 | | 2.21 |
| D | | 0.20 | |
| E | | 0.40 | |
| F | | 1.27 | |
| G | | 0.66 | |
| H | 10.51 | | 10.1 |
| J | | 0.63 | |
| K | | 45° | |
| L | | 5° | |
| M | | 0.25 | |
| N | | 0.76 | |

*Fig.13* ***FX489P 24-pin plastic Package***




**Note: All dimensions in mm.**

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 31.85 | 31.65 |
| B | 13.82 | 13.61 |
| C | 15.75 | 15.11 |
| D | 17.02 | 15.75 |
| E | 0.254 | TYPICAL |
| F | 7° | |
| G | 3.43 | 2.92 |
| H | 0.46 | |
| J | 2.54 | TYPICAL |
| K | 1.52 | |
| L | 3.91 | 3.71 |
| M | 0.75 | TYPICAL |

## Ordering Information

**FX489DW** **24-pin plastic S.O.I.C.**

**FX489P** **24-pin plastic DIL**

# CML Semiconductor Products

**APPLICATION INFORMATION**

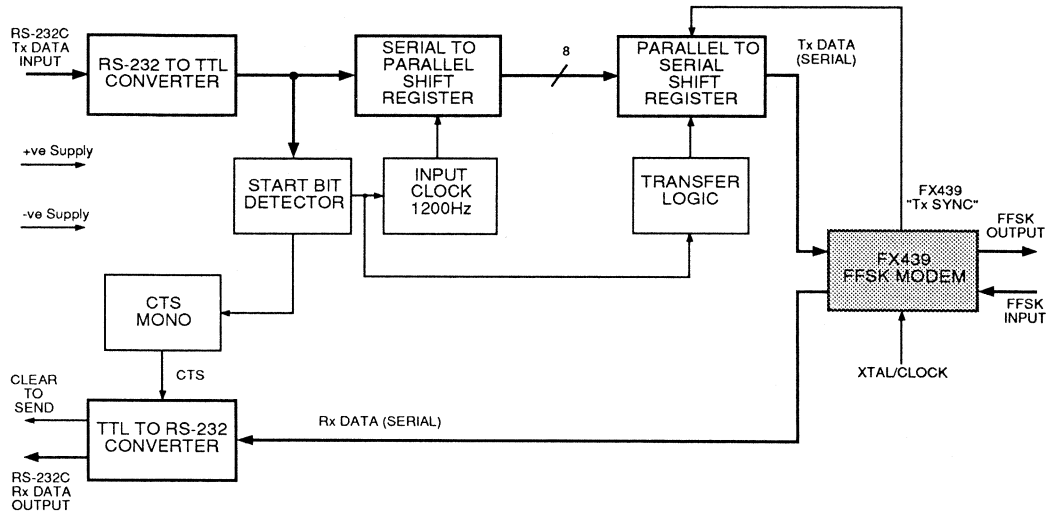
# RS-232C Modem Using the FX439

Publication AP/439 - 232/2 June 1989

## Features/Applications

- RS-232C Compatible
- Full-Duplex
- Single 5-Volt Supply
- Remote Telemetry Applications
- Low-Cost – Low-Power Applications
- Radio and Line Signalling
- Alarm Systems

*Fig.1 System Block Diagram*




## Introduction

This application note, used with a current FX439 Data Sheet, outlines the construction of a low-cost modem for the transmission of RS-232C data in the form of Fast Frequency Shift Keying [1] *(FFSK)*, between terminals by a radio or line medium using the FX439 FFSK Modem. The FX439 is a CMOS, FFSK Modem, operating at 1200 baud.

The transmitter and receiver work independently, allowing full-duplex operation. All synchronization (Tx and Rx) and baud rate signals are provided by the FX439, which uses a pin selected 1.008/4.032 MHz Xtal for high stability. The mark/space frequencies are 1200Hz and 1800Hz respectively, with all frequency transitions occurring at the zero crossing point.

This circuit accepts signals, converts them to TTL, then inputs them to the FX439, synchronized by the FX439 clock, for transmission.

The FX439 receives the FFSK, recovers the transmitted data (RS-232C format) which, once passed through a TTL to RS-232 level converter can be input to a data terminal.

This RS-232C format must be presented as follows:

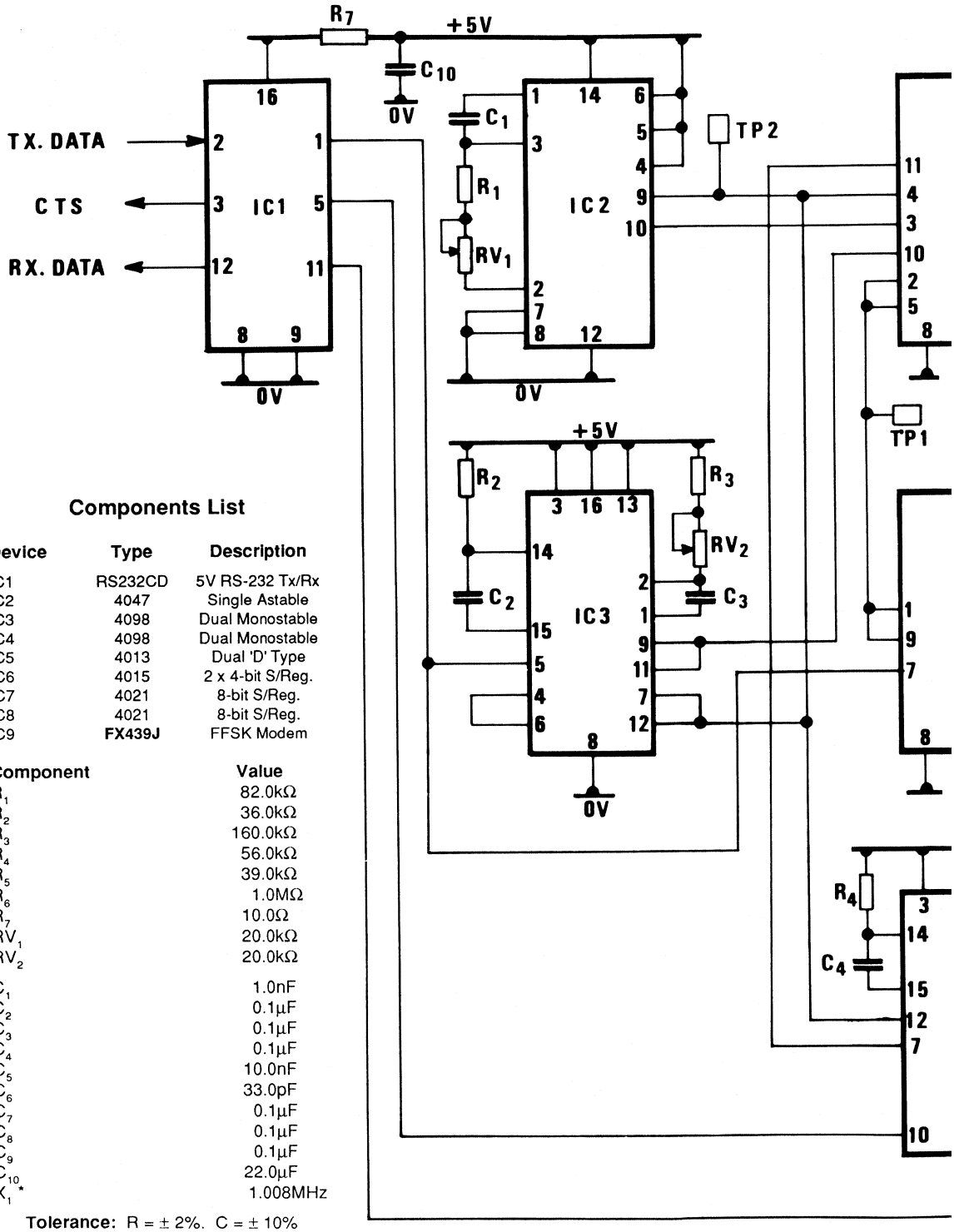
- **(i)** Baud rate - 1200.
- **(ii)** One start bit.
- **(iii)** Eight data bits.
- **(iv)** One stop bit.

– A total of 10 bits per word –

For full-duplex communications, the only RS-232C signals required are: Tx Data, Rx Data, Ground and Clear To Send. This circuit uses only a single 5-volt supply.

*[1] FFSK has proved to be a very rugged method of tone communications in respect of SINAD and Bit Error Rate performance and its use is now mandatory for the Band III radio networks.*

*Figure 2 System Circuit Diagram*

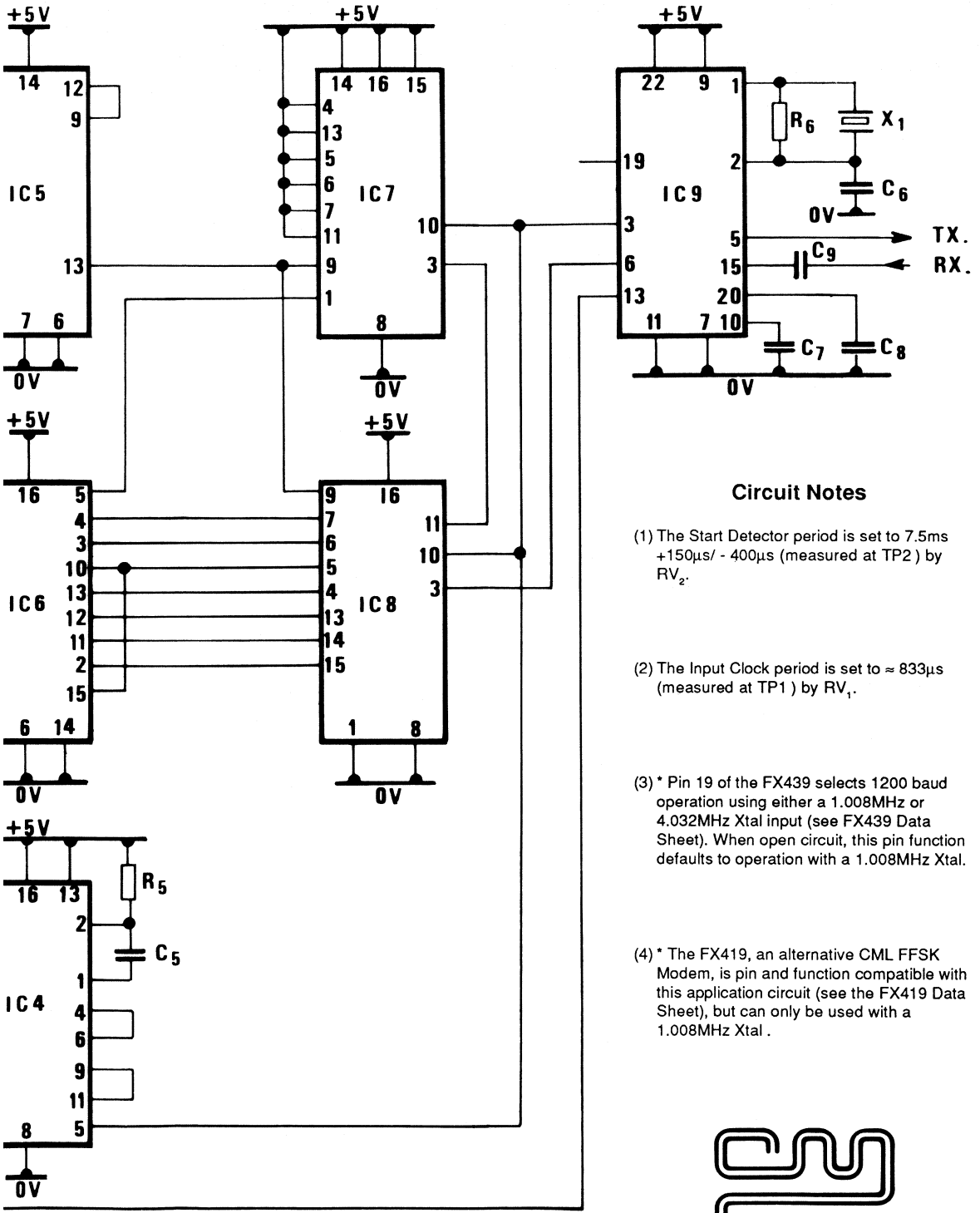



## Components List

| Device | Type | Description |
|---|---|---|
| IC1 | RS232CD | 5V RS-232 Tx/Rx |
| IC2 | 4047 | Single Astable |
| IC3 | 4098 | Dual Monostable |
| IC4 | 4098 | Dual Monostable |
| IC5 | 4013 | Dual 'D' Type |
| IC6 | 4015 | 2 x 4-bit S/Reg. |
| IC7 | 4021 | 8-bit S/Reg. |
| IC8 | 4021 | 8-bit S/Reg. |
| IC9 | **FX439J** | FFSK Modem |

| Component | Value |
|---|---|
| $R_1$ | 82.0kΩ |
| $R_2$ | 36.0kΩ |
| $R_3$ | 160.0kΩ |
| $R_4$ | 56.0kΩ |
| $R_5$ | 39.0kΩ |
| $R_6$ | 1.0MΩ |
| $R_7$ | 10.0Ω |
| $RV_1$ | 20.0kΩ |
| $RV_2$ | 20.0kΩ |
| $C_1$ | 1.0nF |
| $C_2$ | 0.1µF |
| $C_3$ | 0.1µF |
| $C_4$ | 0.1µF |
| $C_5$ | 10.0nF |
| $C_6$ | 33.0pF |
| $C_7$ | 0.1µF |
| $C_8$ | 0.1µF |
| $C_9$ | 0.1µF |
| $C_{10}$ | 22.0µF |
| $X_1$* | 1.008MHz |

**Tolerance:** R = ± 2%. C = ± 10%




## Circuit Notes

(1) The Start Detector period is set to 7.5ms +150µs/ - 400µs (measured at TP2 ) by $RV_2$.

(2) The Input Clock period is set to ≈ 833µs (measured at TP1 ) by $RV_1$.

(3) * Pin 19 of the FX439 selects 1200 baud operation using either a 1.008MHz or 4.032MHz Xtal input (see FX439 Data Sheet). When open circuit, this pin function defaults to operation with a 1.008MHz Xtal.

(4) * The FX419, an alternative CML FFSK Modem, is pin and function compatible with this application circuit (see the FX419 Data Sheet), but can only be used with a 1.008MHz Xtal .

## RS-232C Modem Circuit Diagram – *Figure 2*

**Transmit Data**

IC1, the RS-232 to TTL CMOS converter, supplies the input data at the correct level to the Input Shift Register (IC6) and the Start Bit Detector ($^1/_2$ IC3).
Detection of the negative going edge of the Start Bit (as shown in Figure 3) enables the 1200Hz oscillator (IC2 and $^1/_2$ IC5) for a period of 9 positive clock edges, clocking the eight bits of input data (or seven bits + parity) into the Serial to Parallel Shift Register (IC6). On completion of the input loading, after the 9 clock edges, the eight bits are transferred to the Parallel to Serial Shift Registers (IC7 & IC8) whilst the FX439 Tx Sync Output (FX439 clock) is low.
*– This (Serial/Parallel – Parallel/Serial) operation is carried out to allow for variations between the data input timing and the FX439 clock –*
The data, back in its serial format, is then clocked out of the shift registers starting on the next positive edge of the FX439 TX Sync O/P, to be transmitted by the FX439 (IC9) as 1200 baud (1200Hz/1800Hz) FFSK . The Start Bit (IC8 pin 1) and Stop Bit (IC7 pin 15) are 'hard wired' in the Parallel to Serial registers, giving the correct final RS-232C format.

Whilst the data is being clocked out of IC7 & IC8, more data can be clocked into IC6 – and the cycle restarts. To allow for phase variaton between the RS-232 1200Hz clock and the FX439 clock, the Clear To Send (CTS) line is held low, disabling further transmission for a period equal to one clock cycle (≈ 833µs) from the end of the Stop Bit.

**Receive Data**

The FX439 receiver (IC9) recovers the FFSK data. This data is in the correct format and only requires to be level converted back to RS-232C using IC1.

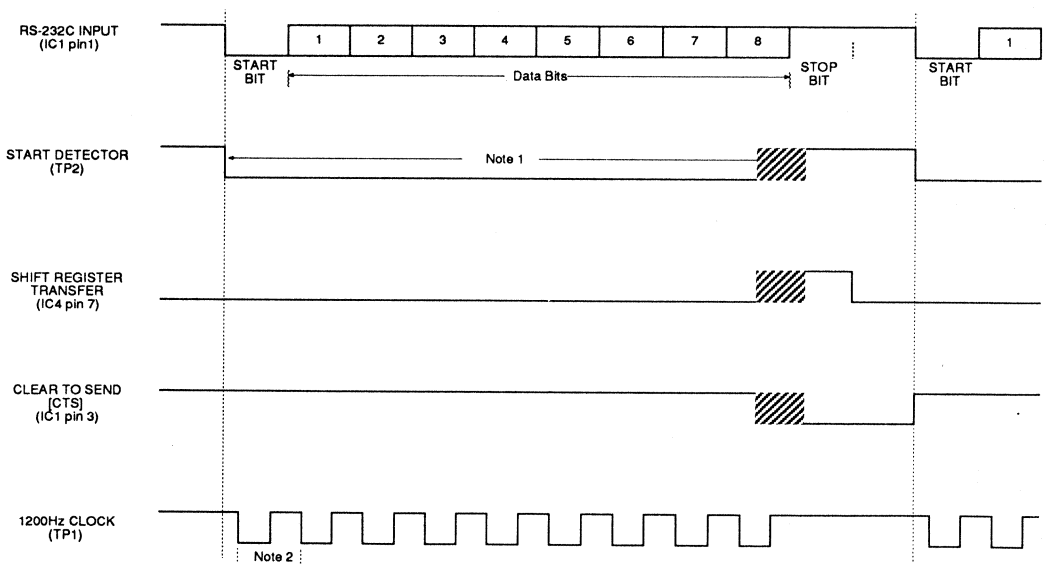
**Data Terminal RS-232C Communications Program**

Software controlling communication has two requirements:
i) To enable the FX439 to sync properly, 16-bits of data should be transmitted as a pre-amble (ideally bit reversals) before the true data is transmitted.
ii) The program must monitor the Clear to Send (CTS) line and transmit only when this line is active (high).

**Power Requirements**

This RS-232C Modem operates on a single 5v, 40mA supply.

*Fig.3 Transmit System Timing Diagram*




**Notes**
(1) The detector period is set by $RV_2$, (7.5ms +0.15ms/ -0.4ms).
(2) ≈ 833µs clock period set by $RV_1$.
(3) For output timing refer to the current FX439 Data Sheet.

# Integrated Circuits Data Book

Section 9

# Voice Security/ Voice Coding

# CML Semiconductor Products

PRODUCT INFORMATION

# FX214 FX224 FX234

## VSB* Audio Scrambler

Publication D/214/2 November 1987
Provisional Issue

### Features/Applications

- *Variable Split-Band Frequency Inversion Voice Scrambler
- 32 Programmable Split Frequencies
- CTCSS HP Filter
- High Recovered Audio Quality
- Low-Power 5 Volt CMOS
- Half-Duplex Switching
- Powersave Facility
- Mobile or Cellular Radio Applications
- Fixed or Rolling Code Applications
- Serial/Parallel Load Options: FX214 (Serial), FX224 (Parallel), FX234 (Serial and Parallel)
- DIL and SMD Package Options

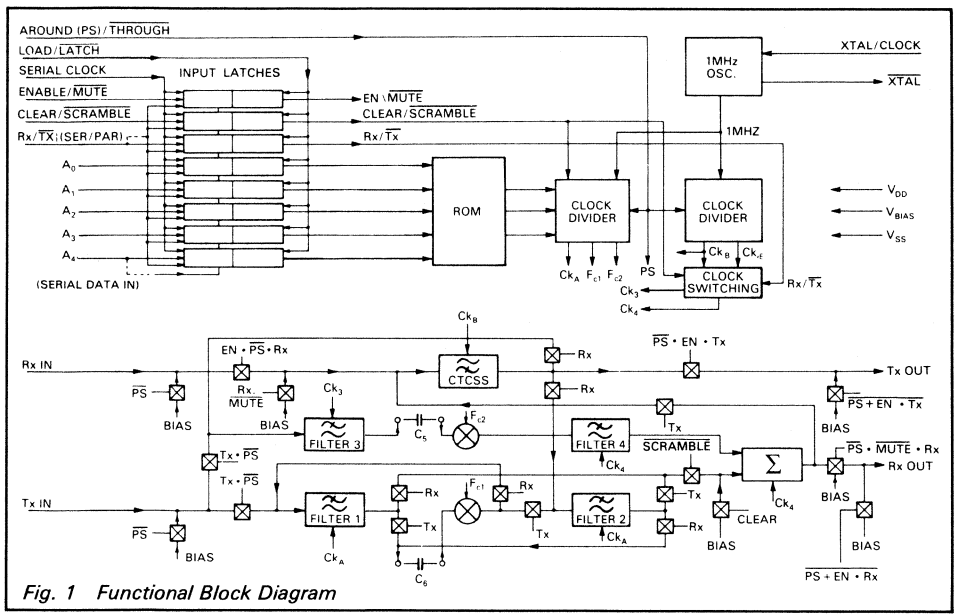



*Fig. 1 Functional Block Diagram*

FX214
FX224
FX234

### Brief Description

The FX214, 224 and 234 are a family of Low-Power CMOS LSI devices designed as Variable Split-Band (VSB) Voice Scramblers.

The device uses separate Rx and Tx paths which are switched for Half-Duplex operation. To prevent interference from sub-audio products, an on-chip Continuous Tone Controlled Squelch System (CTCSS) Highpass Filter is automatically switched to the input in Rx, and to the output in Tx.

Scrambling is achieved by splitting the input voice frequencies into upper and lower frequency bands using switched capacitor filters, modulating each band with selected carrier frequencies to 'frequency invert' the bands, then summing the output.
A total of 32 different split-point and carrier frequency combinations are externally programmable using a 5-bit code, this code can be either fixed or varying (Rolling), for greater security.

'Sync/Speech Mute', 'Powersave', 'Clear' and 'Audio Bypass' facilities are controlled via external commands.

Timing and filter clocks are derived internally from an on-chip 1MHz oscillator requiring only an external 1MHz Xtal or clock pulse input.

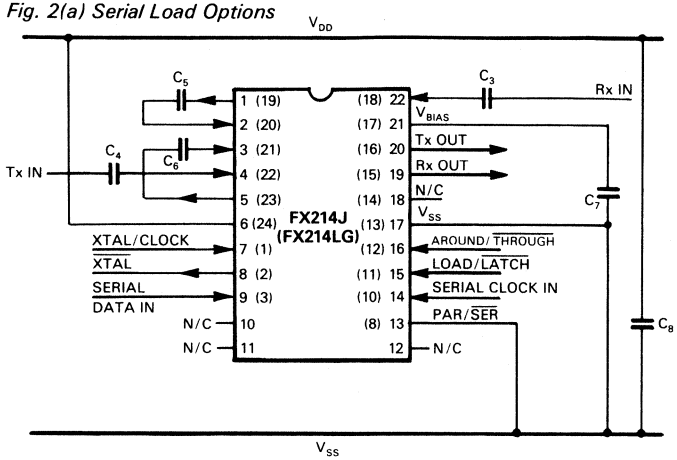
This device demonstrates high baseband and carrier frequency rejection with good 'recovered audio' quality. Serial or Parallel command loading functions are available in both DIL and SMD packages with a 'Dual' load device in a 28-lead plastic leaded chip carrier.

| Pin Number | | | | | Function |
|---|---|---|---|---|---|
| FX 214J | FX 214LG | FX 224J | FX 224LG | FX 234LH | |
| 7 | 1 | 1 | 1 | 1 | **Xtal/Clock:** Input to the clock oscillator inverter. A 1MHz Xtal input or externally derived 1MHz clock is injected here. *See Figure 2.* |
| 8 | 2 | 2 | 2 | 2 | **$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter. |
| 9 | 3 | | | 3 | **Serial Data Input:** This pin is used, on devices wired in the serial loading mode, to input an 8-bit word representing the digital control functions. This word is loaded using the serial data clock and is input in the following sequence:– ENABLE; CLEAR; Rx/$\overline{\text{Tx}}$; $A_0$; $A_1$; $A_2$; $A_3$; $A_4$, with the Load/$\overline{\text{Latch}}$ being operated on completion. *See Timing Diagram Figure 7.* |
| | | 3 | 3 | 4 | $A_4$ |
| | | 4 | 4 | 5 | $A_3$ |
| | | 5 | 5 | 6 | $A_2$ |
| | | 6 | 6 | 7 | $A_1$ |
| | | 7 | 7 | 8 | $A_0$ |
| | | | | | **Programming Inputs:** In parallel mode, these are the 5 digital inputs whose code defines the split point frequency and the High and Low band carrier frequencies. Each of the 5 input pins have a 1MΩ internal pullup resistor. Table 2 contains programming information. |
| | | 8 | 8 | 9 | **Rx/$\overline{\text{Tx}}$:** This digital input selects the Receive or Transmit paths and configures Upperband and Lowerband filter bandwidths whilst setting the CTCSS High Pass Filter position in the signal path. *See Table 1 and Figures 5 and 6.* 1MΩ internal pullup resistor (Rx). |
| 13 | 8 | | | 10 | **Parallel/$\overline{\text{Serial}}$:** This pin defines the loading mode of the digital function inputs. In the FX224J and FX224LG parallel load devices this pin has no external connections. For FX214J and FX214LG serial load devices this pin must be externally connected to $V_{SS}$. For the FX234LH, the dual loading device, this pin must be externally connected to $V_{SS}$ for the serial mode. This pin, on all devices has a 1MΩ internal pullup resistor (Parallel). *See Figure 2(a), (b), (c).* |
| | | 9 | 9 | 11 | **Clear/$\overline{\text{Scramble}}$:** This digital input puts the device into 'Clear' or 'Frequency Inversion' mode by controlling the application of carrier frequency to the Upper and Lower band Balanced Modulators. In 'Scramble' the Balanced Modulator carrier frequency values are selected by the split point address $A_0$–$A_4$ (Table 2). In 'Clear' carriers are turned off and the Balanced Modulators are bypassed internally, the Lower band signal is not added to to the output signal. 1MΩ internal pullup resistor (Clear). |
| | | 10 | 10 | 12 | **Enable/$\overline{\text{Mute}}$:** This digital function is used to disable Receive or Transmit signal paths for rolling code synchronization whilst maintaining bias conditions. To allow synchronizing information to be transmitted, or receiver audio output to be removed during sync periods, a logic '1' will enable, a logic '0' will disable the selected (Rx/$\overline{\text{Tx}}$) audio path. *See Table 1.* 1MΩ internal pullup resistor (Enable). |
| 14 | 10 | | | 13 | **Serial Clock Input:** This is the externally applied data clock frequency used to shift input data along on devices wired in the Serial loading mode. One full data clock cycle is required to shift one data bit completely into the register. *See Timing Diagram Figure 7.* This pin has a 1MΩ internal pullup resistor. |
| 15 | 11 | 11 | 11 | 14 | **Load/$\overline{\text{Latch}}$:** This pin controls the loading of the 8 digital function inputs; ENABLE; CLEAR; Rx/$\overline{\text{Tx}}$; $A_0$–$A_4$ into the internal register. When this pin is at logic '1' all 8 inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel mode Load/$\overline{\text{Latch}}$ must be kept at logic '0' whilst a new function is loaded, then Load/$\overline{\text{Latch}}$ strobed 0-1-0 to latch the inputs in. For serial loading the serial data should be loaded with Load/$\overline{\text{Latch}}$ at logic '0' and then Load/$\overline{\text{Latch}}$ strobed 0-1-0 on completion of data loading. 1MΩ internal pullup resistor (Load). *See Figure 7.* NOTE: Serial and/or parallel loading functions are dependant upon device type *(see pages 9 and 10).* |
| 16 | 12 | 12 | 12 | 15 | **Around (Powersave)/$\overline{\text{Through}}$:** This digital input is used, when at logic '1' to put the device into the Powersave condition where all parts of the device except the 1MHz oscillator circuits are shut down, and signal input and output lines made open circuit, free of all bias. This allows signal paths to be routed externally around the device, whilst reducing current consumption. A logic '0' at this input enables the device to work normally as shown in Table 1. 1MΩ internal pullup resistor (Around). |

| Pin Number | | | | | Function |
|---|---|---|---|---|---|
| FX 214J | FX 214LG | FX 224J | FX 224LG | FX 234LH | |
| 17 | 13 | 13 | 13 | 16 | $V_{SS}$: Negative Supply (GND). |
| 18 | 14 | 14 | 14 | 17 | **Internal Connection:** This pin is internally connected, leave open circuit. |
| 19 | 15 | 15 | 15 | 18 | **Rx Output:** This is the processed received audio signal output. This pin is held at a D.C. 'bias' voltage for all functions except Powersave. This buffered output is driven by the Summer circuit in the Rx mode. Signal paths and bias levels are detailed in Table 1 and Figure 6. |
| 20 | 16 | 16 | 16 | 19 | **Tx Output:** This is the processed audio output for the transmission channel. This pin is held at a D.C. 'bias' for all functions except Powersave. This summed and buffered signal is passed through the CTCSS High Pass Filter to the output pin in the Tx mode. Signal paths and bias levels are detailed in Table 1 and Figure 5. |
| 21 | 17 | 17 | 17 | 20 | $V_{BIAS}$: Normally at $V_{DD}/2$ this pin requires an external decoupling capacitor $C_7$, to $V_{SS}$. |
| 22 | 18 | 18 | 18 | 21 | **Rx Input:** This is the analogue received audio signal input. This pin is held at a D.C. 'bias' voltage by a 300kΩ on-chip bias resistor which is selected for all functions except Powersave, and therefore requires to be connected to external circuitry by a capacitor, $C_3$. *See Figure 2.* This input is routed through the CTCSS High Pass Filter in Rx mode to remove sub audio frequencies from the voice band. Signal paths and bias levels are detailed in Table 1 and Figure 6. |
| 1 | 19 | 19 | 19 | 22 | **Highband Filter Output:** The output of the Input Filter of the Upperband arm. The Rx/$\overline{Tx}$ function sets the lowpass filter at 3400Hz or 2700Hz respectively. This output must be connected to the Highband Balanced Modulator input via capacitor $C_5$. *See Figure 2.* |
| 2 | 20 | 20 | 20 | 24 | **Highband Balanced Modulator Input:** The input to the Balanced Modulator of the Upperband arm. This input must be connected to the Highband Filter Output via capacitor $C_5$. |
| 3 | 21 | 21 | 21 | 25 | **Lowband Balanced Modulator Input:** The input to the Balanced Modulator of the Lowerband arm. This input must be connected to the Lowband Filter Output with capacitor $C_6$. *See Figure 2.* |
| 4 | 22 | 22 | 22 | 26 | **Tx Input:** This is the analogue 'Clear' audio input for the VSB scrambler. This pin is held at a D.C. 'bias' voltage by a 300kΩ on-chip bias resistor which is selected for all functions except Powersave, and therefore requires to be connected to external circuitry by a capacitor, $C_4$. *See Figure 2.* This input, in the Tx mode, is connected to Upper and Lowerband input filters, signal paths and bias levels are detailed in Table 1 and Figure 5. |
| 5 | 23 | 23 | 23 | 27 | **Lowband Filter Output:** The output of the Input Filter of the Lowerband arm, the Rx/$\overline{Tx}$ function determines which filter is used (Filter 1 or 2). *See Figures 5 and 6.* This output must be connected to the Lowband Balanced Modulator Input via capacitor $C_6$. *See Figure 2.* |
| 6 | 24 | 24 | 24 | 28 | $V_{DD}$: A single +5V supply is required. |
| 10, 11, 12 | 4, 5, 6, 7, 9 | | | 23 | **Not Connected** |

## Component Connections

*Fig. 2(a) Serial Load Options*

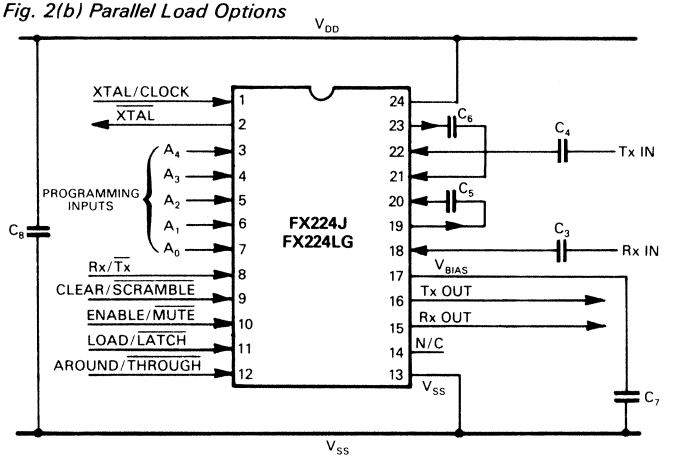


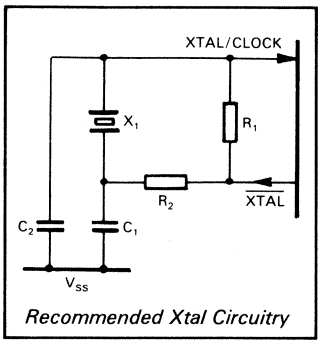

Not Connected

| | |
|---|---|
| FX214J | 10, 11, 12, 18* |
| FX214LG | 4, 5, 6, 7, 9, 14* |
| FX224J | 14* |
| FX224LG | 14* |
| FX234LH | 17*, 23 |

*Internally connected, do not connect to.

*Fig. 2(b) Parallel Load Options*

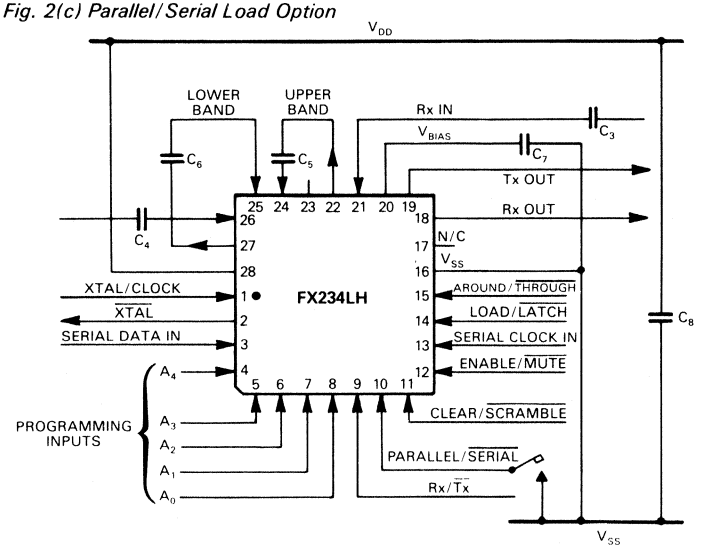



*Recommended Xtal Circuitry*

Xtal circuitry shown is in accordance with CML Application Note D/XT/1 April '86.

*Fig. 2(c) Parallel/Serial Load Option*




| Component References | |
|---|---|
| **Component** | **Unit Value** |
| $R_1$ | 1M |
| $R_2$ | Selectable |
| $C_1$ | 33p |
| $C_2$ | 68p |
| $C_3$ | 15n |
| $C_4$ | 15n |
| $C_5$ | 1.0µ |
| $C_6$ | 1.0µ |
| $C_7$ | 1.0µ |
| $C_8$ | 1.0µ |
| $X_1$ | 1MHz |

**Tolerance** Resistors ± 10%
Capacitors ± 20%

$C_5$ and $C_6$ are coupling capacitors between filter outputs and balanced modulator inputs.

*Fig. 2 External Component Connections*

## Application Information

This device can be used in 'Scramble' (frequency inversion) or 'Clear' speech modes. The inversion frequencies, when selected are controlled by the ROM address code (table 2). Keeping the code in one state (fixed) is the simplest form of operation. A more secure method is to continually change the ROM address code (rolling code) therefore changing split-point and carrier frequencies. This method requires some external form of code change generation with synchronization between transmit and receive stations. Many variations of code sequence are possible.

The recommended external component connections are shown in figure 2. In the Scramble mode, Split-point and Low and High band carrier frequencies ($F_c1$, $F_c2$) are selected and set in accordance with the ROM address code present at the inputs $A_0$ to $A_4$, *See Table 2.*

During the Clear speech function both Lower and Upperband filter arms are selected (figures 5 or 6), the carrier frequencies are turned off and the balanced modulators are bypassed internally. The Low band audio is removed from the output signal prior to summation.

**Enable/$\overline{\text{Mute}}$**

To enable code synchronization to be transmitted the speech output can be interrupted with the Enable/$\overline{\text{Mute}}$ function. A logic '0' will isolate the whole device whilst leaving the audio input and output pins at bias level. *See Table 1.*

**Powersave**

When the Around/$\overline{\text{Through}}$ function is at a logic '1' the device is in the powersave condition. Audio signals may be hardwired around the device normally as the input and output pins are open circuit. *See Table 1.*

| Effect of Chosen Function on Inputs and Outputs | | CHOSEN FUNCTION | | | |
|---|---|---|---|---|---|
| | | **Rx = '1'** | **$\overline{\text{Tx}}$ = '0'** | **$\overline{\text{Mute}}$ = '0'** | **Around** (Powersave) = '1' |
| **Rx Input** | Path | Enabled | Disconnect | Disconnect | High Impedance |
| | Level | Bias | Bias | Bias | |
| **Rx Output** | Path | Enabled | Disconnected | Disconnect | High Impedance |
| | Level | Bias | Bias | Bias | |
| **Tx Input** | Path | Disconnected | Enabled | Enabled | High Impedance |
| | Level | Bias | Bias | Bias | |
| **Tx Output** | Path | Disconnected | Enabled | Disconnected | High Impedance |
| | Level | Bias | Bias | Bias | |

*Table 1 Functions Influencing Signal Paths*

| ROM Address $A_4$–$A_0$ | Split Point Hz | Low Band Carrier, Hz $f_{c1}$ | High Band Carrier, Hz $f_{c2}$ |
|---|---|---|---|
| 0 0 0 0 0 | 2800 | 3105 | 6172 |
| 0 0 0 0 1 | 2625 | 2923 | 6024 |
| 0 0 0 1 0 | 2470 | 2777 | 5813 |
| 0 0 0 1 1 | 2333 | 2631 | 5681 |
| 0 0 1 0 0 | 2210 | 2512 | 5555 |
| 0 0 1 0 1 | 2100 | 2403 | 5494 |
| 0 0 1 1 0 | 2000 | 2304 | 5376 |
| 0 0 1 1 1 | 1909 | 2212 | 5263 |
| 0 1 0 0 0 | 1826 | 2127 | 5208 |
| 0 1 0 0 1 | 1750 | 2049 | 5102 |
| 0 1 0 1 0 | 1680 | 1984 | 5050 |
| 0 1 0 1 1 | 1555 | 1858 | 4950 |
| 0 1 1 0 0 | 1448 | 1748 | 4807 |
| 0 1 1 0 1 | 1354 | 1655 | 4716 |
| 0 1 1 1 0 | 1272 | 1572 | 4629 |
| 0 1 1 1 1 | 1200 | 1501 | 4587 |

| ROM Address $A_4$–$A_0$ | Split Point Hz | Low Band Carrier, Hz $f_{c1}$ | High Band Carrier, Hz $f_{c2}$ |
|---|---|---|---|
| 1 0 0 0 0 | 1135 | 1436 | 4504 |
| 1 0 0 0 1 | 1050 | 1351 | 4424 |
| 1 0 0 1 0 | 976 | 1278 | 4347 |
| 1 0 0 1 1 | 913 | 1213 | 4310 |
| 1 0 1 0 0 | 857 | 1157 | 4273 |
| 1 0 1 0 1 | 792 | 1094 | 4166 |
| 1 0 1 1 0 | 736 | 1037 | 4132 |
| 1 0 1 1 1 | 688 | 988 | 4065 |
| 1 1 0 0 0 | 636 | 936 | 4032 |
| 1 1 0 0 1 | 591 | 891 | 3968 |
| 1 1 0 1 0 | 552 | 853 | 3937 |
| 1 1 0 1 1 | 512 | 813 | 3906 |
| 1 1 1 0 0 | 471 | 772 | 3846 |
| 1 1 1 0 1 | 428 | 728 | 3816 |
| 1 1 1 1 0 | 388 | 688 | 3787 |
| 1 1 1 1 1 | 350 | 650 | 3731 |

*Table 2 ROM Address Programming Table*

## Application Information

For the following descriptions the term 'FX214' can be taken to mean FX214, FX224 and FX234.

### Audio Quality

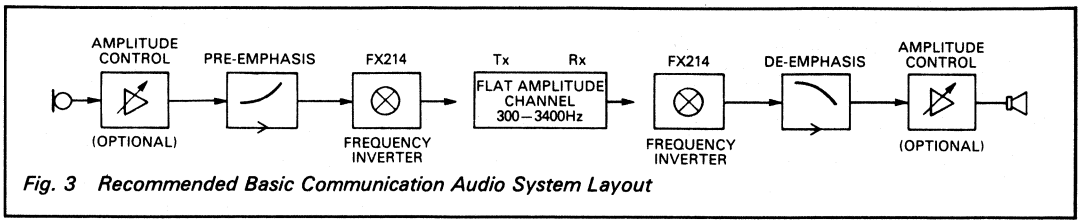



*Fig. 3 Recommended Basic Communication Audio System Layout*

Figure 3 shows the recommended basic audio system layout using added pre- and de-emphasis circuitry to maintain good recovered speech quality. In the Transmit mode *Do Not* pre-emphasise the audio output of the FX214. In the Receive mode de-emphasis should be used after the FX214.

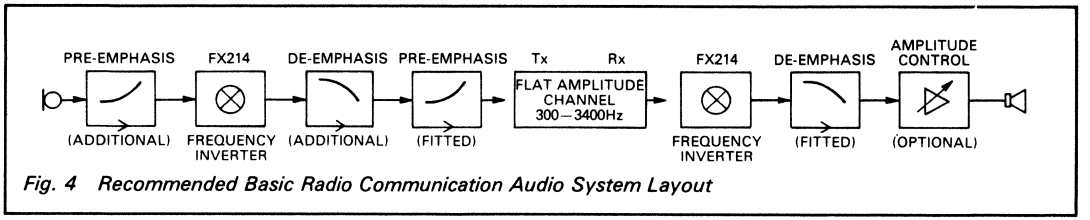



*Fig. 4 Recommended Basic Radio Communication Audio System Layout*

Figure 4 shows the recommended basic audio system layout if it is necessary to install the FX214 within a radio having pre- and de-emphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

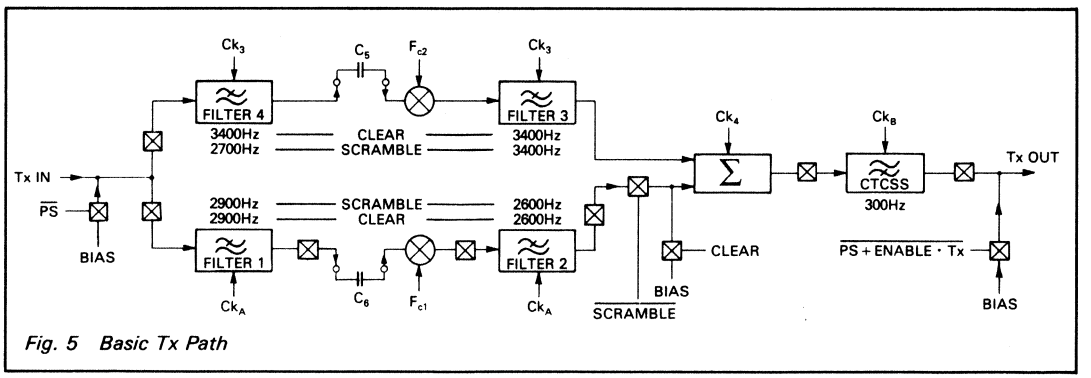



*Fig. 5 Basic Tx Path*

During the Transmit function the Low Pass and CTCSS filters are configured automatically as shown in Figure 5, with cut-off frequencies (-3dB) indicated.

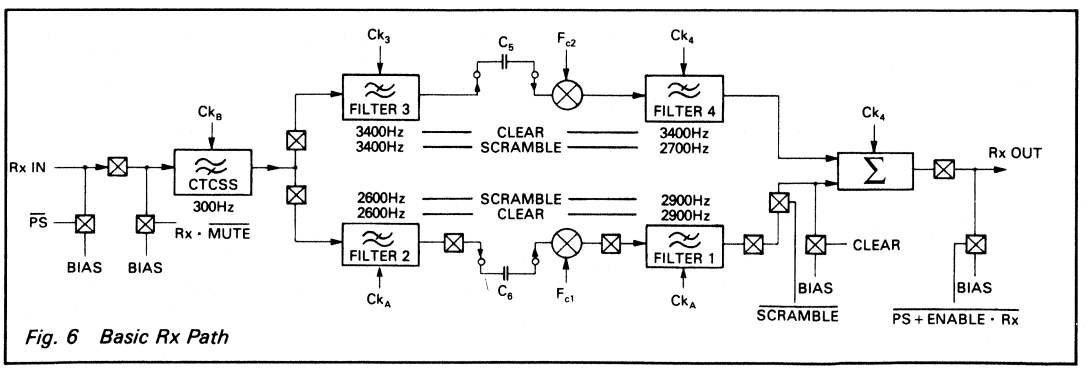



*Fig. 6 Basic Rx Path*

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

# Electrical Specifications

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | ± 30mA |
| (other pins) | | ± 20mA |
| Total device dissipation @ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | FX214J/224J | −30°C to +85°C (Ceramic) |
| | FX214LG/224LG/234LH | −30°C to +70°C (Plastic) |
| Storage temperature range: | FX214J/224J | −55°C to +125°C (Ceramic) |
| | FX214LG/224LG/234LH | −40°C to +85°C (Plastic) |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5.0V, $T_{amb}$ = 25°C, $F_{clk}$ = 1.0MHz, Audio Level Ref: 0dB = 775mVrms.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply voltage | | 4.5 | 5 | 5.5 | V |
| Supply current (Enabled) | | — | 8 | — | mA |
| Supply current (Powersave) | | — | 1.2 | — | mA |
| **Analogue Input Impedances** | | | | | |
| Tx/Rx Input (Enabled) | | — | 100 | — | kΩ |
| Tx/Rx Input (Powersave) | | 1 | — | — | MΩ |
| Balanced Modulator | | — | 40 | — | kΩ |
| **Analogue Output Impedances** | | | | | |
| Rx Output (Tx Mode) | | — | 100 | — | kΩ |
| Rx Output (Rx Mode) | | — | — | 2 | kΩ |
| Rx Output (Powersave) | | 1 | — | — | MΩ |
| Tx Output (Tx Mode) | | — | — | 2 | kΩ |
| Tx Output (Rx Mode) | | — | 100 | — | kΩ |
| Tx Output (Powersave) | | 1 | — | — | MΩ |
| Input LPF | | — | — | 1 | kΩ |
| **Digital Values** | | | | | |
| Digital Input Impedance | | 100 | — | — | kΩ |
| **Dynamic Values** | | | | | |
| Input Logic '1' | | 3.5 | — | — | V |
| Input Logic '0' | | — | — | 1.5 | V |
| Xtal/Clock Frequency | | — | 1 | — | MHz |
| Analogue Input Level | | −18 | — | +6 | dB |
| Carrier Breakthrough | 1 | — | −55 | — | dB |
| Baseband Breakthrough | 1, 2 or 3 | — | −33 | — | dB |
| Filter Clock Breakthrough | 1, 2 or 3 | — | −50 | — | dB |
| Output Noise | 1, 4 | — | −45 | — | dB |
| **Passband Characteristics** | | | | | |
| **Clear Mode** | 7 | | | | |
| Passband Gain | | — | 0 | — | dB |
| Output Lower 3dB Point (Rx or Tx) | | — | 300 | — | Hz |
| Output Upper 3dB Point (Rx or Tx) | | — | 3400 | — | Hz |
| **Scramble-Descramble** | 5 | | | | |
| Received Signal Passband Gain | 6 | — | 0 | — | dB |
| Received Signal Lower 3dB Point | | — | 400 | — | Hz |
| Received Signal Upper 3dB Point | | — | 2700 | — | Hz |
| Transmitted Signal Lower 3dB Point | | — | 300 | — | Hz |
| Transmitted Signal Upper 3dB Point | | — | 3400 | — | Hz |
| **CTCSS (Highpass Filter)** | | | | | |
| −3dB Point | | — | 300 | — | Hz |
| Passband Gain | | — | 0 | — | dB |
| Stopband Attenuation at f>250 Hz | | — | 40 | — | dB |

## Electrical Specifications...

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Timing** *(Figure 7)* | | | | | |
| Serial Mode Enable Set Up ($t_{SMS}$) | | 250 | — | — | ns |
| Serial Clock 'High' Pulse Width ($t_{PWH}$) | | 250 | — | — | ns |
| Serial Clock 'Low' Pulse Width ($t_{PWL}$) | | 250 | — | — | ns |
| Data Set Up Time ($t_{DS}$) | | 150 | — | — | ns |
| Data Hold Time ($t_{DHS}$) | | 50 | — | — | ns |
| Load/$\overline{\text{Latch}}$ Set Up Time ($t_{LL}$) | | 250 | — | — | ns |
| Load/$\overline{\text{Latch}}$ Pulse Width ($t_{LLW}$) | | 150 | — | — | ns |
| Data Set Up Time ($t_{DSP}$) | | 150 | — | — | ns |
| Data Hold Time ($t_{DHP}$) | | 20 | — | — | ns |

**Notes:**
1. *Measured at the output of a single device.*
2. *Tx Mode.*
3. *Rx Mode.*
4. *With input A.C. short-circuited to $V_{SS}$.*
5. *Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400Hz and measured relative to the input signal at the transmitting device.*
6. *Excluding split point ± 150Hz.*
7. *Measured at the Rx or Tx output pin of a single device.*

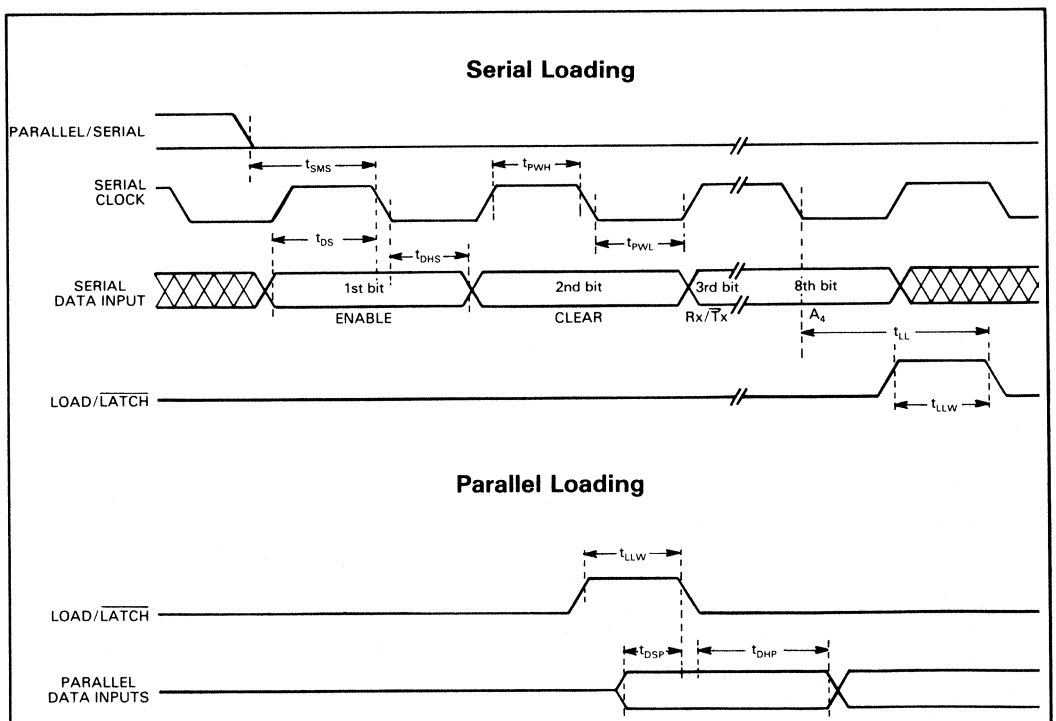



*Fig. 7 Loading Timing Diagram*

## Package Outlines

The FX214J cerdip package is shown in *Figure 8* and the FX224J cerdip package in *Figure 9.* The FX214LG and the FX224LG packages are shown in *Figure 10.* The FX234LH version is shown in *Figure 11.*

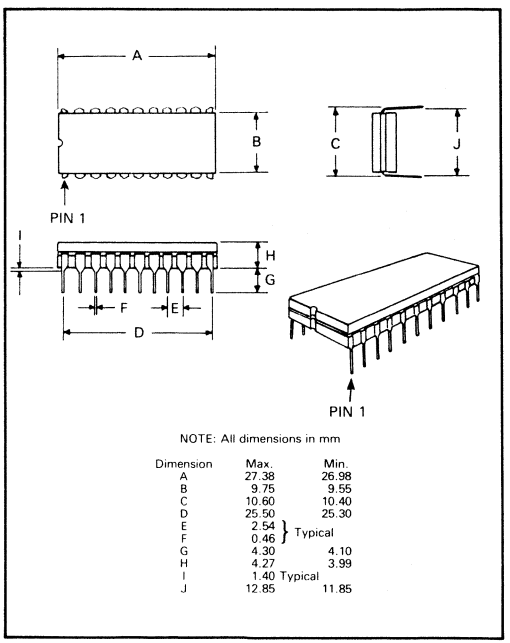
Both 'LG' and 'LH' packages are supplied in conductive trays for handling convenience.

To allow complete identification, the 'LG' and 'LH' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4 for the LG package, between pins 4 and 5 for the LH package.
Pins number anti-clockwise when viewed from the top (indent side).

## Handling Precautions

The FX214, FX224 and FX234 are CMOS LSI circuits which include input protection. However, precautions should be taken to prevent static discharges which may cause damage.

*Fig. 8* **FX214J** *22-pin DIL Package*

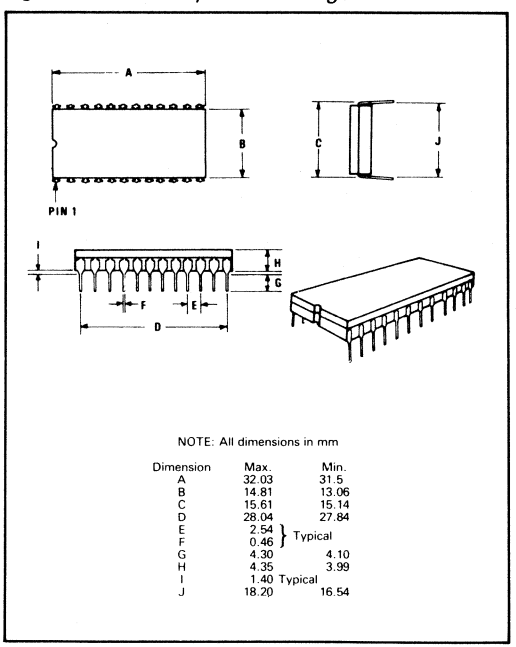



NOTE: All dimensions in mm

| Dimension | Max. | Min. |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 } Typical | |
| F | 0.46 } Typical | |
| G | 4.30 | 4.10 |
| H | 4.27 | 3.99 |
| I | 1.40 Typical | |
| J | 12.85 | 11.85 |

**Serial Load Option**

*Fig. 9* **FX224J** *24-pin DIL Package*



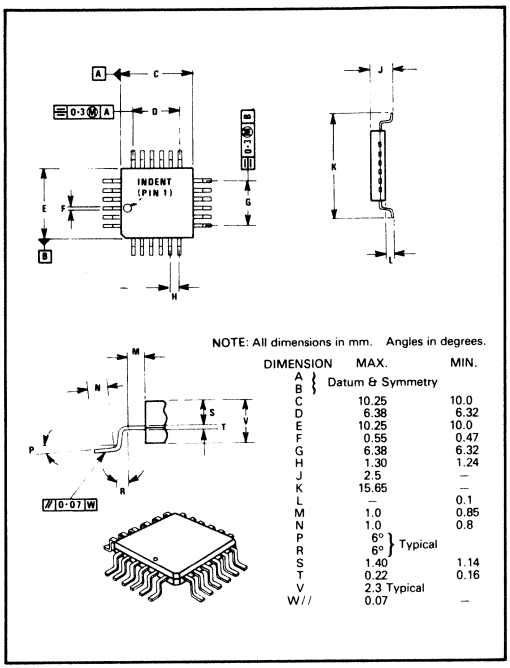

NOTE: All dimensions in mm

| Dimension | Max. | Min. |
|---|---|---|
| A | 32.03 | 31.5 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 } Typical | |
| F | 0.46 } Typical | |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 Typical | |
| J | 18.20 | 16.54 |

**Parallel Load Option**

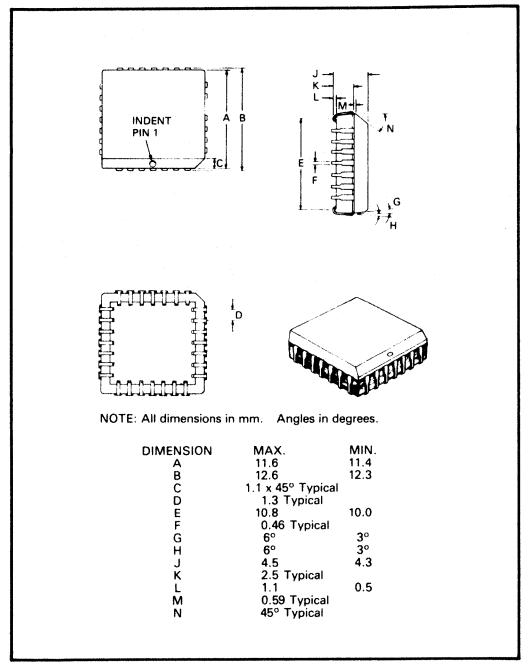
## Package Outlines...

*Fig. 10* **FX214LG and FX224LG** *24-pin Package*




**Serial or Parallel Load Option**

*Fig. 11* **FX234LH** *28-lead Package*




**Serial and Parallel Load Option**

## Ordering Information

| | | |
|---|---|---|
| **FX214J** | **22-pin cerdip DIL** | **Serial Load Only** |
| **FX224J** | **24-pin cerdip DIL** | **Parallel Load Only** |
| **FX214LG** | **24-pin quad plastic encapsulated bent and cropped** | **Serial Load Only (FX214LG)** |
| **FX224LG** | | **Parallel Load Only (FX224LG)** |
| **FX234LH** | **28-lead plastic leaded chip carrier** | **Serial and Parallel Load** |

# CML Semiconductor Products

APPLICATION INFORMATION

# Rolling Code Scrambling Using the FX224 VSB* Audio Scrambler

Publication AP/224 - Sc/1 April 1989

## Features/Applications

- * Variable Split-Band
- High Quality Received Audio
- 6 Code "Hop Rates"
- 32 Different Split-Point/Carrier (Code) Combinations
- Half-Duplex System
- Pseudo-Random Codes

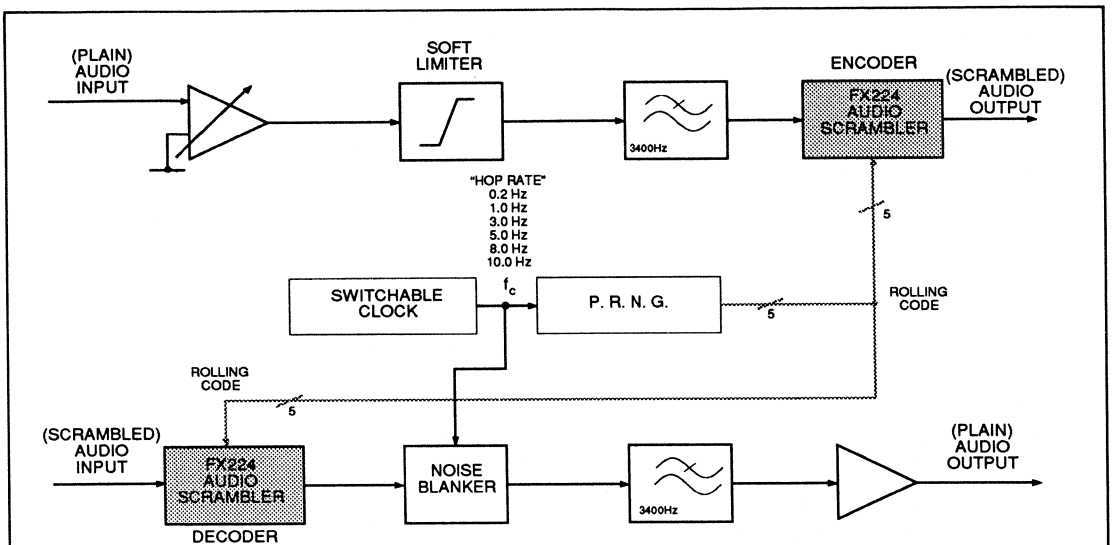



*Fig.1 System Block Diagram*

## Introduction

The principle application of the FX224 *Variable Split-Band Audio Scrambler is that of a frequency domain speech-band inverter.

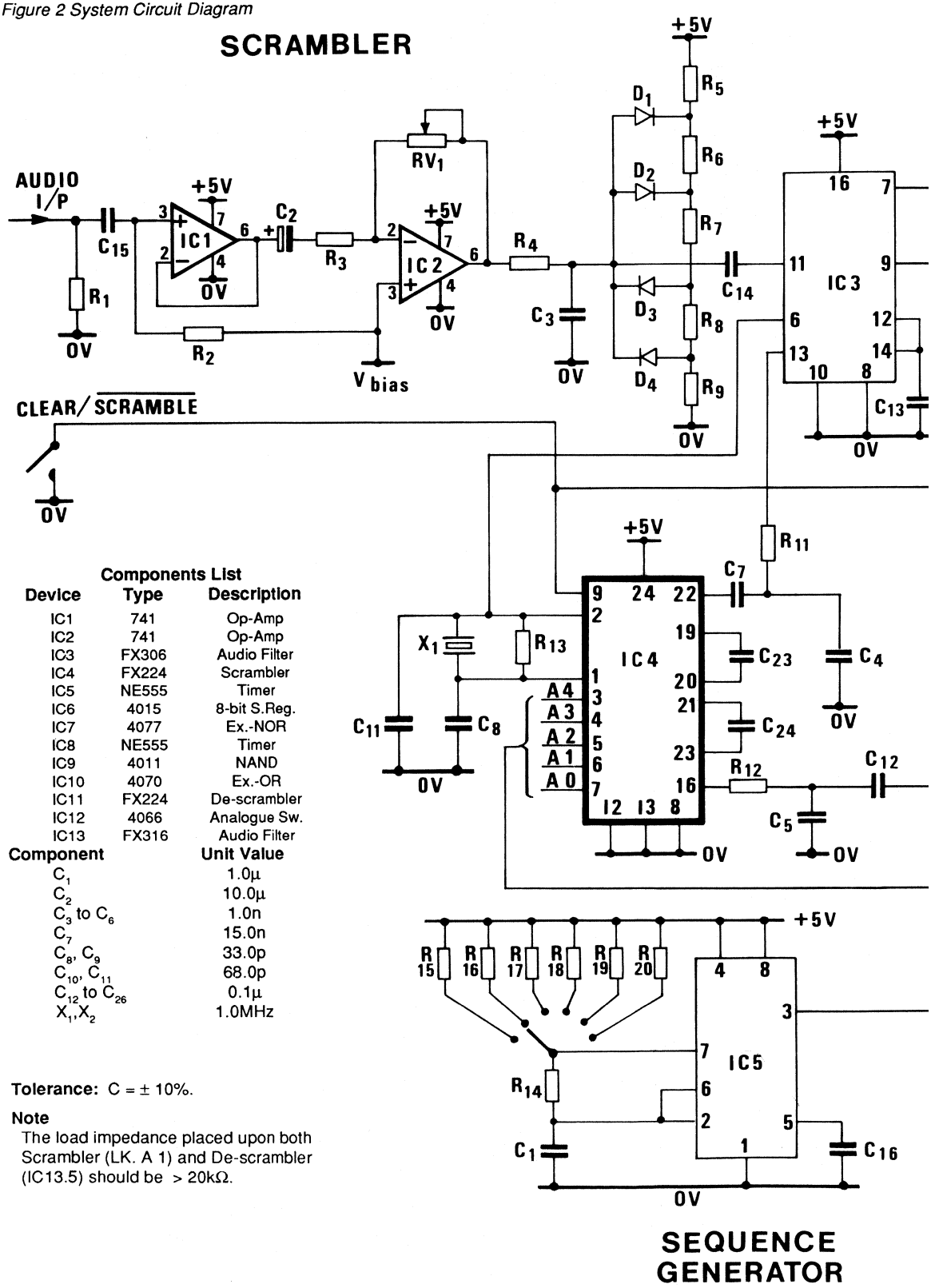
Scrambling is achieved by splitting the input voice frequencies into upper and lower frequency bands using switched capacitor filters, modulating each band with a separate carrier frequency to "frequency invert" the bands, then summing the output.
De-scrambling is carried out using the same method ensuring that the carrier frequencies are the same as those used to scramble the original audio.
Using the FX224 a total of 32 different split-point and carrier frequency combinations are externally programmable using a 5-bit code which can be fixed or varying (Rolling), for greater security.

This application note, used with a current FX224 Data Sheet, is intended to assist in integrating the device into audio circuitry by giving details of:

**(a)** The transmission (scramble) circuit.
**(b)** The reception (de-scramble) circuit.
**(c)** A Pseudo-Random Code Generator with switchable clock circuitry controlling the 'rolling' (change) rate of the 5-bit pseudo-random code at the rates of : 0.2Hz, 1.0Hz, 3.0Hz, 5.0Hz, 8.0Hz and 10.0Hz.

Synchronization of the scrambling and de-scrambling devices is important and can be accomplished by using either FSK data bursts or continuous outband tone signals.
The power requirement of this particular application is between 50 and 60 mA at 5 volts, per Tx/Rx pair, ie. one circuit.

*Figure 2 System Circuit Diagram*




**Components List**

| Device | Type | Description |
|---|---|---|
| IC1 | 741 | Op-Amp |
| IC2 | 741 | Op-Amp |
| IC3 | FX306 | Audio Filter |
| IC4 | FX224 | Scrambler |
| IC5 | NE555 | Timer |
| IC6 | 4015 | 8-bit S.Reg. |
| IC7 | 4077 | Ex.-NOR |
| IC8 | NE555 | Timer |
| IC9 | 4011 | NAND |
| IC10 | 4070 | Ex.-OR |
| IC11 | FX224 | De-scrambler |
| IC12 | 4066 | Analogue Sw. |
| IC13 | FX316 | Audio Filter |

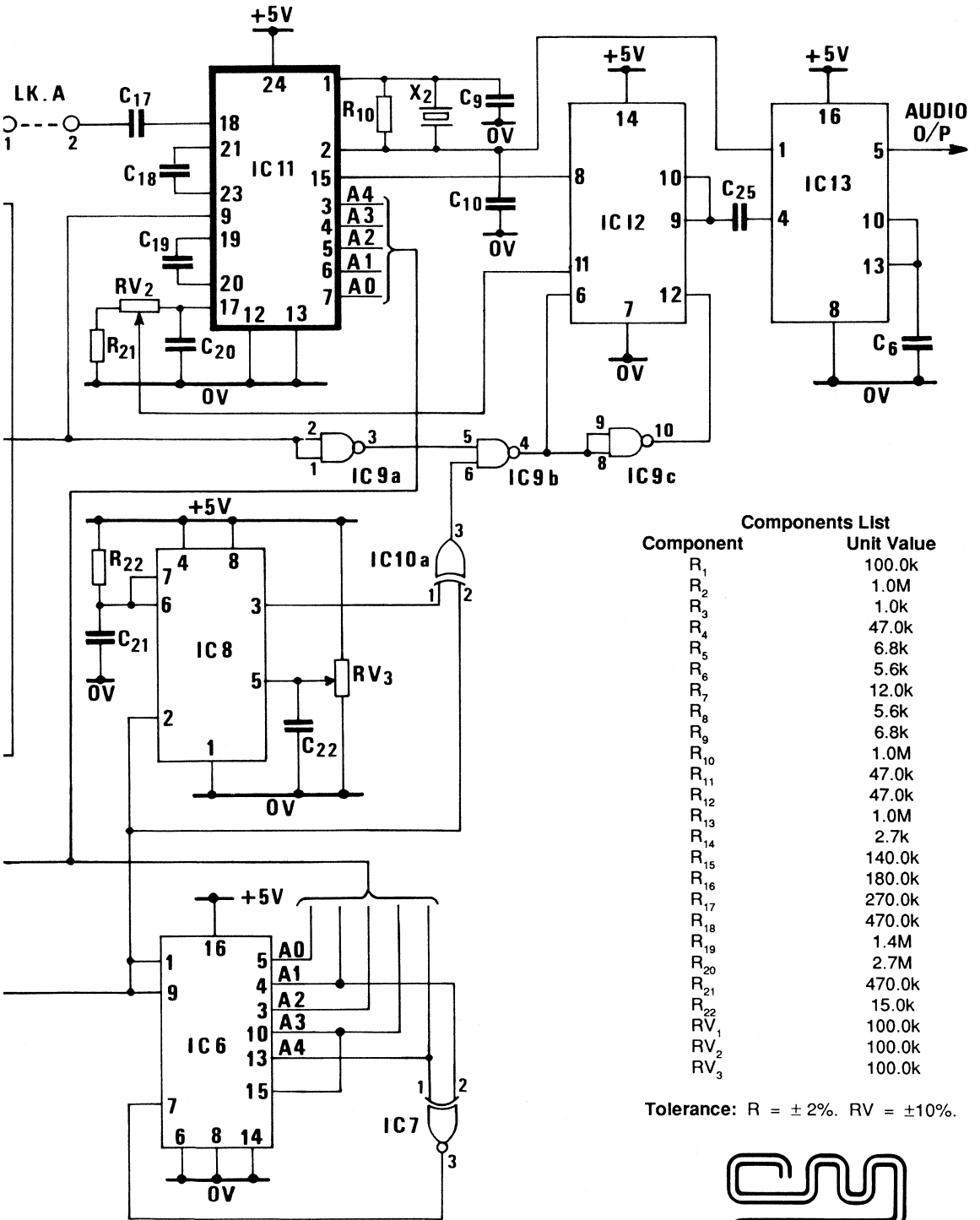
| Component | Unit Value |
|---|---|
| $C_1$ | 1.0µ |
| $C_2$ | 10.0µ |
| $C_3$ to $C_6$ | 1.0n |
| $C_7$ | 15.0n |
| $C_8$, $C_9$ | 33.0p |
| $C_{10}$, $C_{11}$ | 68.0p |
| $C_{12}$ to $C_{26}$ | 0.1µ |
| $X_1$, $X_2$ | 1.0MHz |

**Tolerance:** C = ± 10%.

**Note**

The load impedance placed upon both Scrambler (LK. A 1) and De-scrambler (IC13.5) should be > 20kΩ.

# DE-SCRAMBLER




## Components List

| Component | Unit Value |
|---|---|
| $R_1$ | 100.0k |
| $R_2$ | 1.0M |
| $R_3$ | 1.0k |
| $R_4$ | 47.0k |
| $R_5$ | 6.8k |
| $R_6$ | 5.6k |
| $R_7$ | 12.0k |
| $R_8$ | 5.6k |
| $R_9$ | 6.8k |
| $R_{10}$ | 1.0M |
| $R_{11}$ | 47.0k |
| $R_{12}$ | 47.0k |
| $R_{13}$ | 1.0M |
| $R_{14}$ | 2.7k |
| $R_{15}$ | 140.0k |
| $R_{16}$ | 180.0k |
| $R_{17}$ | 270.0k |
| $R_{18}$ | 470.0k |
| $R_{19}$ | 1.4M |
| $R_{20}$ | 2.7M |
| $R_{21}$ | 470.0k |
| $R_{22}$ | 15.0k |
| $RV_1$ | 100.0k |
| $RV_2$ | 100.0k |
| $RV_3$ | 100.0k |

**Tolerance:** R = ±2%. RV = ±10%.

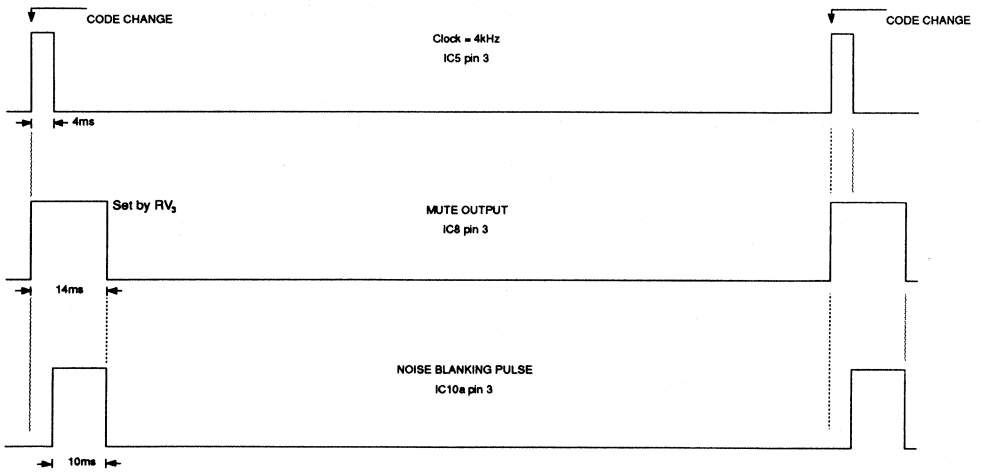



*Fig.3 Receiver Timing*

## Timing

Figure 3 (above) shows the noise blanking pulse generation and its position relative to the code change. The blanking pulse width is variable using $RV_2$ (Figure 2).

**The Circuit Diagram** – *Figure 2* – is laid out as a Scramble/De-scramble evaluation circuit with the Scrambled (unintelligable) audio available at LK.A 1. The pseudo-random code is common to both functions.

## The Scrambler Circuit

The incoming, plain, audio signal is buffered by IC1 and amplified by IC2. $RV_1$ sets a level of 300mV rms (this is found to be the optimum level to the FX224 in this application). Prior to the split-band frequency inversion process the signal is 'soft' limited to remove any high frequency spikes, then filtered to 3.4kHz by IC3 to simulate a radio channel voice bandwidth.
Using the 5-bit pseudo-random code generated by ICs 5, 6, & 7, the signal is frequency inverted by the FX224 (IC4). The inverted output of Variable Split-Band Scrambler is once again filtered (300Hz -3400Hz) by IC3, making the resulting scrambled audio compatible with a radio transmission channel. Scrambled (unintelligable) audio is available at LK.A 1.

## The De-scrambler Circuit

Frequency inverted audio (LK.A 2) is recovered using the identical pseudo-random code to that used in the scrambling process.
As is the problem with most rolling code frequency inversion systems, unwanted transients are produced in the device, at the code change. In this application, a noise blanking circuit (ICs 8, 9, 10 & 12) is utilized to remove these transients by switching the output of the analogue switch (IC12) between the de-scrambling FX224 (IC11) and a d.c. level, at the code change, for a period determined by $RV_3$. The d.c. level is approximately 60mV below the FX224 $V_{bias}$ line and is set by $RV_2$. Whilst the circuit is in the "Clear" mode, the noise blanking is disabled as it is not required.
IC13 completes the audio recovery by removing high frequency noise from the plain audio output.

## The Pseudo-Random Code Generator

Produces a random 31-step-sequence 5-bit logic code capable of change rates between 0.2Hz and10Hz. The sequence generator consists of a variable frequency oscillator (IC5) clocking a dual 4-stage shift register (IC6). By selecting a suitable Exclusive-NOR feedback arrangement using IC7, the random sequence length can be extended or modified.
**NOTE** – The code used at both Scrambler and De-scrambler must be in synchronization.

## Power Requirements

This Rolling Code Scrambler operates on a single 5v, 60mA supply.

THIS APPLICATION NOTE MUST BE READ WITH A CURRENT FX224 DATA SHEET

# Consumer Microcircuits Limited

PRODUCT INFORMATION

# FX609 Continuously Variable Slope Delta Modulation (CVSD) Codec

Publication D/609/3 March 1988
Provisional Issue

## Features/Applications

- Full Duplex CVSD Codec
- On-Chip Input and Output Filters
- Selectable 3 or 4-Bit Compand Algorithm
- Programmable Sampling Clocks
- Forced Idle Facility
- Powersave Facility
- Low Power 5V CMOS
- Digital Speech Communications
- Time Domain Scramblers
- Digital Cordless Telephone
- Voice Storage
- Digital Delay Lines
- Speech Analysis
- Multiplexers
- General Purpose

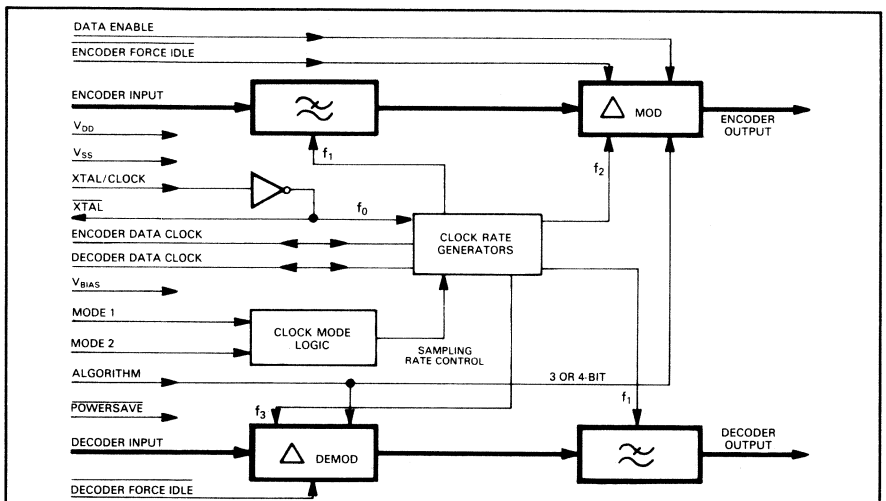



*Fig. 1 Internal Block Diagram*

**FX609**

## Brief Description

The FX609 is an LSI circuit designed as a Continuously Variable Slope Delta Modulation (CVSD) Codec and is intended for use in voice storage, time domain speech scramblers and digital speech communications equipment. Encode input and decoder output analogue filters are incorporated on-chip and use switched capacitor technology. Sampling clock rates can be programmed to 16, 32 or 64k bits/second from an internal clock generator or may be externally applied in the range 8 to 64k bits/second. Sampling clock frequencies are output for the synchronisation of external circuits. The internal clocks are derived from an on-chip reference oscillator using an externally connected crystal. The encoder has an enable function for use in multiplexer applications. When not enabled, the encoder output is high impedance (three-state). Forced idle facilities in the encoder cause a perfect 1010....output pattern and in the decoder an output voltage of $V_{DD}/2$. The companding circuits may be operated with a 3 or 4-bit algorithm which is externally selected. The device may be put into standby mode by selection of the powersave facility. The FX609 is a low power, 5 volt CMOS device and is available in 22- pin DIL, 24-pin plastic quad or 28-pin PLCC packages.

| Pin Number | | | Function |
|---|---|---|---|
| DIL FX609J | Quad Plastic FX609LG | PLCC FX609LH | |
| 1 | 1 | 1 | **Xtal/Clock:** Input to the clock oscillator inverter. A nominal 1.024MHz xtal input or externally derived clock is injected here. See Fig. 2. |
| | 2 | 2 | **No connection.** |
| 2 | 3 | 3 | **$\overline{\text{Xtal}}$:** Output of clock oscillator inverter. |
| 3 | 4 | 4 | **No Connection.** |
| 4 | 5 | 5 | **Encoder Data Clock:** A Logic I/O port. External encode clock input or internal data clock output. Clock frequency dependent upon clock mode 1, 2 inputs and xtal frequency (see **Clock Mode** pins). |
| 5 | 6 | 6 | **Encoder Output:** The encoder digital output, this is a three state output: |
| | | 7, 8 | **No Connection.** |
| 6 | 7 | 9 | **Encoder Force Idle:** When this pin is at logical '0' the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup. |
| 7 | 8 | 10 | **Data Enable:** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup. |
| 8 | 9 | 11 | **No Connection.** |
| 9 | 10 | 12 | **Bias:** Normally at $V_{DD}/2$ bias, this pin requires to be externally decoupled by a capacitor, $C_2$. Internally pulled to $V_{SS}$ when "$\overline{\text{Powersave}}$" is logical '0'. |
| 10 | 11 | 13 | **Encoder Input:** The analogue signal input. Internally biased at $V_{DD}/2$, an external 1$\mu$F input coupling capacitor, $C_1$, is required on this input. See Fig. 2 Note 3 for source impedance details. |
| 11 | 12 | 14 | **$V_{SS}$:** Negative Supply (GND). |
| 12 | 13 | 15,16 | **No connection.** |
| 13 | 14 | 17 | **Decoder Output:** The recovered analogue signal is output at this pin, it is the buffered output of a low pass filter. During "$\overline{\text{Powersave}}$" this output is o/c. |
| 14 | 15 | 18,19 | **No Connection.** |
| 15 | 16 | 20 | **$\overline{\text{Powersave}}$:** A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup. |
| | 17 | 21 | **No Connection.** |
| 16 | 18 | 22 | **Decoder Force Idle:** A logical '0' at this pin gates a 0101...pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup. |
| 17 | 19 | 23 | **Decoder Input:** Received digital signal input. Internal 1MΩ Pullup. |
| 18 | 20 | 24 | **Decoder Data Clock:** A Logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1, 2 inputs, see **Clock Mode** pins. |
| 19 | 21 | 25 | **Algorithm:** A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup. |
| 20 | 22 | 26 | **Clock Mode 2:** These inputs select encoder and decoder data clock modes. |
| 21 | 23 | 27 | **Clock Mode 1:** |
| 22 | 24 | 28 | **$V_{DD}$: Positive Supply:** A single +5 volt power supply is required. |

| Data Enable | $\overline{\text{Powersave}}$ | Encoder Output |
|---|---|---|
| 1 | 1 | Enabled |
| 0 | 1 | High Z (o/c) |
| 1 | 0 | $V_{SS}$ |

Internal 1MΩ pull-ups.

| Clock 1 | Mode 2 | |
|---|---|---|
| 0 | 0 | External Clocks |
| 0 | 1 | Internal, 64kb/s = f ÷ 16 |
| 1 | 0 | Internal, 32kb/s = f ÷ 32 |
| 1 | 1 | Internal, 16kb/s = f ÷ 64 |

Clock rates refer to f = 1.024MHz Xtal/Clock input.
During Internal Data Clock operation the data clock frequencies are available at the ports for external circuit synchronisation. Independent or Common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

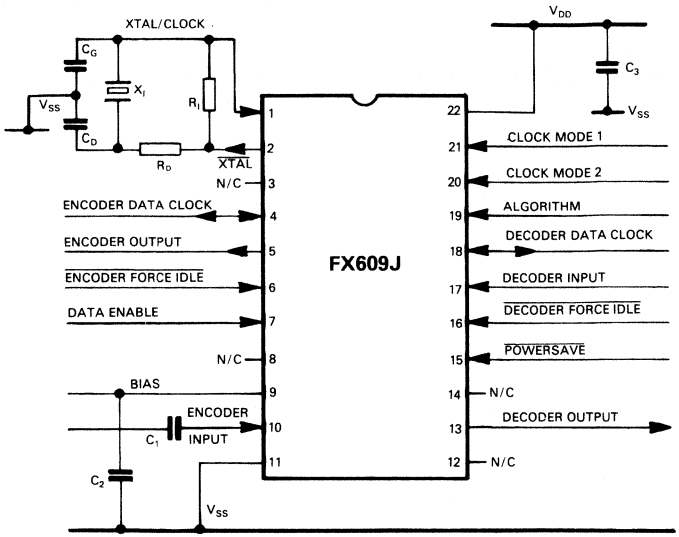



*Fig. 2 External Component Connections*

| Component References | | |
|---|---|---|
| **Component** | **Unit Value** | **Note** |
| $R_1$ | Typ. 1 M | 1 |
| $R_D$ | Selectable | 1 |
| $C_1$ | 1.0$\mu$ | |
| $C_2$ | 1.0$\mu$ | |
| $C_3$ | 1.0$\mu$ | |
| $C_D$ | Typ. 33p | 1 |
| $C_G$ | Typ. 68p | 1 |
| $X_1$ | 1.024 MHz | 1, 2 |

**Tolerance**

*Resistors* $\pm 10\%$
*Capacitors* $\pm 20\%$

**NOTES**

1. *Xtal circuitry shown is in accordance with CML application note D/XT/1 April '86.*
2. *A 1.024 MHz clock/xtal input will yield exactly 16/32/64 kb/s data clock rates.*
3. *To prevent unwanted internal oscillations at the encoder input pin, the source impedance to this input must be less than 100Ω. Output noise levels will improve with even lower source impedances.*

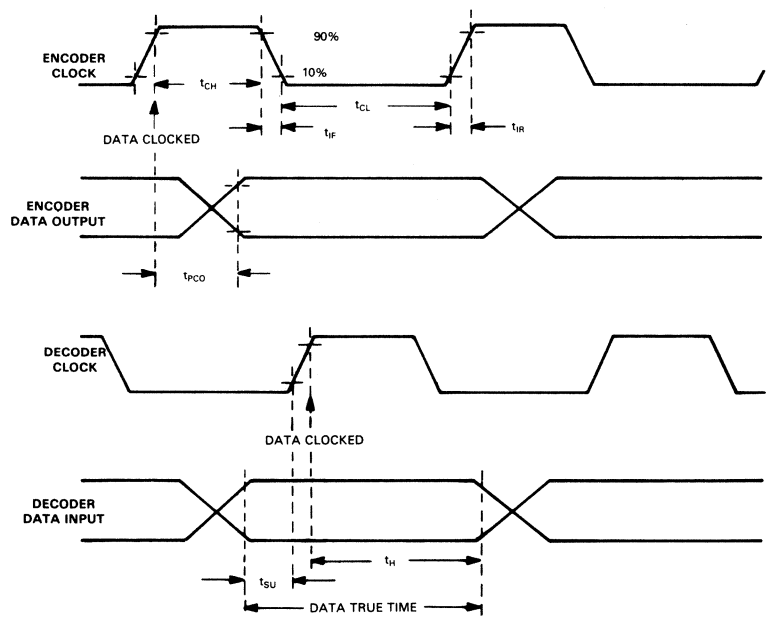



*Fig. 3 Codec Timing Diagrams*

**TIMING**

$t_{CH}$ *Clock '1' Pulse Widths 1µs Min.*

$t_{CL}$ *Clock '0' Pulse Widths 1µs Min.*

$t_{IR}$ *Clock Rise Time 100ns Typ.*

$t_{IF}$ *Clock Fall Time 100ns Typ.*

$t_{SU}$ *Data Set-up Time 450ns Max.*

$t_H$ *Data Hold Time 600ns Min.*

$t_{SU} + t_H$ *Data True Time*

$t_{PCO}$ *Clock to Output Delay Time = 750ns Max.*
*Xtal input 1.024 MHz.*

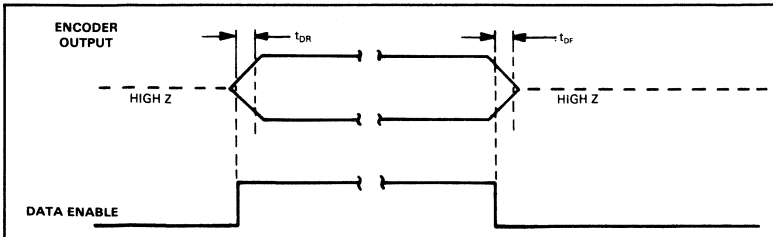



*Fig. 4 Multiplexing Function*

**TIMING**

$t_{DR}$ *Data Rise Time 100ns Typ.*

$t_{DF}$ *Data Fall Time 100ns Typ.*

# Specifications

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3 to ($V_{DD}$ + 0.3V) |
| Output sink/source current (supply pins) | | ±30mA |
| (other pins) | | ±20mA |
| Total device dissipation @ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX609J** | −30°C to +85°C (Ceramic) |
| | **FX609LG/LH** | −30°C to +70°C (Plastic) |
| Storage temperature range: | **FX609J** | −55°C to +125°C (Ceramic) |
| | **FX609LG/LH** | −40°C to +85°C (Plastic) |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

$V_{DD}$ = 5V, $T_{amb}$ = 25°C, Xtal/Clock (f) = 1.024 MHz, Sample Rate 32kb/s.
[Standard Test Signal 820Hz, ref. 0dB = 489mV (rms)]

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | 1 | 4.5 | 5.0 | 5.5 | V |
| Supply Current (Enabled) | | — | 3.5 | — | mA |
| Supply Current (Powersave) | | — | 500 | — | μA |
| Inputs Logic '1' | | 3.5 | — | — | V |
| Inputs Logic '0' | | — | — | 1.5 | V |
| Outputs Logic '1' | | 4.0 | — | — | V |
| Outputs Logic '0' | | — | — | 1.0 | V |
| Digital Input Impedance (logic I/O pins) | | — | 10 | — | MΩ |
| Digital Input Impedance (logic input pins, pullup resistor) | 2 | 300 | — | — | kΩ |
| Digital Output Impedance | | — | 4 | — | kΩ |
| Analogue Input Impedance | | — | 100 | — | kΩ |
| Analogue Output Impedance | | — | 800 | — | Ω |
| Three State Output leakage Current (output disabled) | | — | ±4 | — | μA |
| Insertion Loss | | — | 0 | — | dB |
| **Dynamic Values** | 1 | | | | |
| **Encoder:** | | | | | |
| Analogue Signal Input levels | 5 | −30 | — | +8 | dB |
| Principal Integrator Frequency | | — | 275 | — | Hz |
| Encoder Passband | | | 3400 | | Hz |
| Compand Time Constant | | — | 4 | — | ms |
| **Decoder:** | | | | | |
| Analogue Signal Output levels | 5 | −30 | — | +8 | dB |
| Decoder Passband | | 300 | — | 3400 | Hz |
| **Encoder Decoder (Full codec):** | | | | | |
| Passband | | 300 | — | 3400 | Hz |
| Stopband | | 6 | — | 10 | kHz |
| Stopband Attenuation | | — | 60 | — | dB |
| Passband Gain | | — | 0 | — | dB |
| Passband Ripple | | −3 | — | +3 | dB |
| Output Noise (Input short circuit) | | — | −60 | — | dB |
| Perfect Idle Channel Noise (Encode Forced) | | — | −63 | — | dB |
| Group Delay Distortion | 3 | | | | |
| 1000 − 2600Hz | | — | — | 450 | μs |
| 600 − 2800Hz | | — | — | 750 | μs |
| 500 − 3000Hz | | — | — | 1.5 | ms |
| Xtal/Clock Frequency | | 500 | 1024 | 1500 | kHz |

**Notes:**
1. *Dynamic characteristics specified at 5V only.*
2. *All logic Inputs except, Encoder and Decoder Data Clocks.*
3. *Group delay distortion for full codec relative to the delay at 820Hz, −20dB at the encoder input.*
4. *Relative timings are shown on Figures 3 and 4.*
5. *Recommended values—see graph Fig. 7.*

## Codec Performance

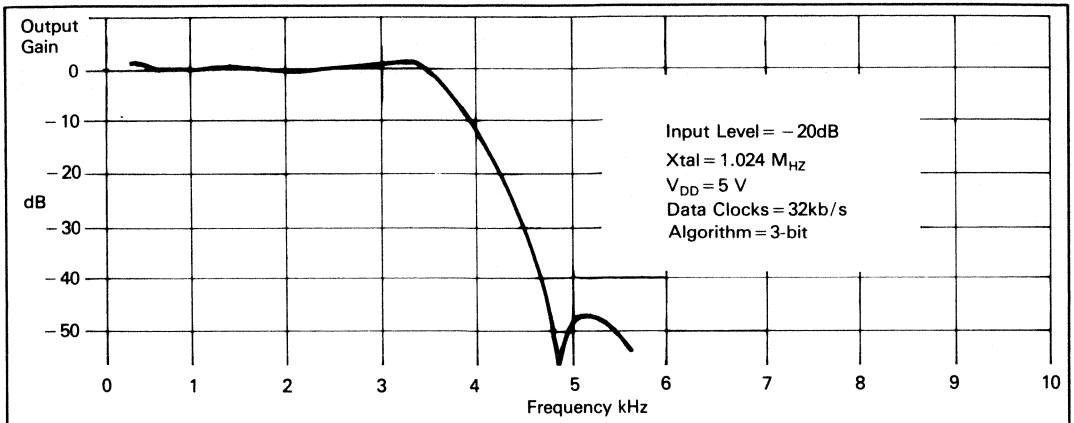



*Fig. 5 Typical Codec Frequency Response*

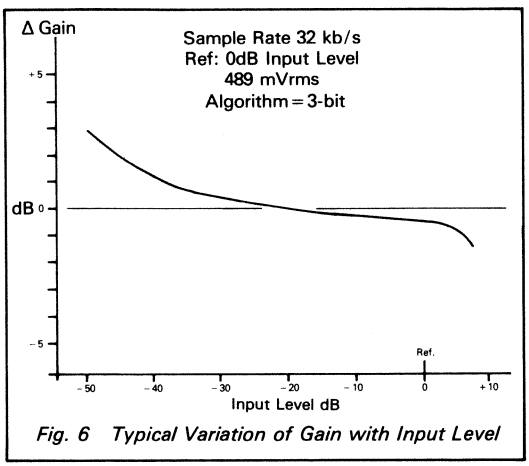



*Fig. 6 Typical Variation of Gain with Input Level*

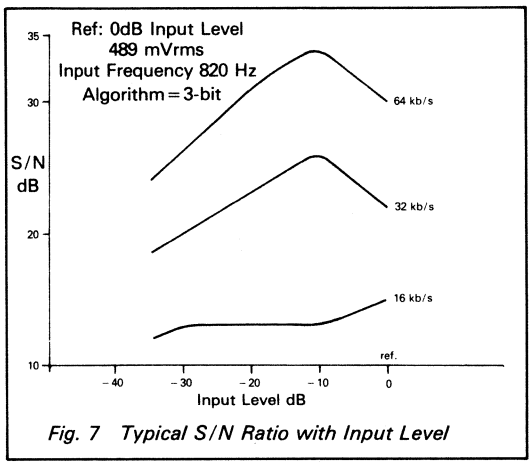



*Fig. 7 Typical S/N Ratio with Input Level*

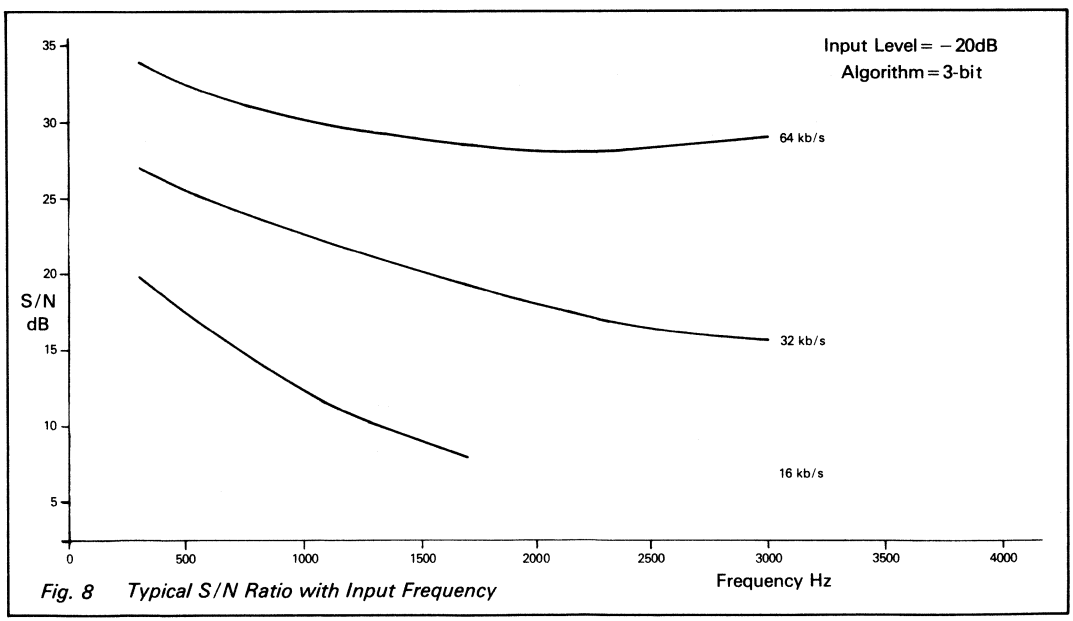


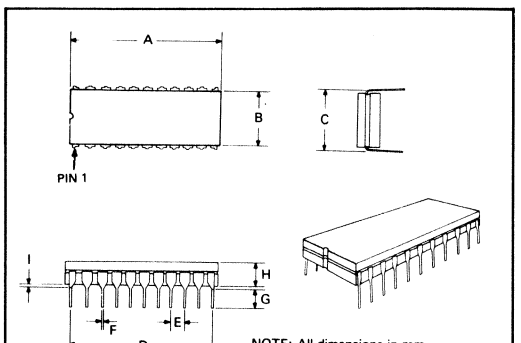

*Fig. 8 Typical S/N Ratio with Input Frequency*

## Package Outlines

The FX609J, the cerdip package, is illustrated in *Figure 9*. The 'LG' version is shown in *Figure 10*, and the 'LH' version in *Figure 11*.

To allow complete identification, the FX609 LG and LH packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4 for LG package, between pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 9* **FX609J** *22-pin DIL Package*



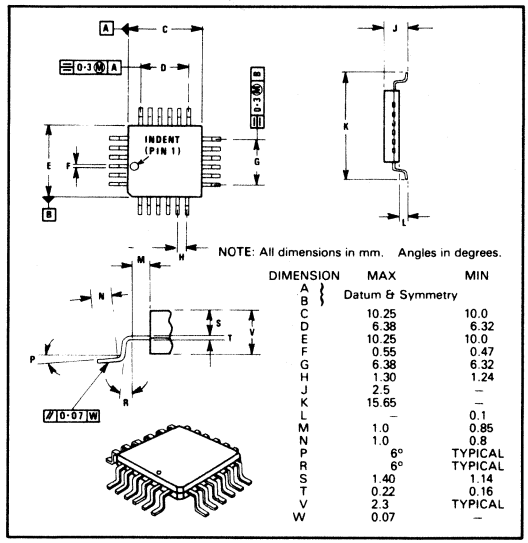

NOTE: All dimensions in mm.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 | TYPICAL DIMENSION |
| F | 0.46 | |
| G | 4.35 | |
| H | 4.27 | 3.99 |
| I | — | 0.5 |

## Handling Precautions

The FX609J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

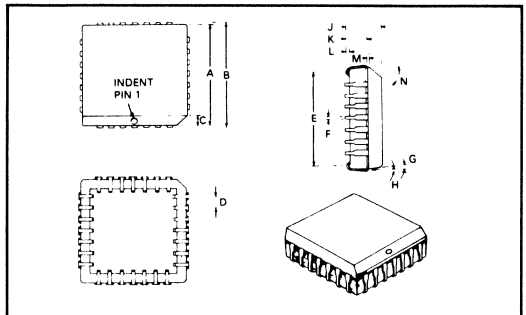
*Fig. 10* **FX609LG** *24-pin Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | — |
| K | 15.65 | — |
| L | — | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | — |

*Fig. 11* **FX609LH** *28-lead Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 11.6 | 11.4 |
| B | 12.6 | 12.3 |
| C | 1.1 x 45° | TYPICAL |
| D | 1.3 | TYPICAL |
| E | 10.8 | 10.0 |
| F | 0.46 | TYPICAL |
| G | 7° | 3° |
| H | 7° | 3° |
| J | 4.5 | 4.3 |
| K | 2.5 | TYPICAL |
| L | 1.1 | 0.5 |
| M | 0.59 | TYPICAL |
| N | 45° | TYPICAL |

## Ordering Information

**FX609J** **22-pin cerdip DIL**

**FX609LG** **24-pin quad plastic encapsulated, bent and cropped.**

**FX609LH** **28-lead Plastic leaded chip carrier.**

# Consumer Microcircuits Limited

PRODUCT INFORMATION

# FX709 Voice Store Retrieve CVSD Codec

Publication D/709/5 February 1993
Provisional Issue

## Features/Applications

- CVSD Encode + Decode
- Programmable Clock Rates
- Programmable Voice Filters
- Voice Power Output
- Voice Spectrum Monitor
- 8-bit Memory/Instruction I/O
- Processor Interface
- Voice Message Mailbox
- Status Annunciators
- Re-try Message Forward
- Voice Security Scrambling
- Voice Data Communications
- Time/Frequency Companding
- Audio Delay Functions

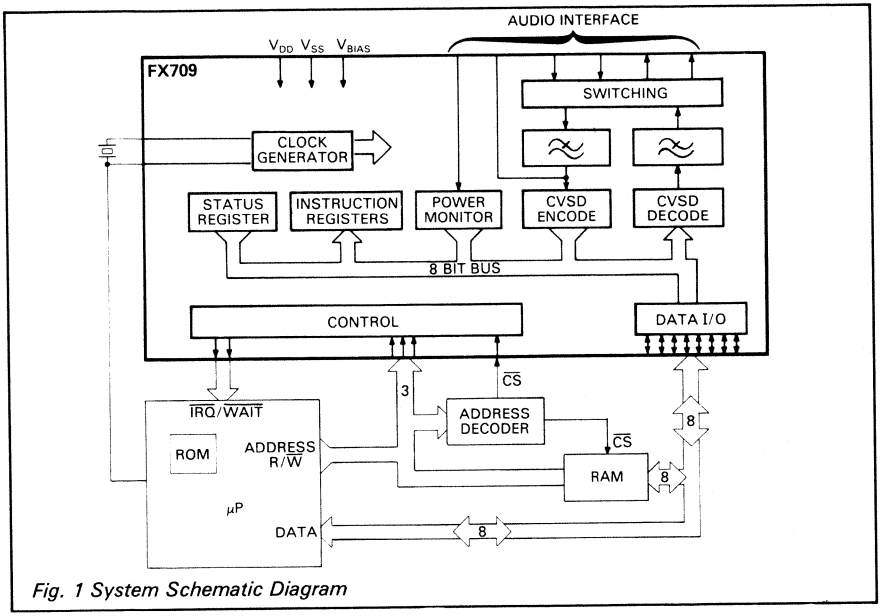



*Fig. 1 System Schematic Diagram*

FX709

## Brief Description

The FX709 is an audio-digital interface codec for microprocessor controlled Voice Store and Retrieve applications.

In encode, audio input signals are band-limited by a lowpass filter and digitised by a CVSD 1-bit serial encoder. After conversion to 8-bit parallel format, encoded data is read to the I/O bus for storage in memory.

In decode, memory contents written into the I/O port are converted back to 1-bit serial form and decoded by a CVSD decoder. The decoder output is lowpass filtered and output as retrieved audio.

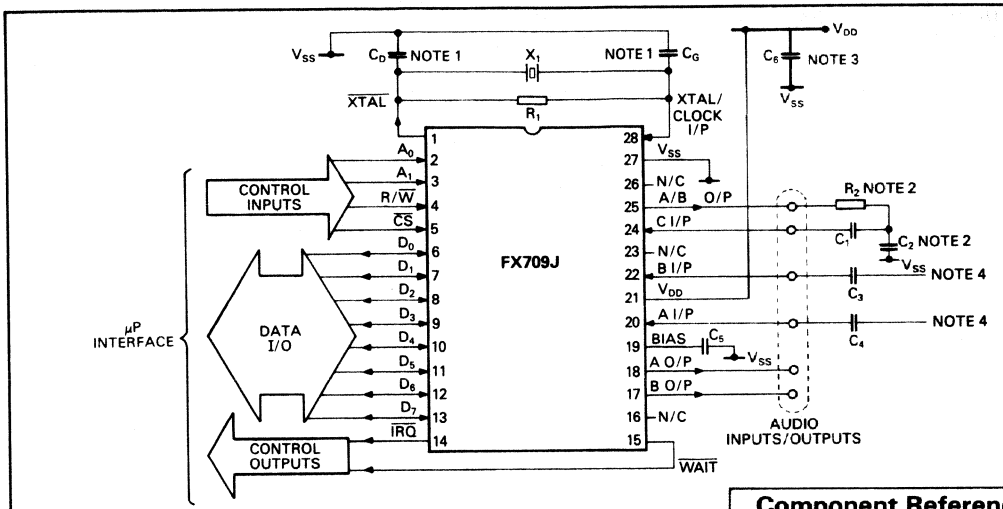
The audio encode/decode functions are independently controlled, permitting concurrent or asynchronous VSR operations to be performed. Time and frequency companding is available via independently programmable encode/decode data rates and filter cut-offs.

Support for VOX functions and 'Pause' memory management is provided by the power assessment register.

This contains two 4-bit numbers representing the average signal levels into the data encoder and a replica encoder over a programmable averaging period.

The device instruction set includes input/output signal switching and a standby powerdown function. The FX709 is a lowpower CMOS circuit and uses a single 5 volt supply.

| Pin Number FX709J/LH | Function |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** Output of clock oscillator inverter. |
| 2<br>3<br>4 | **$A_0$:**<br>**$A_1$:** These pins determine which register may be addressed via the I/0 port.<br>**R/$\overline{W}$:**<br>$A_0$ $A_1$ R/$\overline{W}$ **Register**<br>0 0 0 'A' instruction<br>1 0 0 'B' instruction<br>0 1 0 Decoder<br>1 1 0 No Register<br>0 0 1 Status<br>1 0 1 Power<br>0 1 1 Encoder<br>1 1 1 No Register |
| 5 | **$\overline{\text{CS}}$:** Chip Select input, this input has a 1 MΩ pullup to $V_{DD}$. |
| 6<br>7<br>8<br>9<br>10<br>11<br>12<br>13 | **$D_0$:**<br>**$D_1$:**<br>**$D_2$:**<br>**$D_3$:** **I/0 Port**<br>**$D_4$:**<br>**$D_5$:**<br>**$D_6$:**<br>**$D_7$:** |
| 14 | **$\overline{\text{IRQ}}$:** Interrupt Request Output, this pin is the output of the interrupt request generator. This device can be "wire OR'd" with other active-low components. See section on Interrupt Requests. (100kΩ internal pullup to $V_{DD}$). |
| 15 | **$\overline{\text{WAIT}}$ Output:** The circuit requires a minimum Chip Select time of $t_{ACS}$. If the host µP has a CS time of less than this the WAIT output must be used to delay the µP when accessing the FX709. (See Figure 7). (100kΩ internal pullup to $V_{DD}$).<br>*NOTE:* If the WAIT output is to be used, then to prevent spurious operation of this function during Power-Up, it is recommended that:<br>a: Power-Up of the FX709 is delayed until µP Power-Up is complete, or,<br>b: The Chip Select input is held open-circuit during the FX709 Power-Up sequence. |
| 16 | No connection. |
| 17 | **Analogue Output B:** (See Figure 4). |
| 18 | **Analogue Output A:** (See Figure 4). |
| 19 | **$V_{BIAS}$:** The bias or analogue ground pin and is internally set to $V_{DD}/2$. It should be decoupled to $V_{SS}$ with a capacitor of 1.0µF (min.). |
| 20 | **Analogue Input A:** (See Figure 2, Note 4 and Figure 4). |
| 21 | **$V_{DD}$:** Positive Supply. |
| 22 | **Analogue Input B:** (See Figure 2, Note 4 and Figure 4). |
| 23 | No connection. |
| 24 | **Analogue Input C:** This is the analogue input to the power encoder. |
| 25 | **Analogue Output A/B:** (See Figure 4). |
| 26 | No connection. |
| 27 | **$V_{SS}$:** Negative supply. |
| 28 | **Xtal/Clock Input:** This is the input to the clock oscillator inverter. A 1.0 MHz Xtal input or externally derived clock is injected at this pin. |




**NOTES:**

1. *$C_G$ used to reduce voltage overshoot. Refer to CML Crystal application Applications Note D/XT/1 April 86.*
2. *$R_2$, $C_2$ forms a lowpass filter input to 'C' input power assessment circuit. The values shown represent a 820Hz lowpass although other cutoff frequencies may be selected depending on the application — see page 9.*
3. *Additional decoupling may be necessary for noisy supplies.*
4. *To prevent unwanted internal oscillations at the Encoder input pins, the source impedance to these inputs must be less than 100Ω. Output idle channel noise levels will improve with even lower source impedances.*

**Component References**

| Component | Unit Value | Tolerance |
|---|---|---|
| $R_1$ | >1M | ±10% |
| $R_2$ | 5.6k | ±10% |
| $C_G$ | 68p | Note 1 |
| $C_D$ | 33p | Note 1 |
| $C_1$ | 0.1μ | ±20% |
| $C_2$ | 33n | ±20% |
| $C_3$ | 0.1μ | ±20% |
| $C_4$ | 0.1μ | ±20% |
| $C_5$ | 1.0μ min | ±20% |
| $C_6$ | 0.1μ | ±20% |

*Fig. 2 External Component Connections*

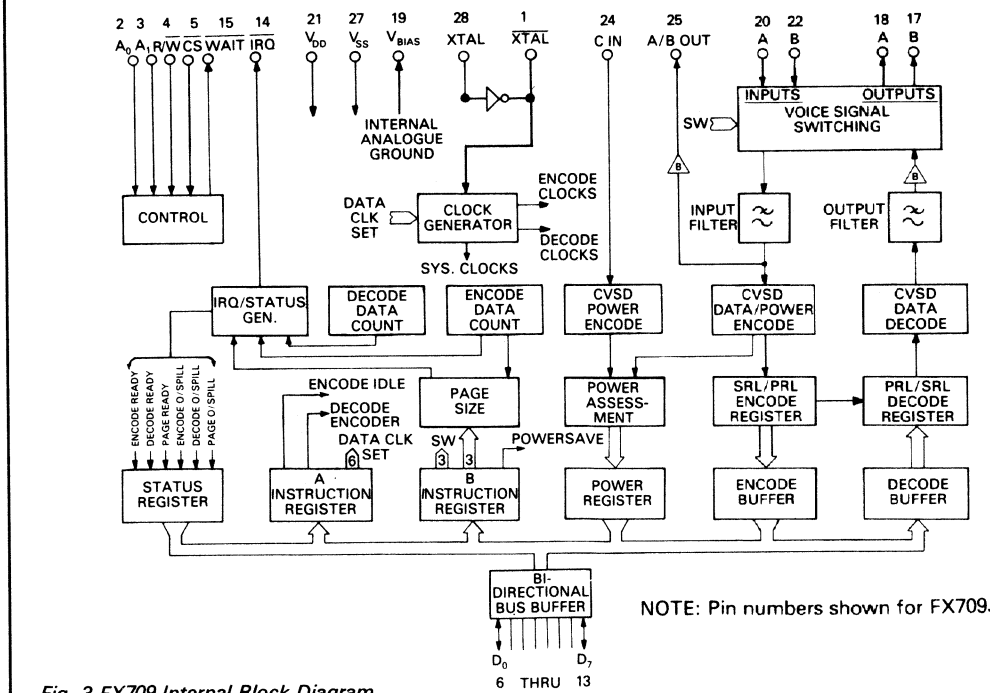
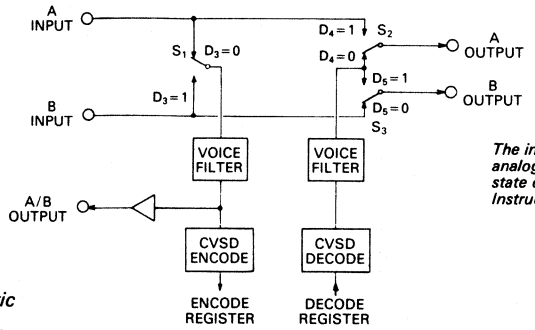



*Fig. 3 FX709 Internal Block Diagram*

## Analogue Switching




*The input and output switching of analogue signals is controlled by the state of bit no's $D_3$, $D_4$ and $D_5$ in Instruction Register B.*

*Fig. 4 Audio Switching — Simplified Block Schematic*

**Frequency and Data Rate Control**

Six bits of Instruction Register A ($D_2 - D_7$) control the data rates of the encoder and decoder and the bandwidths of the filters for the encoder and decoder. The configuration of the frequency dividers is as shown in the diagrams below and obtainable combinations of frequencies with various input clocks are listed.

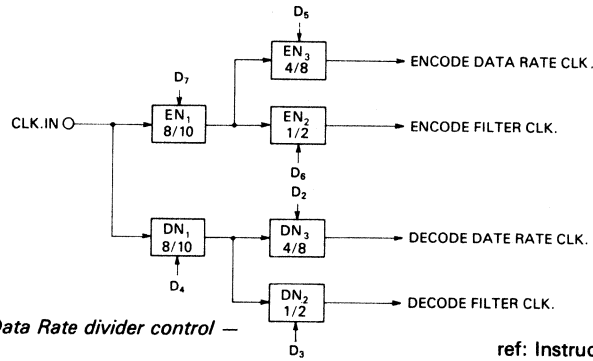



*Fig. 5 Filter Clock and Data Rate divider control — Block diagram*

ref: Instruction Register 'A'

| CLOCK INPUT | N1 | N2 | FILTER CLOCK (Hz) | LOWPASS FILTER BW PB. ± 1dB | N3 | DATA CLOCK (kbs) |
|---|---|---|---|---|---|---|
| 2MHz | 8 | 2 | 125k | 3320 | 4 | 62.5 |
| ,, | 8 | 2 | 125k | 3320 | 8 | 31.25 |
| ,, | 10 | 2 | 100k | 2656 | 4 | 50.0 |
| ,, | 10 | 2 | 100k | 2656 | 8 | 25.0 |
| 1MHz | 8 | 1 | 125k | 3320 | 4 | 31.25 |
| ,, | 8 | 1 | 125k | 3320 | 8 | 15.625 |
| ,, | 8 | 2 | 62.5k | 1660 | 4 | 31.25* |
| ,, | 8 | 2 | 62.5k | 1660 | 8 | 15.625* |
| ,, | 10 | 1 | 100k | 2656 | 4 | 25.0 |
| ,, | 10 | 1 | 100k | 2656 | 8 | 12.5 |
| ,, | 10 | 2 | 50k | 1328 | 4 | 25.0* |
| ,, | 10 | 2 | 50k | 1328 | 8 | 12.5* |
| 2.048MHz | 8 | 2 | 128k | 3400 | 4 | 64.0 |
| ,, | 8 | 2 | 128k | 3400 | 8 | 32.0 |
| ,, | 10 | 2 | 102.4k | 2720 | 4 | 51.2 |
| ,, | 10 | 2 | 102.4k | 2720 | 8 | 25.6 |
| 1.024MHz | 8 | 1 | 128k | 3400 | 4 | 32.0 |
| ,, | 8 | 1 | 128k | 3400 | 8 | 16.0 |
| ,, | 8 | 2 | 64k | 1700 | 4 | 32.0* |
| ,, | 8 | 2 | 64k | 1700 | 8 | 16.0* |
| ,, | 10 | 1 | 102.4k | 2720 | 4 | 25.6 |
| ,, | 10 | 1 | 102.4k | 2720 | 8 | 12.6 |
| ,, | 10 | 2 | 51.2k | 1360 | 4 | 25.6* |
| ,, | 10 | 2 | 51.2k | 1360 | 8 | 12.6* |
| 614.4kHz | 8 | 1 | 76.8k | 2040 | 8 | 9.6* |
| 768.0kHz | 10 | 1 | 76.8k | 2040 | 8 | 9.6* |

***Caution:** Although possible, the Codec insertion loss is not according to the specification at these settings.
(see Page 10).

*Table 1 Possible combinations of clock input frequency, filter cutoff (Hz) and Data Clock (kbs)*

## Register Truth Tables

The following tables describe the function of each bit within each register. 'Address Input' logic states are shown in the top right hand corner of each table. The following registers are described below:



| IRA | INSTRUCTION REGISTER 'A' | | | $A_0 = 0$<br>$A_1 = 0$<br>$R/\overline{W} = 0$ |
|---|---|---|---|---|
| **Bit** | **Function Name** | **Logic State** | **References** | **NOTES** |
| $D_0$ | Encoder Idle | | $SRD_3$ | $D_0$ sets the encoder idle/normal mode of operation. |
| | | 1 | | **FORCED:** Forces the encode register to fill with a 1010101... idle pattern. *Note: incoming encoded data is still available for the power assessment circuits.* |
| | | 0 | | **NORMAL:** Allows the encode register to fill with encoded data. Data is transferred to the encode buffer during the last bit of the encode byte. |
| $D_1$ | Decoder Data Source In Overspill | | $SRD_4$ | $D_1$ determines the source of data for the decoder. |
| | | 1 | | **ENCODER:** Internally connects the output of the encode register to the input of the decode register. This condition effectively connects the audio straight through. The encoded data may still be accessed via the encode buffer, and I/O port. |
| | | 0 | | Fills the decode register with idle pattern. In either case data may be loaded into the decode register via the I/O port. This automatically overwrites the current contents of the decode register. |
| $D_2$ | Decode Data Rate Clock Divider | | Fig. 5 Table 1 | $D_2$ sets the Decode data rate divider. |
| | | 1 | | ÷ 8 |
| | | 0 | | ÷ 4 |
| $D_3$ | Decode Filter Clock Divider | | Fig. 5 Table 1 | $D_3$ sets the Decode Filter Clock Divider and hence the Filter Cut-off Frequency. |
| | | 1 | | ÷ 2 |
| | | 0 | | ÷ 1 |
| $D_4$ | Decode Master Clock Divider | | Fig. 5 Table 1 | $D_4$ sets the Decode Master clock divider. |
| | | 1 | | ÷ 10 |
| | | 0 | | ÷ 8 |

| IRA | INSTRUCTION REGISTER 'A' | | | $A_0$ = 0<br>$A_1$ = 0<br>R/$\overline{W}$ = 0 |
|---|---|---|---|---|
| **Bit** | **Function Name** | **Logic State** | **References** | **NOTES** |
| $D_5$ | Encode Data Rate Divider | 1<br>0 | Fig. 5<br>Table 1 | $D_5$ sets the Encode Data Rate Divider.<br>÷ 8<br>÷ 4 |
| $D_6$ | Encode Filter Clock Divider | 1<br>0 | Fig. 5<br>Table 1 | $D_6$ sets the Encode Filter Clock Divider and hence the filter cut-off frequency.<br>÷ 2<br>÷ 1 |
| $D_7$ | Encode Master Clock Divider | 1<br>0 | Fig. 5<br>Table 1 | $D_7$ sets the Encode Master Clock Divider.<br>÷ 10<br>÷ 8 |

| IRB | INSTRUCTION REGISTER 'B' | | | $A_0$ = 1<br>$A_1$ = 0<br>R/$\overline{W}$ = 0 |
|---|---|---|---|---|
| **Bit** | **Function Name** | **Logic State** | **References** | **NOTES** |
| $D_0$<br>$D_1$<br>$D_2$ | Page<br>Size<br>Set | See Notes | | $D_0 - D_2$ set the "page size" in Encode Data bytes. (one byte = 8 serial data bits) in accordance with the table below: |

| $D_2$ | $D_1$ | $D_0$ | : | PAGE BYTES | Page Period @32kbs |
|---|---|---|---|---|---|
| 0 | 0 | 0 | : | 32 | 8ms |
| 0 | 0 | 1 | : | 64 | 16ms |
| 0 | 1 | 0 | : | 96 | 24ms |
| 0 | 1 | 1 | : | 128 | 32ms |
| 1 | 0 | 0 | : | 160 | 40ms |
| 1 | 0 | 1 | : | 192 | 48ms |
| 1 | 1 | 0 | : | 224 | 56ms |
| 1 | 1 | 1 | : | 256 | 64ms |

Page Period (secs) = 8 x Page Bytes/Data Rate (b/s)

| | | | | |
|---|---|---|---|---|
| $D_3$ | "A/B" Encode | 0<br>1 | Fig. 4 | $D_3$ defines which audio input A or B is connected to the encoder via the encode filter. (See fig. 4).<br>**AUDIO INPUT "A"**: Internally connects the "A" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "A". Audio input "B" set to $V_{DD}/2$.<br>**AUDIO INPUT "B"**: Internally connects the "B" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "B". Audio input "A" set to $V_{DD}/2$. |

| IRB | INSTRUCTION REGISTER 'B' | | | $A_0$ = 1<br>$A_1$ = 0<br>R/$\overline{W}$ = 0 |
|---|---|---|---|---|
| **Bit** | **Function Name** | **Logic State** | **References** | **NOTES** |
| $D_4$ | Switch Audio Output<br><br>"A" | <br><br>1<br>0 | Fig. 4 | $D_4$ controls the Output Audio Switch to determine which source audio is connected to Audio Output "A" pin.<br><br>Input "A" to Output "A" (direct).<br>Decoder to Output "A". |
| $D_5$ | Switch Audio Output<br><br>"B" | <br><br>1<br>0 | Fig. 4 | $D_5$ controls the Output Audio Switch to determine which source audio is connected to Audio Output "B" pin.<br><br>Decoder to Output "B"<br>Input "B" to Output "B" (direct). |
| $D_6$ | Powersave | <br><br>1<br><br>0 | | $D_6$ controls the enablement and disablement of all analogue circuit elements.<br>**POWERSAVE MODE:** Disables the circuit elements, thereby effectively reducing current consumption.<br><br>**OPERATING MODE:** All circuit elements enabled.<br><br>**NOTE:** During POWERSAVE, inputs are biased $V_{DD}/2$. Outputs are biased $V_{DD}/2$ if IRB $D_4/D_5$ are set to "direct". |
| $D_7$ | Power Sensitivity | <br><br>1<br><br>0 | | $D_7$ determines the sensitivity range of the power measuring circuits.<br>**HIGH:** Low power input, assessment circuits have + 12dB gain over LOW Setting.<br><br>**LOW:** Normal power assessment sensitivity range.<br><br>**NOTE:** High input levels in the HIGH condition may lead to overflow, producing an ambiguous reading. |

| SR | STATUS REGISTER | | | $A_0$ = 0<br>$A_1$ = 0<br>R/$\overline{W}$ = 1 |
|---|---|---|---|---|
| **Bit** | **Function Name** | **Logic State** | **References** | **NOTES** |
| $D_0$ | Encode Data Ready | 1 | | $D_0$ indicates that a byte of data has been encoded and can be read from the encode buffer.<br>**READ BYTE:** Set high during the last bit of the byte shifted into the encode register. This condition causes an interrupt request. |
| | | 0 | | **NOT READY/OVERSPILL:** This condition occurs when:<br>1. The last data byte in the encode data register has been read.<br>2. Encode data overspill bit = 1 ie. $SRD_3 = 1$. |
| $D_1$ | Decode Data Ready | 1 | $SRD_4$ | $D_1$ indicates that a byte of data has been decoded and a new byte should be written to the decode buffer.<br>**WRITE BYTE:** This condition occurs when the decode register has been loaded from its buffer, i.e. after the last bit of the previous byte has been clocked out of the register. |
| | | 0 | | **NOT READY/OVERSPILL:** This condition occurs when data has been written into the decode buffer or the decode data overspill condition is valid ($SRD_4 = 1$). |
| $D_2$ | Page Ready | 1 | | This bit indicates that a page of bytes has been encoded.<br>**READ PAGE:** This condition occurs when the page counter has completed the last byte of a page. This is after power measurements have been written into $PRD_0$ to $PRD_7$ inclusive. |
| | | 0 | $SRD_5$ | **NOT READY/OVERSPILL:** This condition occurs when Power Register "PR" has been read or the page overspill condition is valid. |
| $D_3$ | Encode Overspill | 1 | | **OVERSPILL:** Indicates that the encode data was not read between two consecutive "encode data ready" flags. Encoded data bytes have been lost, and no further bytes will be transferred to the encode buffer. |
| | | 0 | | **NORMAL:** This condition occurs when data has been read from the encode buffer, following a data ready flag, $SRD_0 = 1$, or by writing to the decode buffer if both encode and decode overspill bits are set. (See 'Interrupts' page 9). |
| $D_4$ | Decode Overspill | 1 | | **OVERSPILL:** When this bit is set data transfer from the decode buffer to the decode register is inhibited. If the "DECODER/ENCODER BUS" ($IRAD_1$) is not set then the decode register will fill with idle pattern. |
| | | 0 | | **NORMAL:** This condition occurs when data has been written to the decode buffer following a data ready flag, $SRD_1 = 1$ or by reading the contents of the encode buffer if both encode and decode overspill bits are set. (See 'Interrupts' page 9). |

| SR | STATUS REGISTER | | | $A_0 = 0$<br>$A_1 = 0$<br>$R/\overline{W} = 1$ |
|---|---|---|---|---|
| **Bit** | **Function Name** | **Logic State** | **References** | **NOTES** |
| $D_5$ | Page Overspill | 1 | | **OVERSPILL:** This state indicates that the power register was not read before the next page was completed. |
| | | 0 | | **NORMAL:** Power register "read" or IRB written. |

| PR | POWER REGISTER | | $A_0 = 1$<br>$A_1 = 0$<br>$R/\overline{W} = 1$ |
|---|---|---|---|
| **Bit** | **Function Name** | **Logic State** | **NOTES** |
| $D_0$<br>$D_1$<br>$D_2$<br>$D_3$ | "A/B" Power LSB<br>"A/B" Power MSB | | $D_0 - D_3$ represent the average signal level of the last page of data in the range from +6dBm to −24dBm (at 1kHz) for the A or B input. The relationship between binary value and signal level is frequency dependant and exhibits pre-emphasis characteristics. (see fig. 9). |
| $D_4$<br>$D_5$<br>$D_6$<br>$D_7$ | "C" Power LSB<br>"C" Power MSB | | $D_4 - D_7$ represent the average signal level of the last page of data in the range from +6dBm to −24dBm (at 1kHz) for the C input. |

## Interrupts

Three conditions can cause interrupt requests to the host microprocessor.

(i) The encode buffer contains an unread byte of data which is the most recent byte encoded.

(ii) The decode buffer is ready to receive the next consecutive byte for decoding.

(iii) The power register contains a power assessment for the most recent whole page encoded.

The status register indicates which of the above conditions are true.

If an interrupt condition remains unserviced and the condition becomes irrecoverably untrue, the status bit is cleared, the corresponding overspill bit is set and further interrupts are automatically inhibited. Also the encode and decode data buffers retain the data present when the data bit was set, i.e. register-buffer update is inhibited. The power register is updated at all times.

Condition (i) is serviced by a valid address to the encode buffer. Condition (ii) is serviced by a valid address to the decode buffer. If conditions (i) and (ii) have both become UNTRUE, servicing either buffer resets both to a cleared start position. Condition (iii) is serviced by reading the Power Register.

### The C Input

By careful selection of the audio frequency filtering to the C input the A/B and C power words can be used in the processor to provide frequency as well as power information. This facility could be used for word, pause or voice recognition.

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref. $V_{SS}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX709J | −30°C to + 85°C |
| | FX709LH | −30°C to + 70°C |
| Storage temperature range: | FX709J | −55°C to +125°C |
| | FX709LH | −40°C to + 85°C |

## Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5V, $T_{amb}$ = 25°C, Ø = $f_{in}$ = 1kHz.

| Characteristics | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Static Characteristics** | | | | | |
| Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | — | 6 | — | mA |
| Supply Current (Power Save) | | — | 1 | — | mA |
| Supply Ripple | | — | 50 | — | mV |
| Input Impedance (Audio) | | 100 | — | — | kΩ |
| Output Impedance (Audio) | | — | — | 6 | kΩ |
| Input Logic '1' | | 3.5 | — | — | V |
| Input Logic '0' | | — | — | 1.5 | V |
| Output Logic '1' | 1 | 3.5 | — | — | V |
| Output Logic '0' | 1 | — | — | 1.5 | V |
| Input Current (Logic I/P's) | | — | — | 1.0 | μA |
| Input Capacitance (Logic I/P's) | | — | — | 7.5 | pF |
| Output Logic '1' Source current | 2 | — | — | 120 | μA |
| Output Logic '0' Sink current | 3 | — | — | 360 | μA |
| Three State output leakage current | | — | — | 4 | μA |
| **Dynamic Characteristics** | | | | | |
| Audio Input Level | | — | 500 | — | mV (rms) |
| Insertion Loss, (direct) | 4, 7 | −1.5 | — | +1.5 | dB |
| Attenuation distortion *(See Fig. 6)* | | | | | |
| Clock bit Rate | 5 | 8 | — | 64 | k bits/s |
| Idle Channel Noise | 4, 6 | — | 2.5 | — | mV (rms) |
| Signal/Noise Ratio *(See Fig. 8)* | | | | | |

**Notes**

1. *Load 50pF, 200kΩ.*
2. *$V_{out}$=4.6V, not pins 14 ($\overline{IRQ}$) and 15 ($\overline{WAIT}$), these wire OR 'able pins have 100kΩ pullups .*
3. *$V_{out}$=0.4V.*
4. *Measured from Codec audio input to audio output.*
5. *2.048MHz master clock ÷ 32.*
6. *32kHz clock.*
7. *For a load of > 100kΩ, (serial switch impedance is 3kΩ/switch, see Fig. 4.*

## Typical Performance

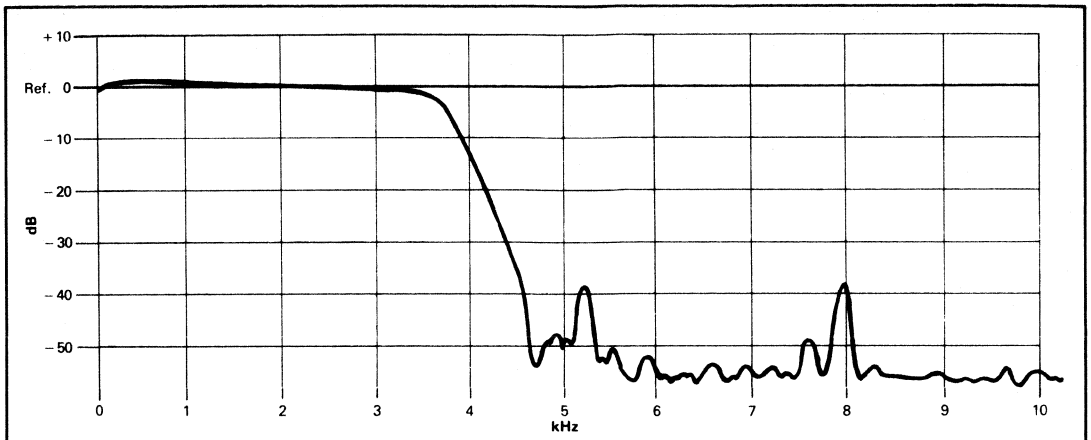
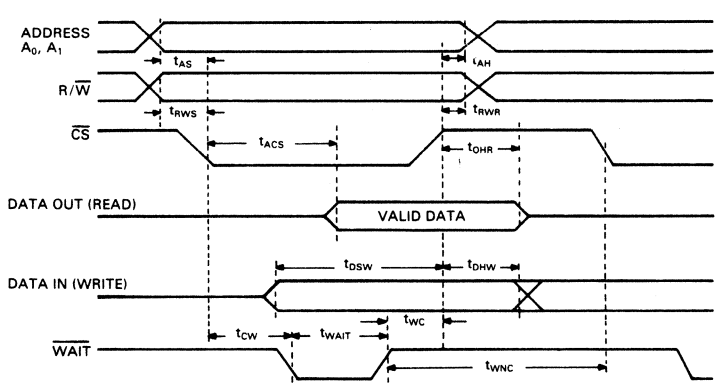



*Fig. 6 Typical FX709 System Response measured at: filter 3320 Hz, $V_{IN}$ −24 dBm, 32 kb/s*




| t= | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| $t_{AS}$ | 50 | – | – | ns |
| $t_{RWS}$ | 50 | – | – | ns |
| $t_{AH}$ | 0 | – | – | ns |
| $t_{RWR}$ | 0 | – | – | ns |
| $t_{ACS}$ | – | – | 250 | ns |
| $t_{OHR}$ | 0 | – | 100 | ns |
| $t_{DSW}$ | 150 | – | – | ns |
| $t_{DHW}$ | 150 | – | – | ns |
| $t_{CW}$ | – | – | 100 | ns |
| $t_{WAIT}$ | 2 | – | 3 | Xtal Cycle |
| $t_{WC}$ | 0 | – | – | ns |
| $t_{WNC}$ | 2 | – | – | Xtal Cycle |

**KEY**

$t_{AS}$ – Address Set Up Time
$t_{RWS}$ – Read/Write Set Up Time
$t_{AH}$ – Address Hold Time
$t_{RWR}$ – Read/Write Recovery Time
$t_{ACS}$ – Chip Select Access Time
$t_{OHR}$ – Output Hold Time (Read)
$t_{DSW}$ – Data Set Up Time (Write)
$t_{DHW}$ – Data Hold Time (Write)
$t_{CW}$ – Chip Select to WAIT Output
$t_{WAIT}$ – WAIT Time
$t_{WC}$ – WAIT High to Chip Select High
$t_{WNC}$ – End of Wait to Next Chip Select

*Fig. 7 Timing Diagram*

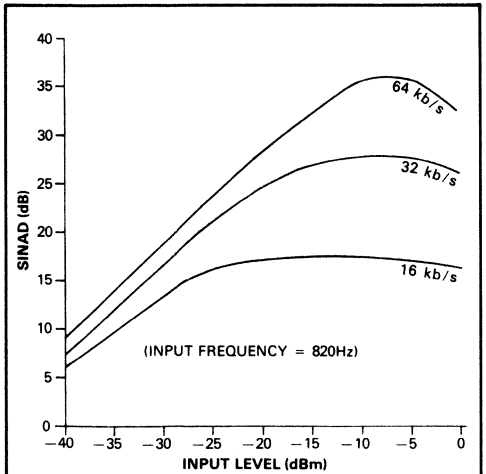



*Fig. 8 Typical FX709 Sinad versus Input Level*

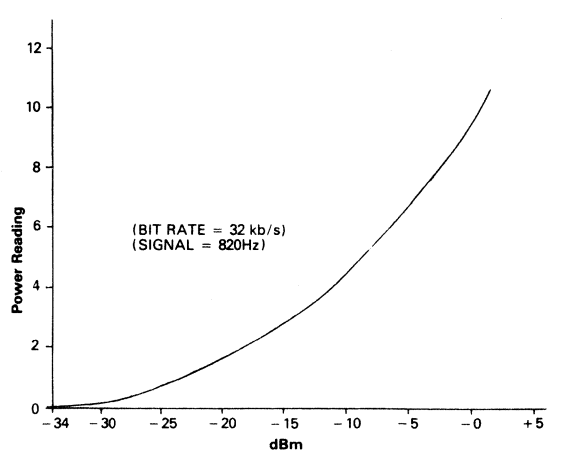


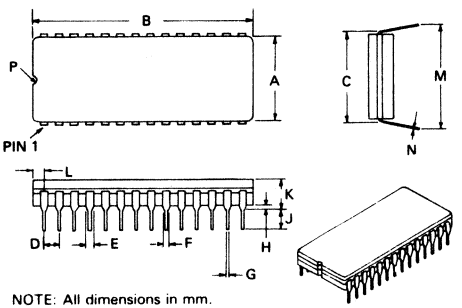

*Fig. 9 Power Reading versus Input Level*

## Package Outlines

The FX709J, the cerdip package, is illustrated in *Figure 10.* The 'LH' version is shown in *Figure 11.*

To allow complete identification, the FX709LH package has an indent spot adjacent to pin 1 and a chamfered corner between pins 4 and 5. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 10* **FX709J** *DIL Package*



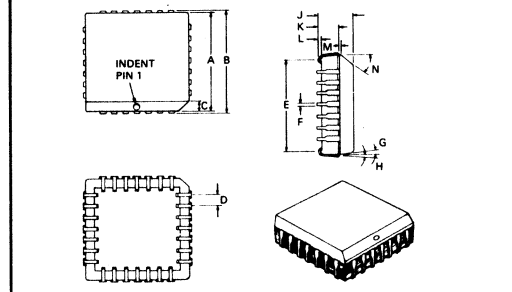

NOTE: All dimensions in mm.

| DIMENSION | MAX | MIN | DIMENSION | MAX | MIN |
|---|---|---|---|---|---|
| A | 13.36 | 13.06 | H | 1.30 | 0.50 |
| B | 37.05 | 36.58 | J | 3.81 | 3.00 |
| C | 15.7 | 15.5 | K | 5.57 | 4.49 |
| D | Typical | 2.54 | L | 2.54 | – |
| E | Typical | 1.39 | M | Typical | 17.00 |
| F | Typical | 0.81 | N | Typical | 0.25 |
| G | Typical | 0.45 | P | Typical | 0.64 |

## Handling Precautions

The FX709J/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

*Fig. 11* **FX709LH** *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 11.6 | 11.4 |
| B | 12.6 | 12.3 |
| C | 1.1 x 45° | TYPICAL |
| D | 1.3 | TYPICAL |
| E | 10.8 | 10.0 |
| F | 0.46 | TYPICAL |
| G | 7° | 3° |
| H | 7° | 3° |
| J | 4.5 | 4.3 |
| K | 2.5 | TYPICAL |
| L | 1.1 | 0.5 |
| M | 0.59 | TYPICAL |
| N | 45° | TYPICAL |

## Ordering Information

**FX709J** **28-pin cerdip DIL**
**FX709LH** **28-lead plastic leaded chip carrier.**

# Integrated Circuits Data Book

Section 10

# General Purpose

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX009A Low-Noise Digitally Controlled Amplifier Array

Publication D/009A/2 February 1993
Provisional Issue

## Features/Applications

- **8 Digitally Controlled Low-Noise Amplifiers**
- **15 Gain/Attenuation Steps**
- **7 Trimmers, with a ± 3dB Range in 0.43dB Steps**
- **1 'Volume' Trimmer, with a ± 14dB Range in 2.0dB Steps**
- **8-Bit Serial Data Control**
- **Output Mute/Powersave Function**
- **Audio and Data Gain Control Applications**
- **Cellular, PMR, PABX Applications**

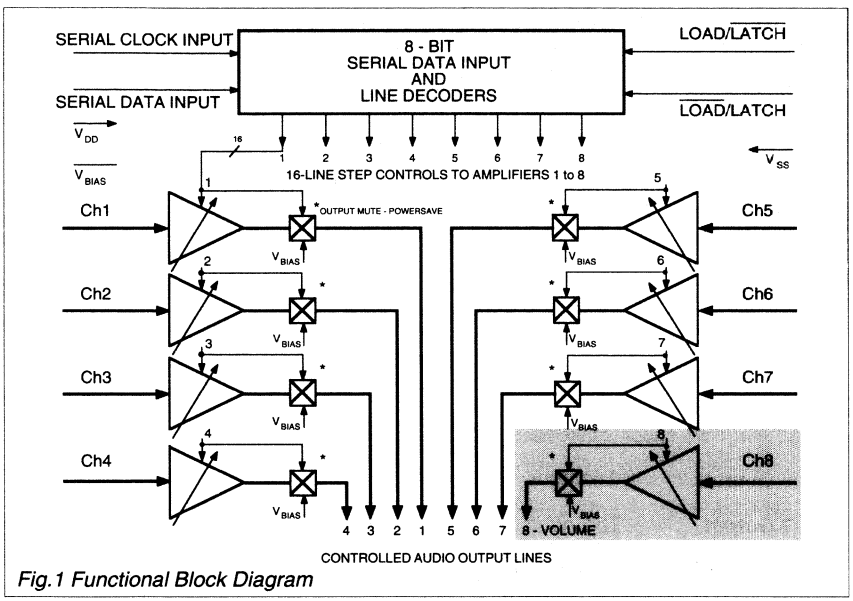



*Fig.1 Functional Block Diagram*

FX009A

## Brief Description

The FX009A Digitally Adjustable Amplifier Array is intended to replace trimmer potentiometers and volume controls in Cellular, PMR, Telephony and Communications applications where d.c., voice or data signals need adjustment.

The FX009A is a low-noise single-chip LSI consisting eight digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Seven of the amplifier stages offer a +/-3dB range in steps of 0.43dB, whilst the remaining amplifier offers a +/-14dB range in steps of 2dB, and is intended for volume control applications. Each amplifier includes a 16th 'Mute' state which sets the output to bias ($V_{DD}/2$) and powersaves the entire section. Minimum current drain may be achieved by muting all eight sections.

This product replaces the need for manual trimming of audible signals by using the host microprocessor to digitally control the set-up of all audio levels.

**Applications include:**

(i) Control, adjustment and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Level, Rx Audio Level etc.

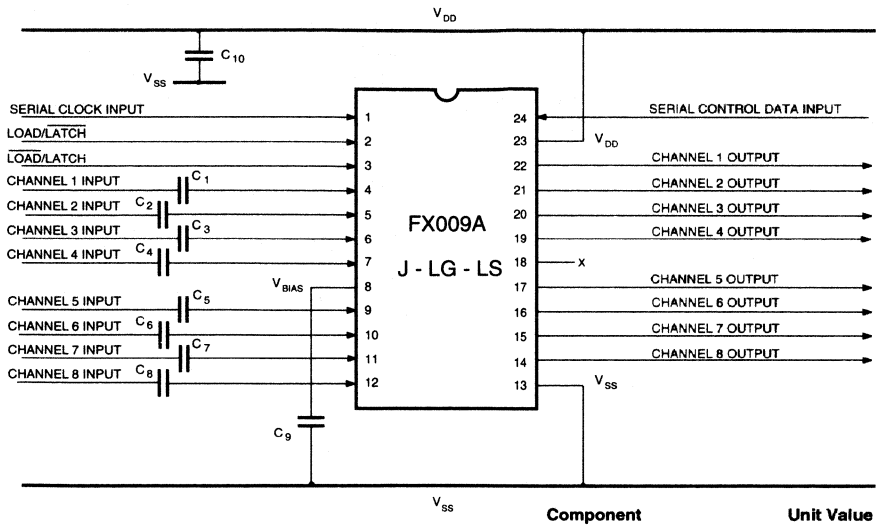
(ii) Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.

(iii) Fully automated servicing and re-alignment.

The FX009A is a low-power, single 5-volt CMOS device available in both 24-pin DIL and SMD package versions.

| Pin Number | | Function |
|---|---|---|
| FX009A J | FX009A LG/LS | |
| 1 | 1 | **Serial Clock :** This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Data Load Timing. This input has an internal 1MΩ pullup resistor. |
| 2 | 2 | **Load/Latch :** Governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0' ⇒ '1' ⇒ '0' to latch the new data in. Data is executed on the falling edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor. |
| 3 | 3 | **Load/Latch :** The inverted Load/Latch input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor. |
| 4 | 4 | **Ch1 Input :** **Analogue Inputs :** |
| 5 | 5 | **Ch2 Input :** These individual amplifier inputs are self-biasing, a.c. input analogue signals must be capacitively coupled to these pins, as shown in Figure 2. |
| 6 | 6 | **Ch3 Input :** In the powersave modes the inputs are biased at $V_{DD}/2$. |
| 7 | 7 | **Ch4 Input :** Note that amplifiers Ch1 to Ch8 are 'inverting amplifiers.' |
| 8 | 8 | **$V_{BIAS}$ :** The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ as shown in Figure 2. |
| 9 | 9 | **Ch5 Input :** **Analogue Inputs :** |
| 10 | 10 | **Ch6 Input :** |
| 11 | 11 | **Ch7 Input :** |
| 12 | 12 | **Ch8 Input :** |
| 13 | 13 | **$V_{SS}$ :** Negative supply rail (GND). |
| 14 | 14 | **Ch8 Output :** **Analogue Outputs :** |
| 15 | 15 | **Ch7 Output :** The individual "Gain Controlled" amplifier outputs. |
| 16 | 16 | **Ch6 Output :** Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps, Ch8 could be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps. |
| 17 | 17 | **Ch5 Output :** In the powersave mode the selected output is biased at $V_{DD}/2$. |
| 18 | 18 | No internal connection. Do not use. |
| 19 | 19 | **Ch4 Output :** **Analogue Outputs** |
| 20 | 20 | **Ch3 Output :** Note that amplifiers Ch1 to Ch8 are 'inverting amplifiers.' |
| 21 | 21 | **Ch2 Output :** |
| 22 | 22 | **Ch1 Output :** |
| 23 | 23 | **$V_{DD}$ :** Positive supply rail. A single +5-volt power supply is required. |
| 24 | 24 | **Control Data Input :** Operation of the 8 amplifier channels (Ch1 – Ch8) is controlled by the 8 bits of data entered serially at this pin . The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor. |

## Application Notes




**Notes**

(1) Channel Amplifiers 1 to 8 are inverting amplifiers.

(2) Analogue input capacitors $C_1$ to $C_8$ are only required for a.c. input signals, d.c. input signals do not require these components.

| Component | Unit Value |
|---|---|
| $C_1$ to $C_8$ | 0.1µ |
| $C_9$ | 1.0µ |
| $C_{10}$ | 1.0µ |

Tolerances: C = ± 20%

*Fig.2 External Component Connections*

## Application Recommendations

To avoid excess noise and instability in the final installation it is recommended that the following points be noted.

(a) A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

(b) Care should be taken on the design and layout of the printed circuit board.

(c) All external components (Figure 2) should be kept close to the FX009A package.

(d) Inputs and outputs should be screened wherever possible.

(e) Tracks should be kept short.

(f) Analogue tracks should not run parallel to digital tracks.

(g) A "Ground Plane" connected to $V_{SS}$ will assist in eliminating external pick-up on the channel input and output pins.

(h) Do not run high-level output tracks close to low-level input tracks.

(i) Input signal amplitudes should be applied with due regard to Figure 3.

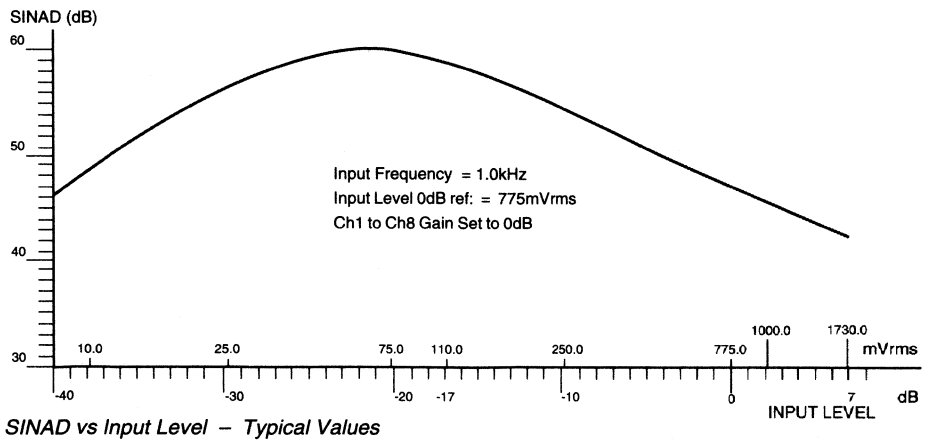



*Fig.3 SINAD vs Input Level – Typical Values*

The gain of each amplifier block (Channel 1 to Channel 8) in the FX009A is set by a separate 8-bit data word ( bit 7 to bit 0 ). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

Data is loaded to the FX009A on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/Latch (Load/Latch) pulse. Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 4 describing the data loading operation and timing.

*Table 1 Address Word Format*

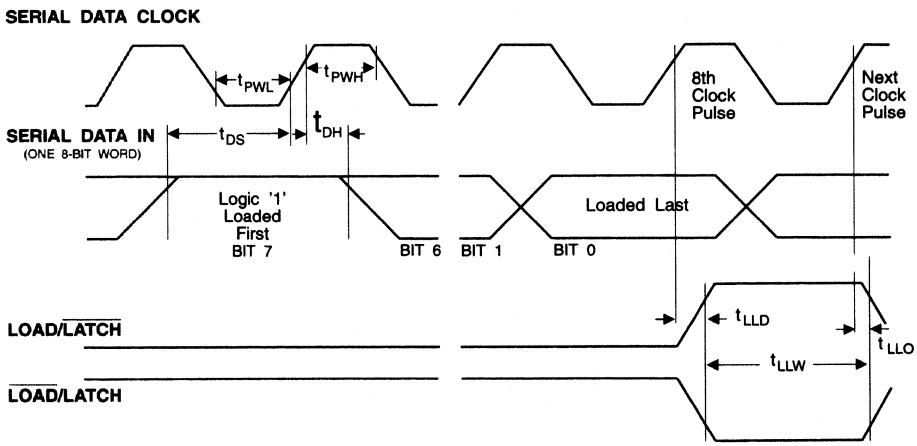
| Bit 7 MSB | Bit 6 | Bit 5 | Bit 4 LSB | Channel Selected |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 2 |
| 1 | 0 | 1 | 0 | 3 |
| 1 | 0 | 1 | 1 | 4 |
| 1 | 1 | 0 | 0 | 5 |
| 1 | 1 | 0 | 1 | 6 |
| 1 | 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 1 | 8 |

## Data Loading

The 8-bit data word is loaded *bit 7 first and bit 0* last.
Bit 7 must be a logic "1" to address the chip.
If bit 7 in the word is a logic "0" that 8-bit word will not be executed. Figure 4 (below) shows the timing information required to load and operate this device.

*Table 2 Gain Control Word Format*

| Bit 3 MSB | Bit2 | Bit 1 | Bit 0 LSB | Stage 1 to 7 (0.43dB) | Stage 8 (2.0dB) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Powersave | Powersave |
| 0 | 0 | 0 | 1 | -3.0 | -14.0 dB |
| 0 | 0 | 1 | 0 | -2.571 | -12.0 dB |
| 0 | 0 | 1 | 1 | -2.143 | -10.0 dB |
| 0 | 1 | 0 | 0 | -1.714 | -8.0 dB |
| 0 | 1 | 0 | 1 | -1.286 | -6.0 dB |
| 0 | 1 | 1 | 0 | -0.857 | -4.0 dB |
| 0 | 1 | 1 | 1 | -0.428 | -2.0 dB |
| 1 | 0 | 0 | 0 | 0 | 0 dB |
| 1 | 0 | 0 | 1 | 0.428 | 2.0 dB |
| 1 | 0 | 1 | 0 | 0.857 | 4.0 dB |
| 1 | 0 | 1 | 1 | 1.286 | 6.0 dB |
| 1 | 1 | 0 | 0 | 1.714 | 8.0 dB |
| 1 | 1 | 0 | 1 | 2.143 | 10.0 dB |
| 1 | 1 | 1 | 0 | 2.571 | 12.0 dB |
| 1 | 1 | 1 | 1 | 3.0 | 14.0 dB |




**Timing**

$t_{PWH}$
Serial Clock "High" Pulse Width

$t_{PWL}$
Serial Clock "Low" Pulse Width

$t_{DS}$
Data Set-up Time

$t_{DH}$
Data Hold Time

$t_{LLD}$
Load/Latch Delay

$t_{LLW}$
Load/Latch Pulse Width

$t_{LLO}$
Load/Latch Over Time

*Fig.4 Serial Control Data Loading Diagram*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX009A J** | -30°C to +85°C (cerdip) |
| | **FX009A LG/LS** | -30°C to +70°C (plastic) |
| Storage temperature range: | **FX009A J** | -55°C to +125°C (cerdip) |
| | **FX009A LG/LS** | -40°C to +85°C (plastic) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Audio Level 0dB ref: = 775mVrms. Amplifier Gain Set = 0dB.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage ($V_{DD}$) | | 4.5 | 5.0 | 5.5 | V |
| Supply Current – | | | | | |
| – All Stages Quiescent | | – | 0.16 | – | mA |
| – All Stages Operating | | – | 3.75 | – | mA |
| **Dynamic Values** | | | | | |
| **Control Functions** | | | | | |
| Input Logic '1' | | 3.5 | – | – | V |
| Input Logic '0' | | – | – | 1.5 | V |
| Digital Input Impedances | | 0.5 | 1.0 | – | MΩ |
| **Amplifier Stages** (General) | | | | | |
| Bandwidth (-3dB) | | 15.0 | – | – | kHz |
| Output Impedance | | – | 0.8 | 3.0 | kΩ |
| Total Harmonic Distortion | 1 | – | 0.35 | 0.5 | % |
| Output Noise Level (per stage) | 2 | – | 65.0 | - | µVrms |
| Onset of Clipping | 3 | – | 1.73 | – | Vrms |
| Gain Variation | 4 | – | – | 0.1 | dB |
| Interstage Isolation | | – | 60.0 | – | dB |
| **"Trimmer" Stages** (Ch1 – Ch7) | | | | | |
| Gain | | -3.0 | | +3.0 | dB |
| Gain per Step (15 in No.) | | – | 0.43 | – | dB |
| Step Error | 5 | – | – | ±0.2 | dB |
| Input Impedance | | 100.0 | – | – | kΩ |
| **"Volume" Stage** (Ch8) | | | | | |
| Gain | | -14.0 | | +14.0 | dB |
| Gain per Step (15 in No.) | | – | 2.0 | – | dB |
| Step Error | 5 | – | – | ±0.4 | dB |
| Input Impedance | | 50.0 | – | – | kΩ |
| **Timing** (Figure 4) | | | | | |
| Serial Clock "High" Pulse Width ($t_{PWH}$) | | 250 | – | – | ns |
| Serial Clock "Low" Pulse Width ($t_{PWL}$) | | 250 | – | – | ns |
| Data Set-up Time ($t_{DS}$) | | 150 | – | – | ns |
| Data Hold Time ($t_{DH}$) | | 50 | – | – | ns |
| Load/Latch Over Time ($t_{LLO}$) | | – | – | 50.0 | ns |
| Load/Latch Delay ($t_{LLD}$) | | 200 | – | – | ns |
| Load/Latch Pulse Width ($t_{LLW}$) | | 150 | – | – | ns |
| Serial Data Clock Frequency | | – | – | 2.0 | MHz |

**Notes**

1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 3.
4. Over temperature and supply voltage range.
5. With reference to a 1.0kHz signal.

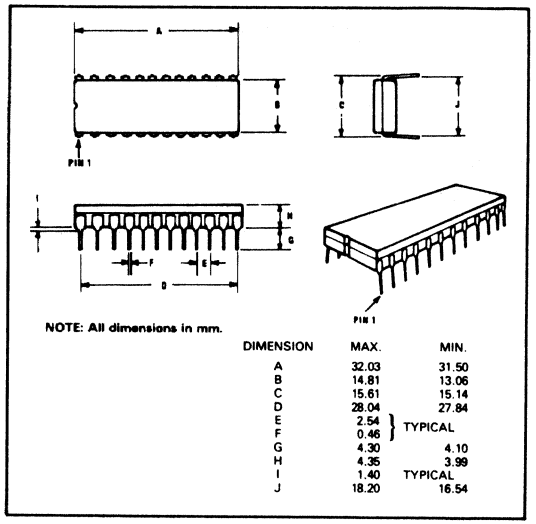
## Package Outlines

The FX009A J, the cerdip package is shown in Figure 5. The 'LG' version is shown in Figure 6, and the 'LS' version in Figure 7. To allow complete identification, the FX009A LG and LS packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4.

## Handling Precautions

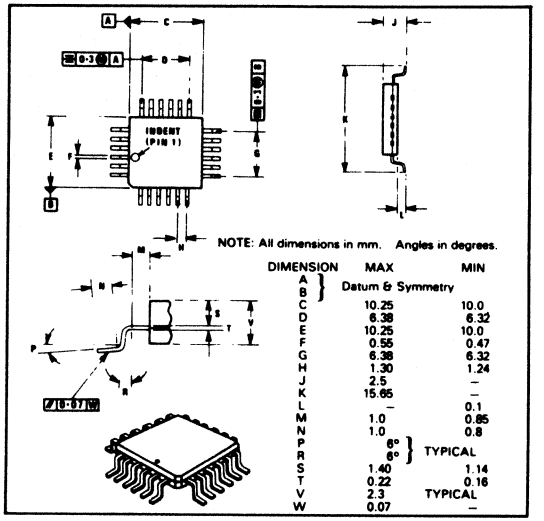
The FX009A is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

*Fig.5* ***FX009A J 24-pin DIL Package***



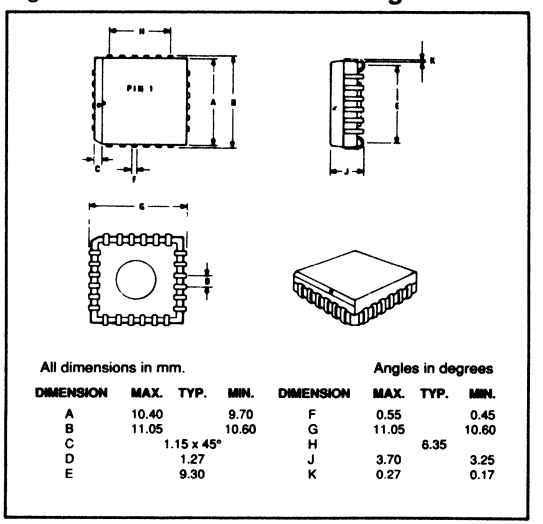

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 32.03 | 31.50 |
| B | 14.81 | 13.06 |
| C | 15.61 | 15.14 |
| D | 28.04 | 27.84 |
| E | 2.54 | TYPICAL |
| F | 0.46 | TYPICAL |
| G | 4.30 | 4.10 |
| H | 4.35 | 3.99 |
| I | 1.40 | TYPICAL |
| J | 18.20 | 16.54 |

*Fig.6* ***FX009A LG 24-pin Package***




| DIMENSION | MAX | MIN |
|---|---|---|
| A | Datum & Symmetry | |
| B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

*Fig.7* ***FX009A LS 24-lead Package***




| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.40 | | 9.70 | F | 0.55 | | 0.45 |
| B | 11.05 | | 10.60 | G | 11.05 | | 10.60 |
| C | | 1.15 x 45° | | H | | 6.35 | |
| D | | 1.27 | | J | 3.70 | | 3.25 |
| E | | 9.30 | | K | 0.27 | | 0.17 |

## Ordering Information

**FX009A J** **24-pin cerdip DIL**

**FX009A LG** **24-pin quad plastic encapsulated bent and cropped**

**FX009A LS** **24-lead plastic leaded chip carrier**

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX019 Digitally Controlled Quad Amplifier Array

Publication D/019/2 February 1993
Provisional Issue

## Features

- 4 Digitally Controlled Amplifiers
- 15 Gain/Attenuation Steps
- 3 Amplifiers, with a ± 3dB Range in 0.43dB Steps
- 1 'Volume' Amplifier, with a ± 14dB Range in 2dB Steps
- 8-Bit Serial Data Control
- Output Mute Function
- Audio and Data Gain Control Applications
- Telecoms, Radio and Industrial Applications

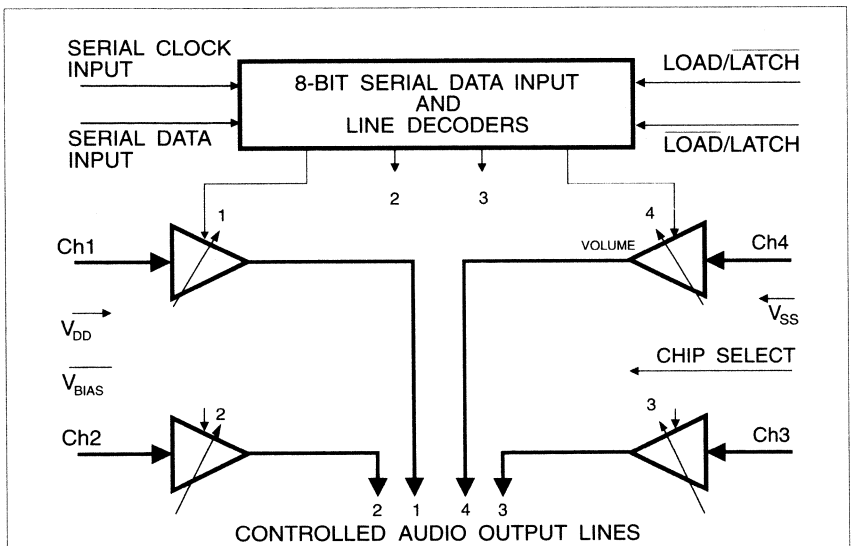



*Fig.1 Functional Block Diagram*

**FX019**

## Brief Description

The FX019 Digitally Adjustable Amplifier Array is available to replace trimmer potentiometers and volume controls in Cellular, PMR, Telephony and Communications applications where d.c., voice or data signals need adjustment.

The FX019 is a single-chip LSI consisting of four digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Three of the amplifier stages offer a +/-3dB range in steps of 0.43dB, whilst the remaining amplifier offers a +/-14dB range in steps of 2dB, and is suggested for volume control applications. Each amplifier includes a 16th 'Off' state which when applied, mutes the output audio from that channel. This array uses a Chip Select input to select one of two FX019s in a system.

This product replaces the need for manual trimming of audible signals by using the host microprocessor to digitally control the set-up of all audio levels during development, production/calibration and operation.

**Applications include:**

(i) Control, adjustment and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Levels, Rx Audio Level etc.

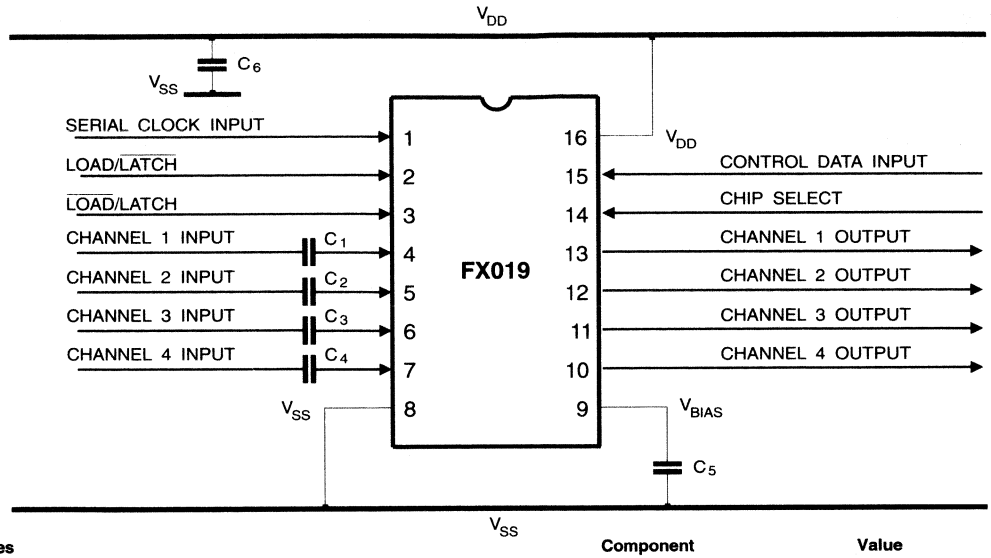
(ii) Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.

(iii) Fully automated servicing and re-alignment.

The FX019 is a low-power, single 5-volt CMOS device available in 16-pin cerdip and plastic DIL and Small Outline (S.O.I.C.) SMD package versions.

| Pin Number<br>FX019DW<br>FX019J<br>FX019P | Function |
|---|---|
| 1 | **Serial Clock :** This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Serial Control Data Load Timing. This input has an internal 1MΩ pullup resistor. |
| 2 | **Load/$\overline{\text{Latch}}$ :** Governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0' - '1' - '0' to latch the new data in. Data is executed on the falling edge of the strobe. If the $\overline{\text{Load}}$/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor. |
| 3 | **$\overline{\text{Load}}$/Latch :** The inverted Load/$\overline{\text{Latch}}$ input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor. |
| 4 | **Ch1 Input :** **Analogue Inputs :** |
| 5 | **Ch2 Input :** These individual amplifier inputs are self-biasing, a.c. input analogue signals must be capacitively coupled to these pins, as |
| 6 | **Ch3 Input :** shown in Figure 2. |
| 7 | **Ch4 Input :** Note that amplifiers Ch1 to Ch4 are 'inverting amplifiers.' |
| 8 | $V_{SS}$ : Negative supply rail (GND). |
| 9 | $V_{BIAS}$ : The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to $V_{SS}$ as shown in Figure 2. |
| 10 | **Ch4 Output :** **Controlled Analogue Outputs :** |
| 11 | **Ch3 Output :** The individual "Gain Controlled" amplifier outputs. |
| 12 | **Ch2 Output :** Ch1 to Ch3 range from -3dB to +3dB in 0.43dB steps, Ch4 could be utilized as a volume control, ranging from -14dB to +14dB in 2.0dB steps. |
| 13 | **Ch1 Output :** In the "OFF" mode there is no output from the selected amplifier. |
| 14 | **Chip Select :** A logic input to select one of two FX019 microcircuits in a system, see Table 1. This input has an internal 1MΩ pulldown resistor. |
| 15 | **Control Data Input :** Operation of the 4 amplifier channels (Ch1 – Ch4) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1MΩ pullup resistor. |
| 16 | $V_{DD}$ : Positive supply rail. A single +5-volt power supply is required. |

## Application Notes




**Notes**

(1) Channel Amplifiers 1 to 4 are inverting amplifiers.

(2) Analogue input capacitors $C_1$ to $C_4$ are only required for a.c. input signals, d.c. input signals do not require these components.

| Component | Value |
|---|---|
| $C_1$ to $C_4$ | 0.1µF |
| $C_5$ | 1.0µF |
| $C_6$ | 1.0µF |

Tolerances: C = ± 20%

*Fig.2 External Component Connections*

## Application Recommendations

To avoid excess noise and instability in the final installation it is recommended that the following points be noted.

(a) A noisy or badly regulated power supply can cause instability and/or variance of selected gains.

(b) Care should be taken on the design and layout of the printed circuit board.

(c) All external components (Figure 2) should be kept close to the FX019 package.

(d) Inputs and outputs should be screened wherever possible.

(e) Tracks should be kept short.

(f) Analogue tracks should not run parallel to digital tracks.

(g) A "Ground Plane" connected to $V_{SS}$ will assist in eliminating external pick-up on the channel input and output pins.

(h) Do not run high-level output tracks close to low-level input tracks.

(i) Input signal amplitudes should be applied with due regard to Figure 3.

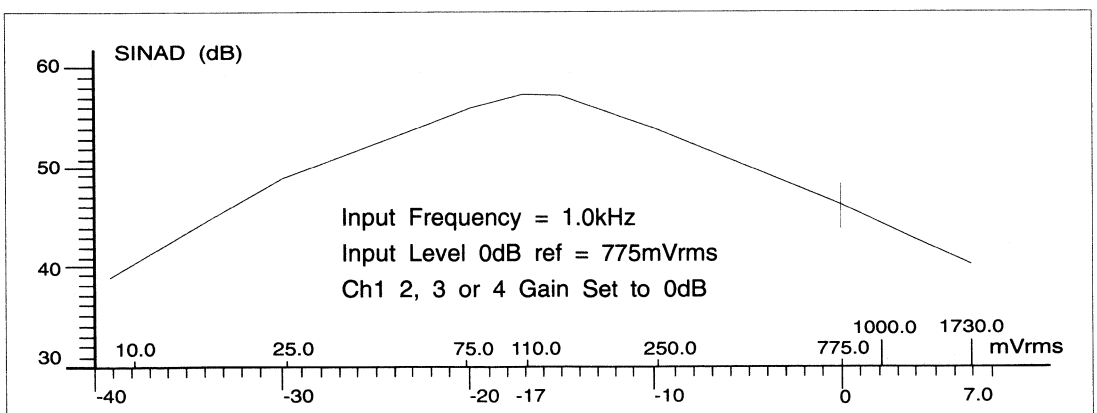



*Fig.3 SINAD vs Input Level – Typical Values*

## Control Data and Timing

The gain of each amplifier block (Channel 1 to Channel 4) in the FX019 is set by a separate 8-bit data word ( bit 7 to bit 0 ). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

Data is loaded to the FX019 on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/Latch (Load/Latch) pulse. Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 4 describing the data loading operation and timing.

*Table 1 Address Word Format*

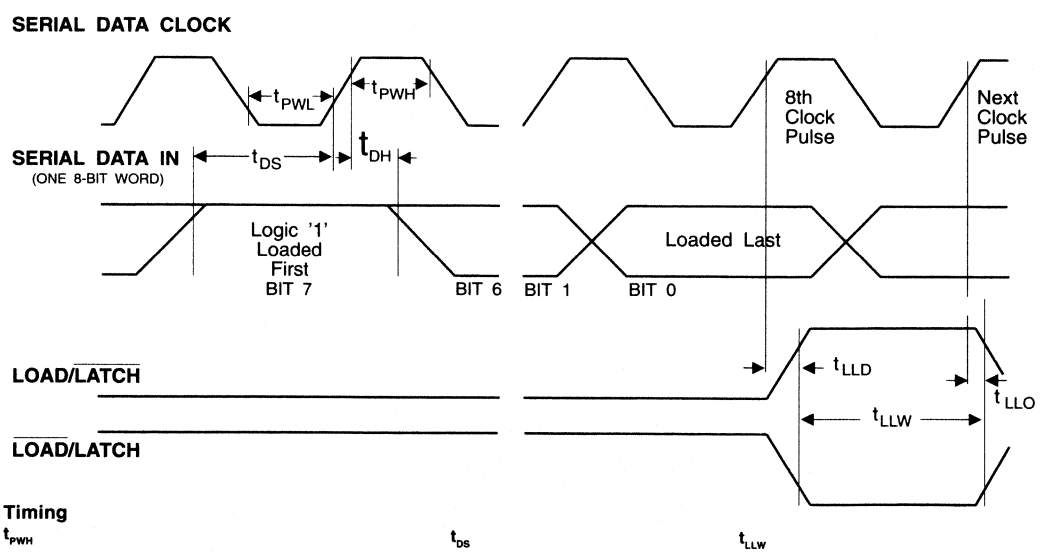
| Bit 7 MSB | Bit 6 | Bit 5 | Bit 4 LSB | Channel Selected | Chip Select | Chip Number |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | |
| 1 | 0 | 0 | 1 | 2 | 0 | Chip |
| 1 | 0 | 1 | 0 | 3 | 0 | 1 |
| 1 | 0 | 1 | 1 | 4 | 0 | |
| 1 | 1 | 0 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 1 | 2 | 1 | Chip |
| 1 | 1 | 1 | 0 | 3 | 1 | 2 |
| 1 | 1 | 1 | 1 | 4 | 1 | |

*Table 2 Gain Control Word Format*

| Bit 3 MSB | Bit2 | Bit 1 | Bit 0 LSB | Stage 1, 2, 3 (0.43dB) | Stage 4 (2.0dB) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | OFF | OFF |
| 0 | 0 | 0 | 1 | -3.0 | -14.0dB |
| 0 | 0 | 1 | 0 | -2.571 | -12.0 |
| 0 | 0 | 1 | 1 | -2.143 | -10.0 |
| 0 | 1 | 0 | 0 | -1.714 | -8.0 |
| 0 | 1 | 0 | 1 | -1.286 | -6.0 |
| 0 | 1 | 1 | 0 | -0.857 | -4.0 |
| 0 | 1 | 1 | 1 | -0.428 | -2.0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0.428 | 2.0 |
| 1 | 0 | 1 | 0 | 0.857 | 4.0 |
| 1 | 0 | 1 | 1 | 1.286 | 6.0 |
| 1 | 1 | 0 | 0 | 1.714 | 8.0 |
| 1 | 1 | 0 | 1 | 2.143 | 10.0 |
| 1 | 1 | 1 | 0 | 2.571 | 12.0 |
| 1 | 1 | 1 | 1 | 3.0 | 14.0 |

### Data Loading

The 8-bit data word is loaded *bit 7 first and bit 0* last. Bit 7 must be a logic "1" to address the chip.
If bit 7 in the word is a logic "0" that 8-bit word will not be executed. The Chip Select input permits the use of two devices in a system; To facilitate this, Bit 6 can be either a logic "0" or "1." Figure 4 (below) shows the timing information required to load and operate this device.




**Timing**

$t_{PWH}$
Serial Clock "High" Pulse Width

$t_{PWL}$
Serial Clock "Low" Pulse Width

$t_{DS}$
Data Set-up Time

$t_{DH}$
Data Hold Time

$t_{LLD}$
Load/Latch Delay

$t_{LLW}$
Load/Latch Pulse Width

$t_{LLO}$
Load/Latch Over Time

*Fig.4 Serial Control Data Loading Diagram*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | | 800mW Max. |
| Derating | | 10mW/°C |
| Operating temperature range: | **FX019DW/P** | -40°C to +85°C (plastic) |
| | **FX019J** | -40°C to +85°C (cerdip) |
| Storage temperature range: | **FX019DW/P** | -40°C to +85°C (plastic) |
| | **FX019J** | -55°C to +125°C (cerdip) |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Audio Level 0dB ref: = 775mVrms. Amplifier Gain Set = 0dB.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage ($V_{DD}$) | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | | - | 1.5 | - | mA |
| **Dynamic Values** | | | | | |
| **Control Functions** | | | | | |
| Input Logic '1' | | 3.5 | – | – | V |
| Input Logic '0' | | – | – | 1.5 | V |
| Digital Input Impedances | | 0.5 | 1.0 | – | MΩ |
| **Amplifier Stages** (General) | | | | | |
| Bandwidth (-3dB) | | 20.0 | – | – | kHz |
| Output Impedance | | – | 1.0 | - | kΩ |
| Total Harmonic Distortion | 1 | – | 0.35 | 0.5 | % |
| Output Noise Level (per stage) | 2 | – | 180.0 | 400.0 | µVrms |
| Onset of Clipping | 3 | – | 1.73 | – | Vrms |
| Gain Variation | 4 | – | – | 0.1 | dB |
| Interstage Isolation | | – | 60.0 | – | dB |
| **"Trimmer" Stages** (Ch1 – Ch3) | | | | | |
| Gain | | -3.0 | | +3.0 | dB |
| Gain per Step (15 in No.) | | – | 0.43 | – | dB |
| Step Error | 5 | – | – | ±0.2 | dB |
| Input Impedance | | 100.0 | – | – | kΩ |
| **"Volume" Stage** (Ch4) | | | | | |
| Gain | | -14.0 | | +14.0 | dB |
| Gain per Step (15 in No.) | | – | 2.0 | – | dB |
| Step Error | 5 | – | – | ±0.4 | dB |
| Input Impedance | | 50.0 | – | – | kΩ |
| **Timing** (Figure 4) | | | | | |
| Serial Clock "High" Pulse Width ($t_{PWH}$) | | 250 | – | – | ns |
| Serial Clock "Low" Pulse Width ($t_{PWL}$) | | 250 | – | – | ns |
| Data Set-up Time ($t_{DS}$) | | 150 | – | – | ns |
| Data Hold Time ($t_{DH}$) | | 50.0 | – | – | ns |
| Load/Latch Pulse Width ($t_{LLW}$) | | 150 | – | – | ns |
| Load/Latch Delay ($t_{LLD}$) | | 200 | – | – | ns |
| Load/Latch Over ($t_{LLO}$) | | – | – | 50.0 | ns |
| Serial Data Clock Frequency | | – | – | 2.0 | MHz |

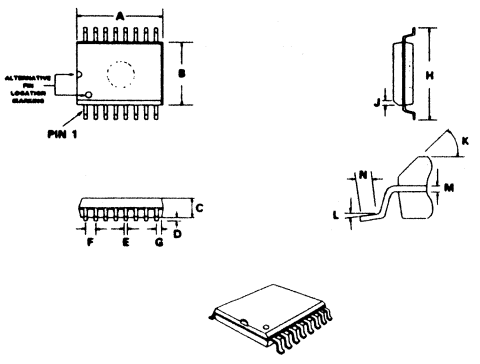
**Notes**

1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. With an a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 3.
4. Over the temperature and supply voltage range.
5. With reference to a 1.0kHz signal.

## Package Outlines

The FX019DW, the Small Outline Integrated Circuit (S.O.I.C.) package is shown in Figure 5, the 'J' cerdip version in Figure 6 and the 'P' plastic version in Figure 7. Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top (marked side).

*Fig.5* ***FX019DW 16-pin S.O.I.C. Package***




All dimensions in mm. Angles in degrees

| DIMENSION | MAX. | TYP. | MIN. | DIMENSION | MAX. | TYP. | MIN. |
|---|---|---|---|---|---|---|---|
| A | 10.31 | | 10.03 | G | | 0.66 | |
| B | 7.59 | | 7.39 | H | 10.51 | | 10.11 |
| C | 2.67 | | 2.21 | J | | 0.63 | |
| D | | 0.20 | | K | | 45° | |
| E | | 0.40 | | L | | 5° | |
| F | | 1.27 | | M | | 0.25 | |
| | | | | N | | 0.76 | |

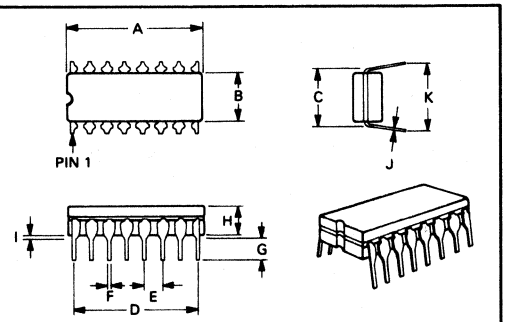
## Ordering Information

| | |
|---|---|
| **FX019DW** | **16-pin plastic S.O.I.C.** |
| **FX019J** | **16-pin cerdip DIL** |
| **FX019P** | **16-pin plastic DIL** |

## Handling Precautions

The FX019 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

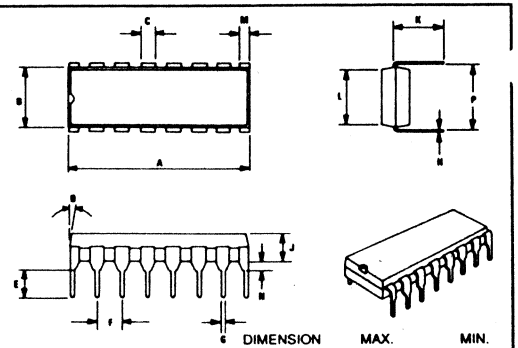
*Fig.6* ***FX019J 16-pin cerdip Package***




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 19.48 | 19.12 |
| B | 7.40 | 7.24 |
| C | 8.00 | 7.80 |
| D | 17.78 | TYPICAL |
| E | 2.54 | TYPICAL |
| F | 0.46 | TYPICAL |
| G | 4.30 | 4.10 |
| H | 4.27 | TYPICAL |
| I | 1.40 | TYPICAL |
| J | 0.25 | TYPICAL |
| K | 9.45 | 8.45 |

*Fig.7* ***FX019P 16-pin plastic Package***




| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.24 | 18.86 |
| B | 6.41 | 6.29 |
| C | 1.54 | 1.51 |
| D | 7°,30' | 6°,30' |
| E | 3.20 | 3.15 |
| F | 2.54 | TYPICAL |
| G | 0.46 | TYPICAL |
| H | 0.25 | TYPICAL |
| J | 3.33 | 3.27 |
| K | 5.77 | 5.65 |
| L | 5.90 | 5.78 |
| M | 1.00 | 0.98 |
| N | 1.78 | 0.51 |
| P | 9.40 | 8.38 |

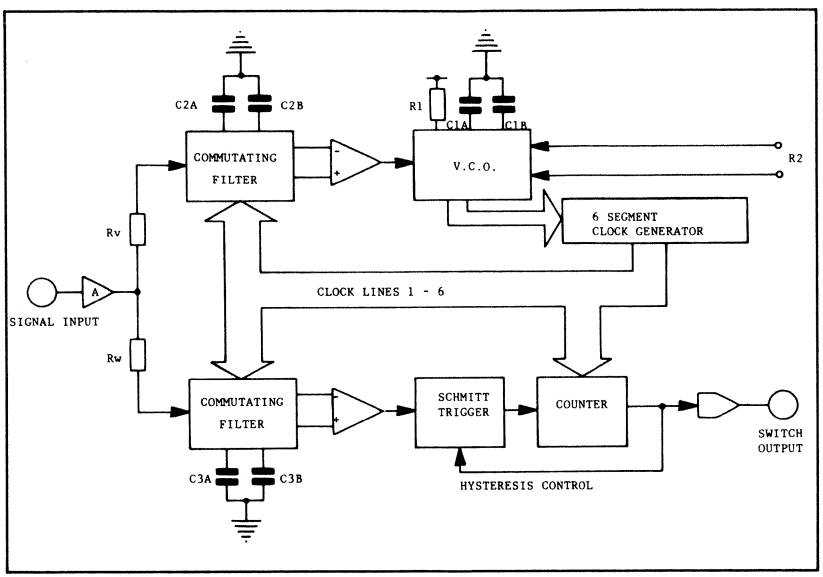
NOTE: All dimensions in mm. Angles in degrees.

# CML Semiconductor Products
**PRODUCT INFORMATION**

# FX105 Tone Detector

Publication D/105/3/12/0

## FUNCTIONAL SCHEMATIC FX-105




**FX105**
**TONE DETECTOR**

## FEATURES

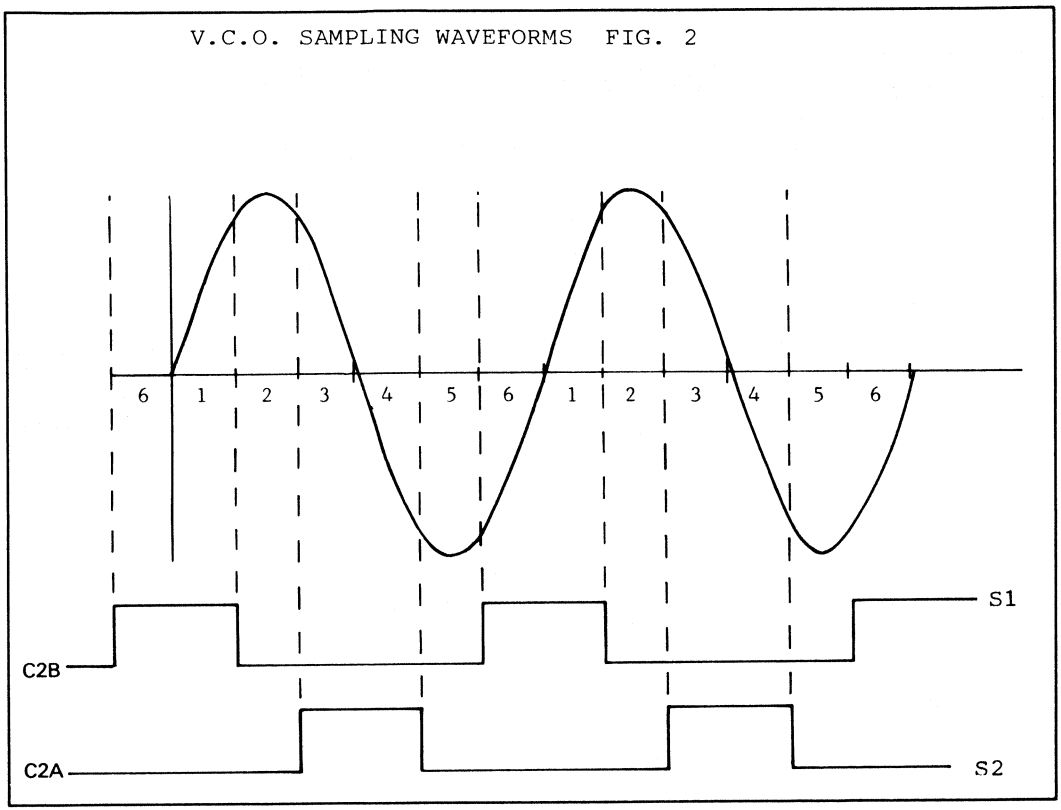
- OPERATES IN HIGH NOISE CONDITIONS
- ⩾40dB SIGNAL INPUT RANGE
- SIMULTANEOUS TONE DETECTION
- ADJUSTABLE BANDWIDTH
- HERMETICALLY SEALED CERAMIC PACKAGE
- WIDE FREQUENCY RANGE

## DESCRIPTION

The FX-105 is a monolithic tone operated switch, designed for tone decoding in single and multitone signalling systems.

The device employs decoding techniques which allow tones to be recognised in the presence of high noise levels or strong adjacent channel tones.

Tone channel centre frequency and channel bandwidth can each be adjusted independently. The circuit has a high noise immunity against harmonic and sub-harmonic responses and is able to maintain a constant bandwidth and high noise immunity over a wide range of input signal levels.




## METHOD OF OPERATION

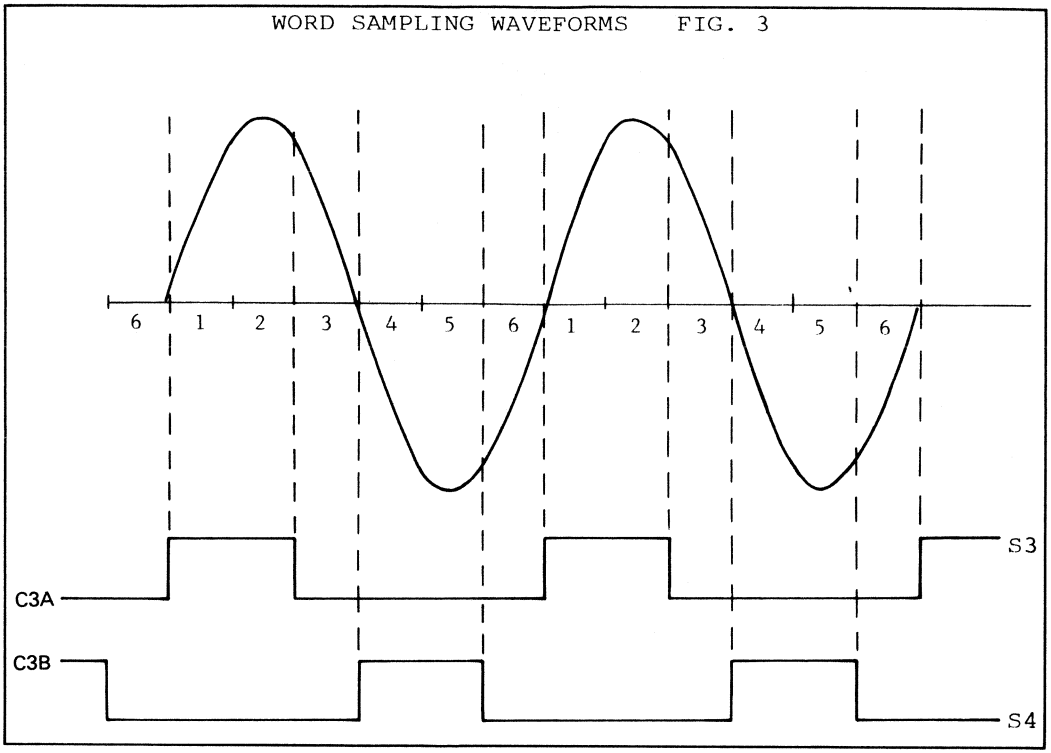
Input signals are A.C. coupled to the buffer input, which is internally biased at 50% of supply voltage, the signal appears at the output of the buffer as an A.C. voltage superimposed on the D.C. bias level. The signal is then coupled via RV and RW to the voltage controlled oscillator and word sampling switches, which sequentially connect C2 and C3 into circuit to form four sample and hold RC integrators.

With no input signal, each capacitor charges to the D.C. bias level and differential voltages are zero. When an input signal is applied, each capacitor receives an additional charge according to the integrated average of the signal waveform during the interval the capacitor is switched into circuit.

Figure 2 above shows the operating sequence of the V.C.O. sampling switches and their phase relationship to a locked on inband signal. As can be seen from Figure 2 C2A and C2B should not receive any additional charge as they always sample the input as it crosses the D.C. bias level. Should the signal not be locked to the V.C.O. then a positive or negative charge voltage will appear on C2A or C2B, this voltage when differentially amplified is applied to the V.C.O. as an error correcting signal to enable the V.C.O. to achieve lock.

Figure 3 shows the operating sequence of the 'Word' sampling switches and their relationship to a locked on inband signal. As can be seen from Figure 3 the charge being applied to C3A should always be positive and the charge applied to C3B should always be negative with respect to the common bias level.

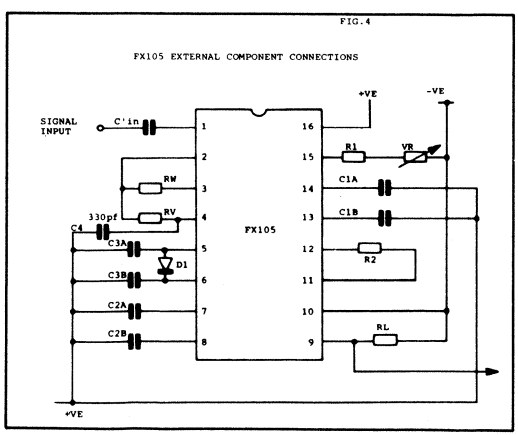
These capacitor potentials are differentially amplified and applied to a D.C. comparator, which switches at a predetermined threshold voltage. The comparator output is a logic signal used to control a counter which switches the FX-105 output ON when the comparator output is maintained in the 'Word Present' state for a minimum number of consecutive signal samples. The output switch reduces the comparator threshold by 50% when turned on, thereby introducing threshold hysterises which minimises output chatter with marginal input signal amplitudes.




## METHOD FOR CALCULATING EXTERNAL COMPONENT VALUES

The external components shown below in Figure 4 are used to adjust the various performance parameters of the FX-105. The signal to noise performance, turn on delay and signal bandwidth are all interrelated factors which should be optimised to meet the requirements of the application.

By selecting component values in accordance with the following graphs nominally optimum circuit performance is obtained for any given application.




The user should first define the following application parameters.

A. The centre frequency to be detected (f'o).

B. The FX-105 Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the FX-105 f'o due to supply voltage (0.07%/%) and ambient temperature (0.02%/°C) changes.

C. The maximum permissible FX-105 response time.

D. The minimum input signal amplitude.

Using this information the appropriate component values can be calculated, and the signal to noise performance obtained may then be read from a chart.

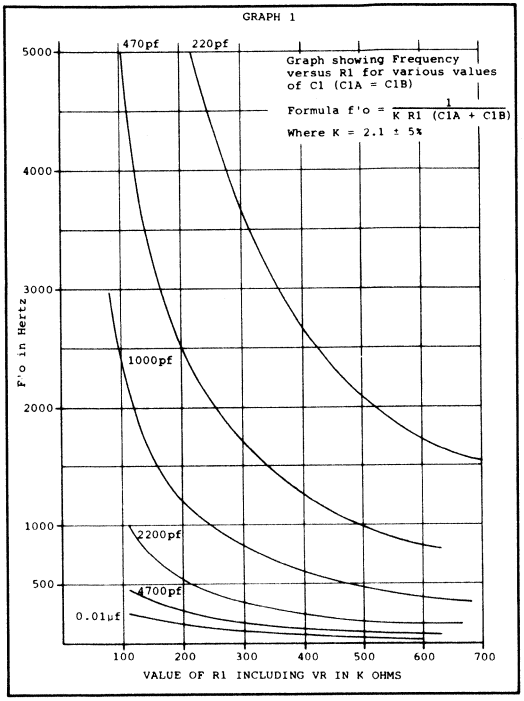
Using the graphs overleaf the following worked example may be used to calculate component values for any given application.

A. FX-105 centre band frequency (f'o) = 2800Hz.

B. FX-105 bandwidth = 6%.

C. FX-105 maximum response time = 50ms.

D. Minimum input signal amplitude = 200mVolts R.M.S.




# R1 C1A C1B

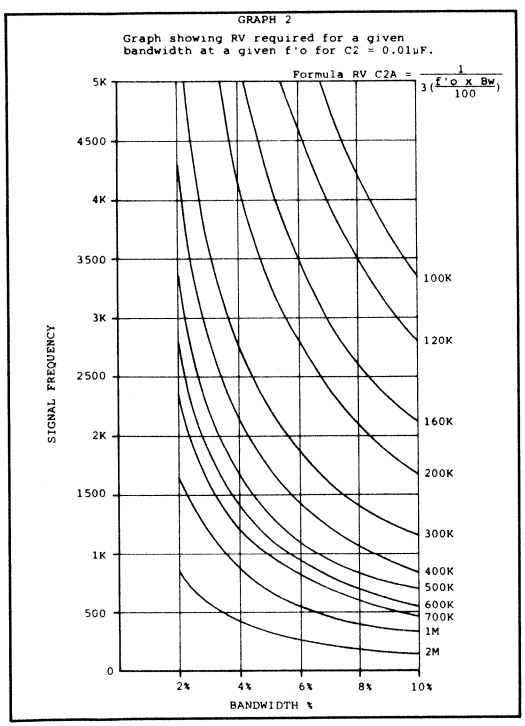
These components set the free running frequency of the V.C.O. and thereby the centre band frequency of the FX-105.

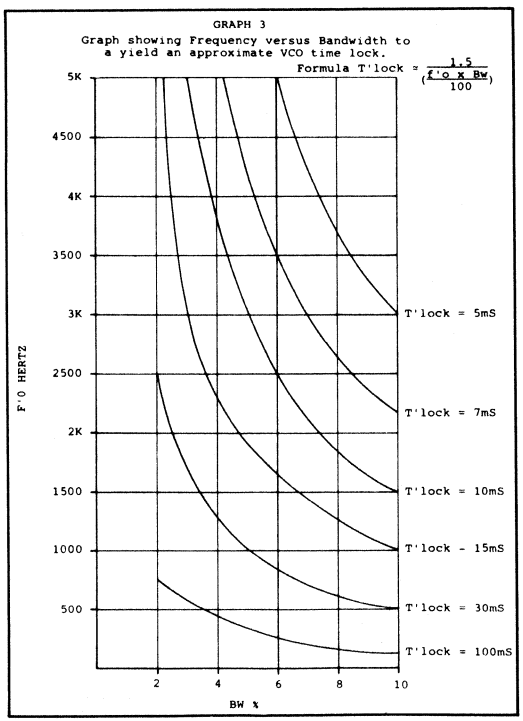
By using graph number 1 the frequency 2800Hz can be seen to correspond to a value of capacitor of 220 picofarads and a resistor value of 385k ohms, this resistance can be achieved with a 300k ohm fixed resistor for R1 and a 100k ohm potentiometer.

Graph number 2 shows that for a frequency of 2800Hz and a bandwidth of 6% a resistor RV of 200k ohms and a capacitance for C2A and C2B of 0.01 microfarads will be required.

The response time of the FX-105 is the sum of the V.C.O. 'Lock' time (T'lock) and the 'Word' integration time (T'word).

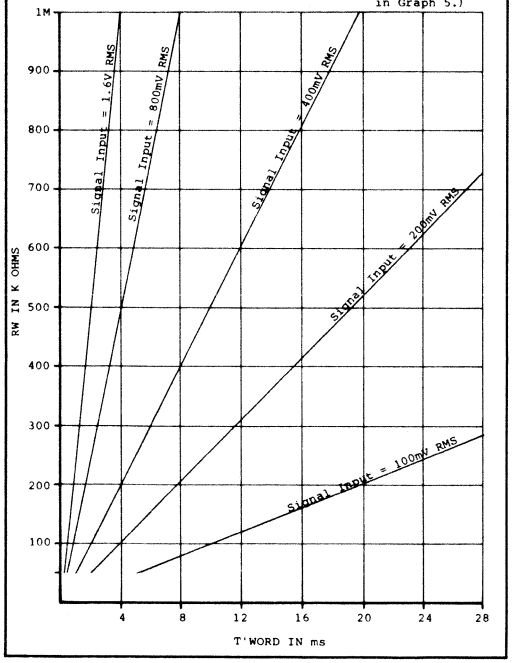
Graph number 3 shows that for a frequency of 2800Hz and a bandwidth of 6% the approximate 'Lock' time will be 9 milliseconds, as we have a maximum response time of 50 milliseconds, this allows for a 'Word' time of 41 milliseconds.



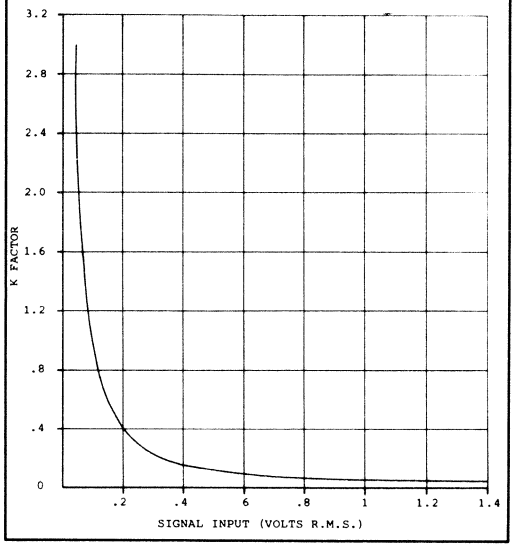
GRAPH 4

Graph showing RW required for T'word for a given signal input assuming C3A = C3B = 0.1μF. Formulae T'word = RwC3A x K(given in Graph 5.)



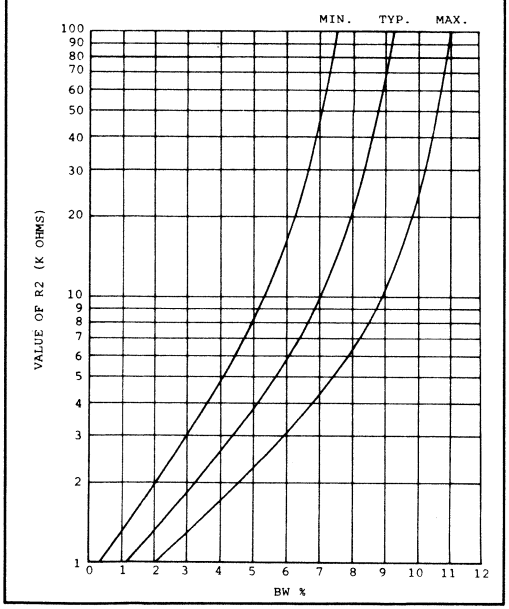

GRAPH 5

GRAPH SHOWING K FACTOR VS SIGNAL INPUT AMPLITUDE.



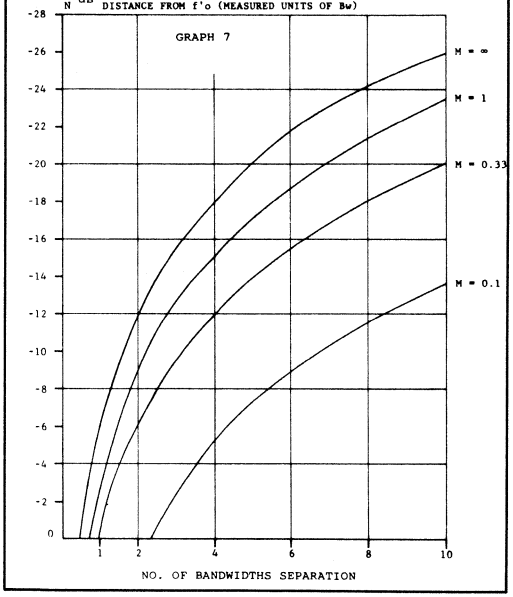

GRAPH 6

GRAPH SHOWING VALUE OF R2(KΩ) TO YIELD SELECTED BANDWIDTH(%)




GRAPH 7

S/N dB GRAPH SHOWING SIGNAL TO NOISE RATIO (dB) VS DISTANCE FROM f'o (MEASURED UNITS OF Bw)



Graph number 4 shows that for a signal amplitude of 200mVolts, a resistor value RW of 510k ohms with a 0.1 microfarad capacitor for C3A and B will yield a 'Word' time of 20ms. This will yield a response time of 9ms + 20ms = 29ms.

Graph 6 shows the range of values for R2 to yield a given bandwidth. The exact bandwidth given by any value of R2 will vary with differing production batches, therefore in applications where an exact bandwidth is required R2 should be a variable resistor which is adjusted on test.

To calculate the worst case signal to noise ratio the FX-105 will work with the above component values. The formula is as follows:

$$M = \frac{f'o \times Bw}{100} \times (Rw\ C3A)$$

$$\therefore M = \frac{2800 \times 6}{100} \times (0.51M\Omega \times 0.1\mu F)$$

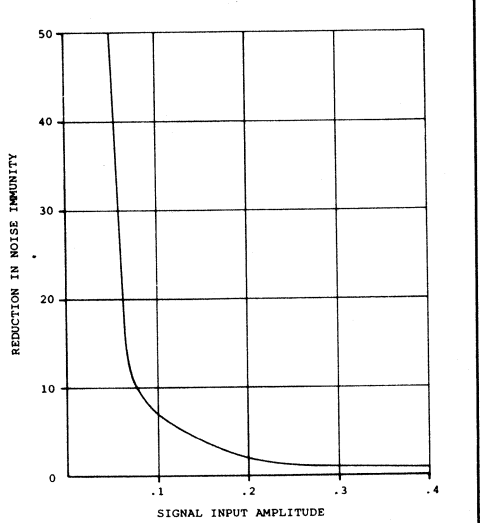
$$\therefore M = 168 \times 0.051$$

$$\therefore M \simeq 8.57$$

By substituting the value for M of 8.57 in graph number 7 the signal to noise ratio of an adjacent tone can be found, this then has to be decreased depending upon the tone amplitude. The figure to decrease SNR by is given in graph 8.

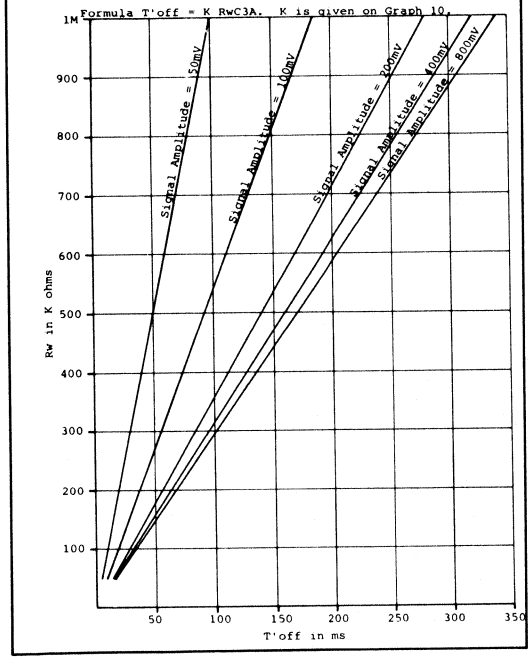
Graphs 9 and 10 show the approximate time the FX-105 will take to turn off after an inband signal has been removed. The turn off time is calculated with a diode (1N914 or similar) between pins 5 and 6 as shown in Figure 4. The effect of this diode is to greatly reduce the turn off time with signal input amplitudes greater than 300mV R.M.S.

GRAPH 8




GRAPH 9

Graph showing T'off time for a given Signal Amplitude C3 = 0.1uF and Diode D1 between C3A & C3B.




GRAPH 10

Graph showing 'K' factor for T'off vs Signal Input Amplitude (volts RMS).

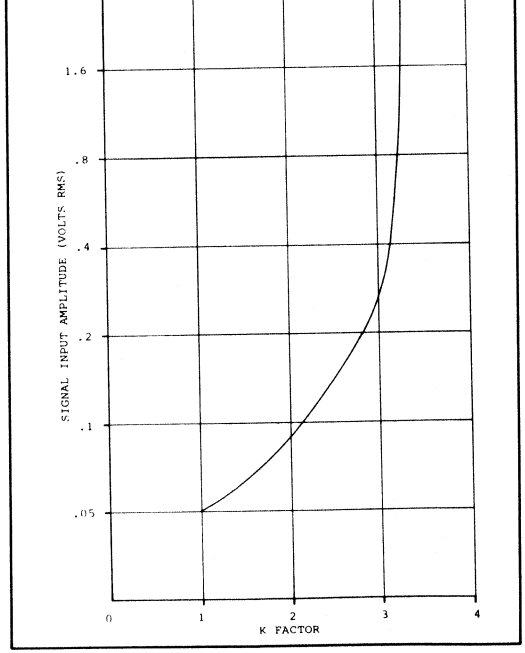
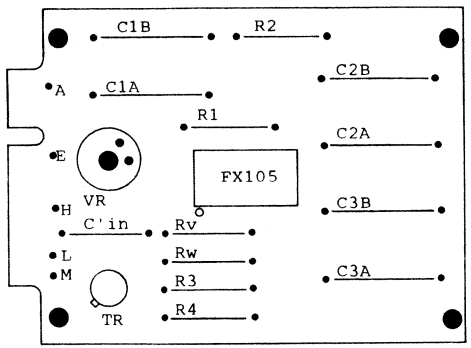


FIG.5

COMPONENT LAYOUT C-05 P.C.B.




EDGE CONNECTIONS.

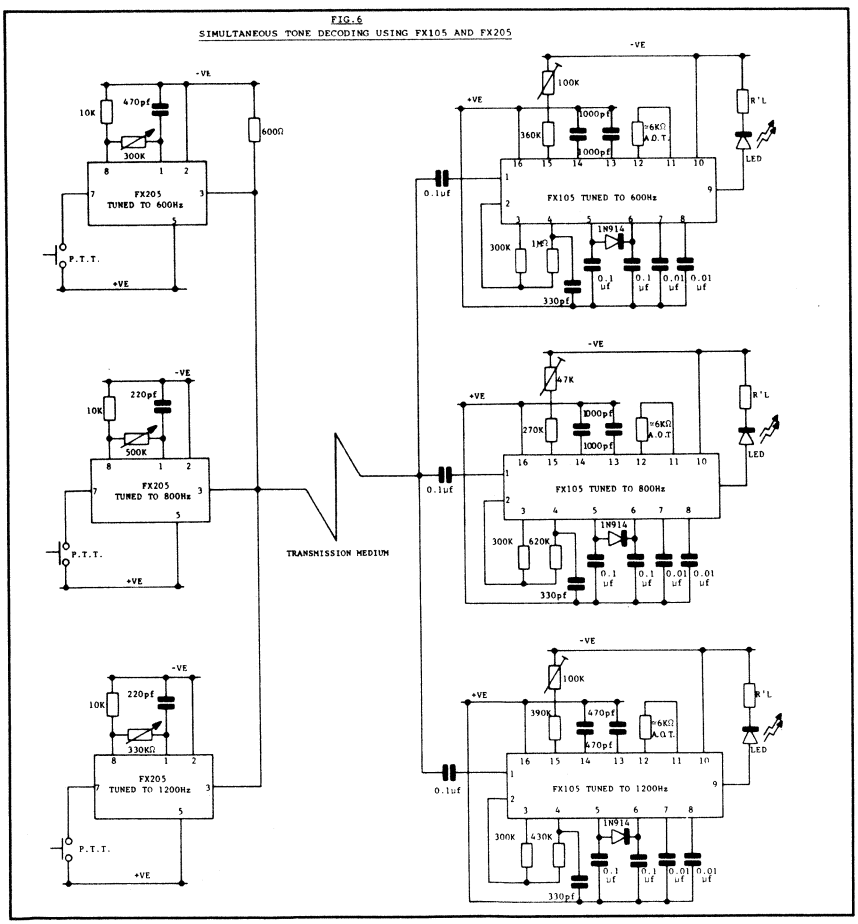
A = +ve
E = -ve
H = Signal Input
L = Switch Output
M = Buffer Output

To assist engineers in designing systems utilising the FX-105, C.M.L. have produced a printed circuit board, allowing the necessary external components to be connected, so that a full working system may be easily and quickly constructed. Please note there is no provision on the P.C.B. for capacitor C4 or diode D1 and it is recommended that these components are added for improved system operation.

Due to the FX-105's ability to decode tones in the presence of adjacent channel tones or noise, the device is ideally suited to applications where a number of tones are sequentially or simultaneously transmitted over a common link. In the example shown in Figure 6 a number of single tone transmitters (FX-205) are transmitting over a common link such as cable, radio, optical, etc., to a number of receivers (FX-105). The transmitters may transmit either individually or simultaneously to the FX-105s without the possibility of missing a call or receiving a false call.

FIG.6

SIMULTANEOUS TONE DECODING USING FX105 AND FX205



# SPECIFICATION

## MAX. RATINGS Failure to observe may result in device damage.

MAX. VOLTAGE BETWEEN ANY PIN AND +VE SUPPLY (pin 16) ..... −20V and +0.3V
OPERATING TEMPERATURE RANGE ..... −30°C to +85°C
STORAGE TEMPERATURE RANGE ..... −55°C to +125°C
DEVICE DISSIPATION (at 20°C ambient temperature) ..... 400mW
MAX. OUTPUT SWITCH LOAD CURRENT ..... 10mA

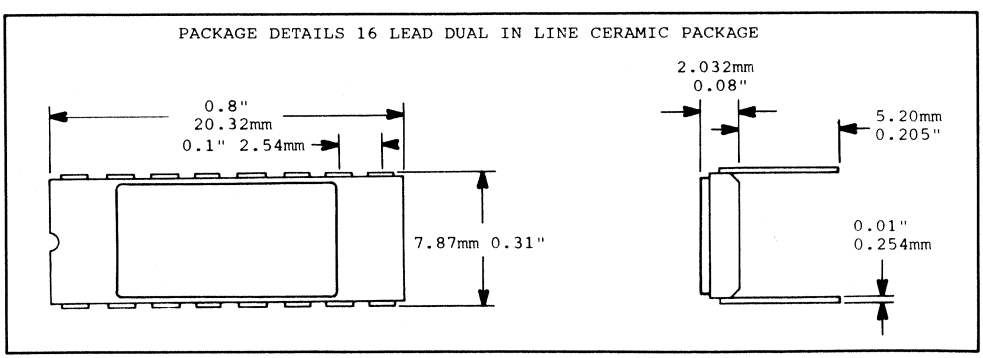
## CHARACTERISTICS

**Note:** Due to A.C. signal coupling either supply polarity may be 'ground'.

| SYMBOL | PARAMETER | NOTES | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | Operating range | 10 | 12 | 15 | Volts |
| $I_s$ | Supply current | Total, excluding loads | | 5 | | mA |
| | Signal Input | Signal + noise range | 0.055 | | 5[1] | Volts R.M.S. |
| F'o | Channel Frequency | | 0.04 | | 5 | kHz |
| Bw | Bandwidth | | 2% | | 10% | |
| | O/P switch load current | | | | 10 | mA |
| Zin | Input impedance | | | 200 | | k ohm |
| | Frequency Stability | vs T'AMB | | 0.02%/°C | | |
| | Frequency Stability | Per 1% change in supply volts | | 0.07% | | |

## NOTE

1. For input voltages greater than VDD x 0.143 pins 1 and 2 should be open circuit and the signal applied via C'in to the junction of RV and RW.



# CML Semiconductor Products

PRODUCT INFORMATION

# FX326 Audio Bandpass Filter

Publication D/326/3 March 1989
Provisional Issue

## Features/Applications

- 300Hz – 3000/3400Hz Audio Bandpass Filter
- Low Group Delay Distortion
- On-Chip Uncommitted Amplifier
- Range of Usable Xtal/Clock Frequencies
- Switched Capacitor Filters
- Chip Enable Powersave Feature
- Plastic DIL and SMD Packages
- General Purpose Audio Filtering
- Mobile and Portable Radio
- Data Signalling – Modems
- Portable Audio Equipment
- Delta and PCM Audio Filtering
- Cordless Telephones and Intercoms
- PABX and Trunk Equipment

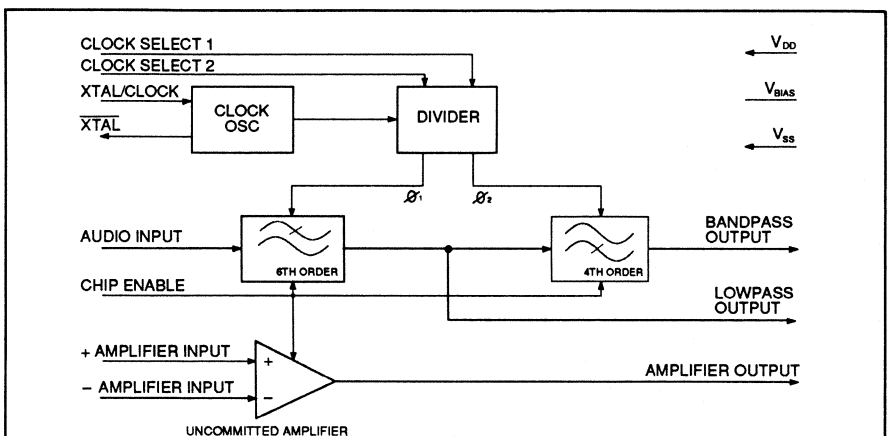



*Fig.1 Internal Block Diagram*

FX326

## Brief Description

The FX326 is a general purpose low-power CMOS switched capacitor audio bandpass filter.
The filter frequency response is clock related and with the pin programmable divider allows for standard (300Hz - 3000/3400Hz) or non-standard frequency responses.

The device in detail consists of:

(1) A 6th order low group delay distortion lowpass filter.
(2) A 4th order highpass filter.
(3) An uncommitted amplifier.
(4) On-chip clock circuitry.

The two filters are connected in series, thus providing an audio bandpass filter output, the lowpass filter output may be used independently.

An on-chip oscillator requiring a Xtal, resonator or external clock pulse input provides all reference clocks for the switched capacitor filters. The two clock select lines (S1, S2) enable the device to be used with various clock frequencies without significantly altering the filter response. Additionally the clock select inputs provide the facility to shift the filter cut-off frequencies, allowing non-standard bandpasses and lowpasses to be produced. The chip enable input, when a logic '0,' will disable the filter and amplifier sections, thus reducing current consumption. The uncommitted amplifier may be used for any specific application such as pre-emphasis, de-emphasis, buffering, gain, etc.
The FX326 Audio Bandpass Filter is available in 14-pin Plastic DIL and 24-pin SMD packages.

| Pin Number | | Function |
|---|---|---|
| Quad FX326LG | DIL FX326P | |
| 1 | 1 | $V_{DD}$ : Positive supply rail. A single +5 volt power supply is required. |
| 2 | 2 | **Select 2** (S2) : Control inputs to the clock programmable divider. The configuration of these inputs selects a division ratio (n), which with the input clock frequency ($f_C$) is used to select either the *upper* ($f_H$) or *lower* ($f_L$) filter cut-off frequency. The division ratio (n) is achieved |
| 3 | 3 | **Select 1** (S1) : using S1 and S2 as shown in the following table : |

| S1 | S2 | n |
|---|---|---|
| 0 | 0 | 10 |
| 0 | 1 | 6 |
| 1 | 0 | 20 |
| 1 | 1 | 12 |

The lower (-3dB) cut-off frequency ($f_L$) and the upper (-3dB) cut-off frequency ($f_H$) are calculated using the formulas described below.

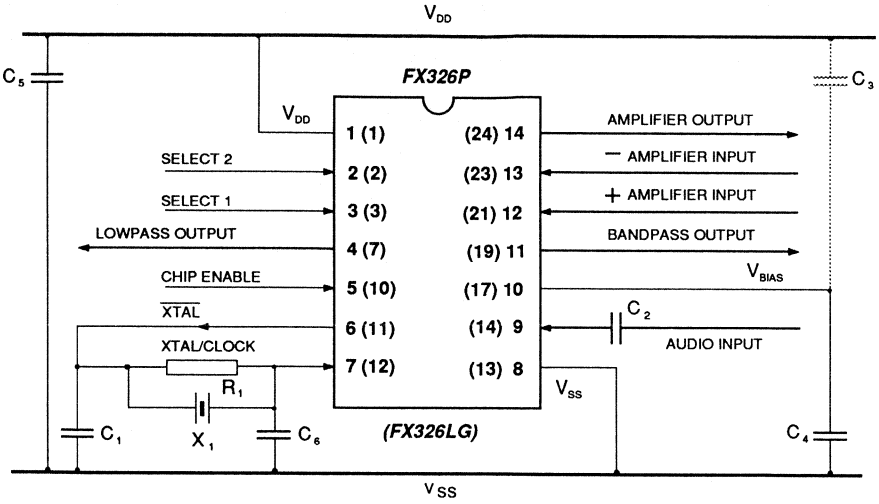
$$f_L = \frac{2.5 \times f_C}{n} \qquad f_H = \frac{34 \times f_C}{n}$$

where : $f_L$ and $f_H$ are calculated in Hz.
$f_C$ is the Clock Frequency in kHz.
n is the Division Ratio set by inputs S1 and S2.

Inputs S1 and S2 each have internal 1MΩ pulldown resistors (n = 10).

| | | |
|---|---|---|
| 7 | 4 | **Lowpass Output :** The audio output of the lowpass filter section whose upper cut-off frequency (-3dB) is determined by the input clock frequency ($f_C$) and the selection control inputs, S1 and S2, see Figure 5. This output is internally biased to $V_{BIAS}$. |
| 10 | 5 | **Chip Enable :** Internally pulled to $V_{DD}$ (logic'1') - enabling this device. A logic '0' applied to this pin will disable all filters and the uncommitted amplifier, putting the device into powersave to reduce current consumption. |
| 11 | 6 | $\overline{\text{Xtal}}$ **:** Output of the clock oscillator inverter. The clock oscillator remains powered in powersave. See Figure 2 (circuitry). |
| 12 | 7 | **Xtal/Clock :** The input to the clock oscillator inverter. A Xtal, resonator or externally derived clock pulse ($f_C$) is applied to this input. The clock frequency ($f_C$), with selection control inputs S1 and S2 will determine the upper and lower (-3dB) filter cut-off frequencies. See Figures 2, 3, 4 and 5. |
| 13 | 8 | $V_{SS}$ : Negative supply rail (GND). |
| 14 | 9 | **Audio Input :** The input to the Lowpass/Bandpass filters. This input should be a.c. coupled using capacitor $C_2$, see Figure 2. |
| 17 | 10 | $V_{BIAS}$ : The output of the on-chip analogue bias circuitry, held at $V_{DD}/2$. Remains at $V_{BIAS}$ during powersave. This pin requires to be decoupled to $V_{SS}$ by capacitor $C_4$, see Figure 2. |
| 19 | 11 | **Bandpass Output :** The audio bandpass output, whose upper and lower cut-off frequencies (-3dB) are determined by the input clock frequency ($f_C$) and the selection control inputs, S1 and S2. |
| 21 | 12 | **Amplifier Input (+ve) :** The uncommitted amplifier non-inverting input. |
| 23 | 13 | **Amplifier Input (-ve) :** The uncommitted amplifier inverting input. |
| 24 | 14 | **Amplifier Output :** The output of the uncommitted amplifier. |
| 4,5,6, 8,9,15,16, 18,20,22. | | No internal connection, do not use. |

## Application Information




| Component | Value | Note | Component | Value | Note |
|---|---|---|---|---|---|
| $R_1$ | 1MΩ | 1 | $C_4$ | 0.1µF | 2 |
| $C_1$ | 33pF | 1 | $C_5$ | 0.1µF | |
| $C_2$ | 0.1µF | | $C_6$ | 33pF | 1 |
| $C_3$ | 0.1µF | 2 | $X_1$ | Xtal/Resonator | 3 |

Tolerances : R = 10%. C = 20%.

**Notes**

1. Xtal/Clock components shown are in accordance with CML application note D/XT/1 April 1986. This input can be either a Xtal/Resonator circuit as shown, or a clock 'pulse' input.
2. $V_{BIAS}$ may be decoupled to $V_{SS}$ and $V_{DD}$. For input signals referenced to $V_{SS}$, decouple $V_{BIAS}$ to $V_{SS}$ using $C_4$ only.
3. Xtal/clock frequencies are dependant upon required filter responses – Table 1, Figures 4 and 5.

*Fig.2 Recommended External Component Connections*

Table 1 shows the upper or lower cut-off frequencies that can be achieved with differing combinations of Clock Rate ($f_C$) and Division Ratio (n) using the formulas described on Page 2 (pins 2 and 3). Typical bandpass characteristics using a 1.0MHz clock are displayed in Figure 3.

| Clock $f_C$ *(kHz)* | Division Ratio n | Lower Cut-Off *(-3dB)* $f_L$ *(Hz)* | | Upper Cut-Off *(-3dB)* $f_H$ *(Hz)* | Bandwidth *(Hz)* |
|---|---|---|---|---|---|
| 560 | 6 | 233 | – | 3173 | 2940 |
| | 10 | 140 | – | 1904 | 1764 |
| | 12 | 116 | – | 1586 | 1470 |
| | 20 | 70 | – | 952 | 882 |
| 1000 | 6 | 416 | – | 5666 | 5250 |
| | 10 | 250 | – | 3400 | 3150 |
| | 12 | 208 | – | 2833 | 2625 |
| | 20 | 125 | – | 1700 | 1575 |
| 1500 | 6 | 625 | – | 8500 | 7875 |
| | 10 | 375 | – | 5100 | 4725 |
| | 12 | 312 | – | 4250 | 3938 |
| | 20 | 187 | – | 2550 | 2363 |
| 2000 | 6 | 833 | – | 11333 | 10500 |
| | 10 | 500 | – | 6800 | 6300 |
| | 12 | 416 | – | 5666 | 5250 |
| | 20 | 250 | – | 3400 | 3150 |
| 2500 | 6 | 1041 | – | 14166 | 13125 |
| | 10 | 625 | – | 8500 | 7875 |
| | 12 | 520 | – | 7083 | 6563 |
| | 20 | 312 | – | 4250 | 3983 |

*Table 1 Examples of Upper and Lower Cut-Off Frequencies*

## Application Information

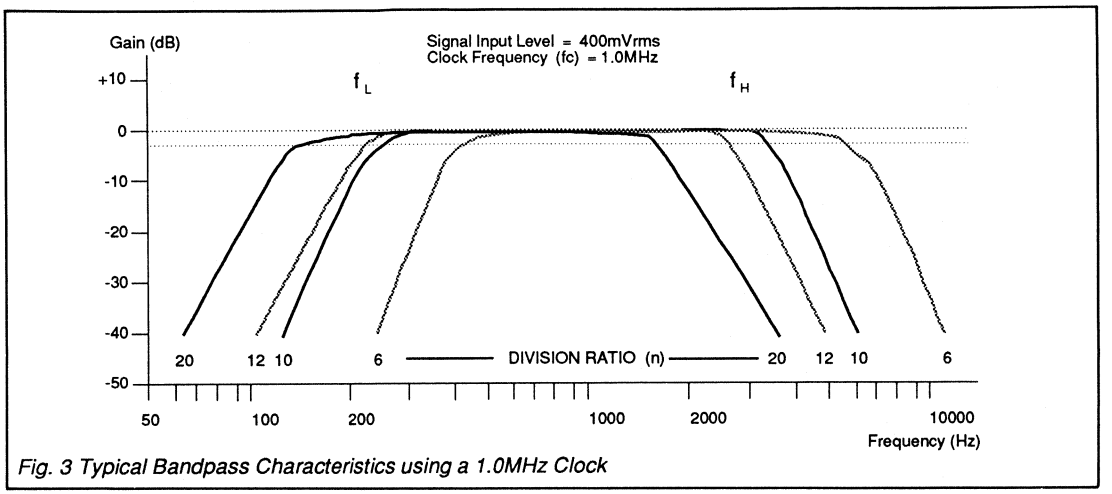



*Fig. 3 Typical Bandpass Characteristics using a 1.0MHz Clock*

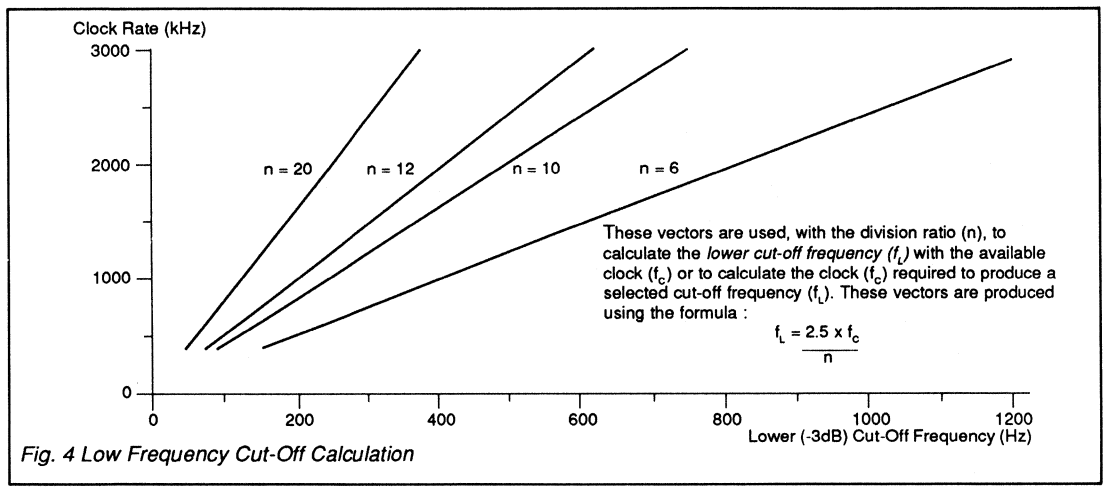



*Fig. 4 Low Frequency Cut-Off Calculation*

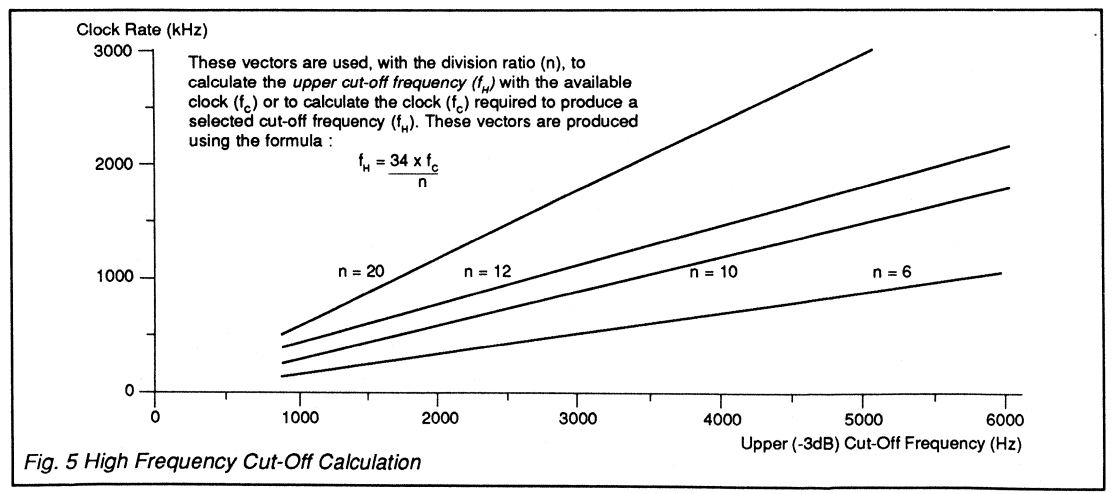



*Fig. 5 High Frequency Cut-Off Calculation*

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | |
|---|---|
| Supply voltage | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | +/- 30mA |
| (other pins) | +/- 20mA |
| Total device dissipation @ $T_{AMB}$ 25°C | 800mW Max. |
| Derating | 10mW/°C |
| Operating temperature range: **FX326LG/P** | -30°C to +70°C |
| Storage temperature range: **FX326LG/P** | -40°C to +85°C |

## Operating Limits

All device characteristics are measured using the following parameters unless otherwise specified :

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Xtal/Clock $f_c$ = 1.0 MHz. n = 10 *(S1 & S2 logic '0')*. Audio level 0dB ref: = 400mV rms.

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Static Values** | | | | | |
| Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply Current (Enabled) | | – | 3.5 | – | mA |
| Supply Current (Powersave) | | – | 1.0 | – | mA |
| Input Logic '1' | | 3.5 | – | – | V |
| Input Logic '0' | | – | – | 1.5 | V |
| **Input Impedance** | | | | | |
| Filters and Amplifier | | 100 | – | – | kΩ |
| Logic | | – | 1.0 | – | MΩ |
| **Output Impedance** | | | | | |
| Filters | | – | 3.0 | – | kΩ |
| Amplifier – Open Loop | | – | 800 | – | Ω |
| Amplifier – Closed Loop | | – | 6.0 | – | Ω |
| **Clock Oscillator Inverter** | | | | | |
| $R_{in}$ | | – | 10.0 | – | MΩ |
| $R_{out}$ | | – | 10.0 | – | kΩ |
| Gain | | – | 15.0 | – | dB |
| Gain Bandwidth Product | | – | 5.0 | – | MHz |
| Clock Frequency ($f_c$) Limits | 1 | 0.5 | – | 3.0 | MHz |
| **Dynamic Values** | | | | | |
| Signal Input Range | 2 | – | 0 | 8.0 | dB |
| Output Noise Level | 3 | – | -48.0 | – | dB |
| Insertion Loss | 4 | – | 0 | – | dB |
| Group Delay Distortion (300Hz – 3400Hz) | 6 | – | – | 200 | µs |
| **Cut-off Frequency -3dB** | | | | | |
| Lowpass - ($f_H$) | | – | 3400 | – | Hz |
| Highpass - ($f_L$) | | – | 250 | – | Hz |
| **Stopband Attenuation** | | | | | |
| f > 6kHz | | – | 47.0 | – | dB |
| f < 200Hz | | – | 27.0 | – | dB |
| Aliasing Frequency | | – | $f_c$/2n | – | Hz |
| **Uncommited Amplifier** | | | | | |
| Open Loop Gain | 5 | – | 30.0 | – | dB |
| Gain Bandwidth Product | | – | 1.0 | – | MHz |

**Notes**

1. These frequency limits are those at which the High or Low cut-off frequencies are in accordance with the formulas described in Figures 4 and 5.
2. Upper figure gives 3% distortion in 30dB SINAD. Typical figure gives minimum distortion in maximum SINAD.
3. Measured at the Bandpass Output with the Audio Input a.c. short circuit.
4. Input frequency 1.0kHz.
5. Relative to 1.0kHz at 100mV rms input.
6. Reference frequency 800Hz. See Figure 7.

## Application Information...

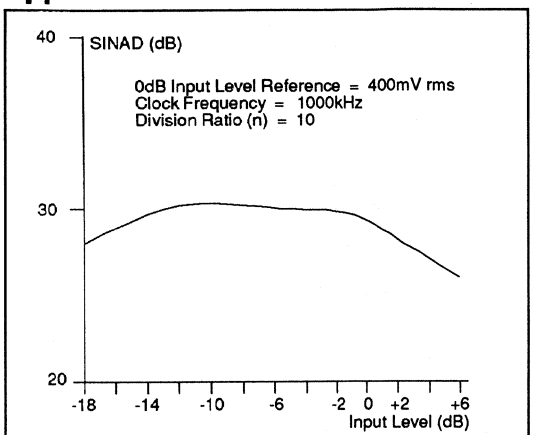



*Fig.6 Input Level Vs SINAD*

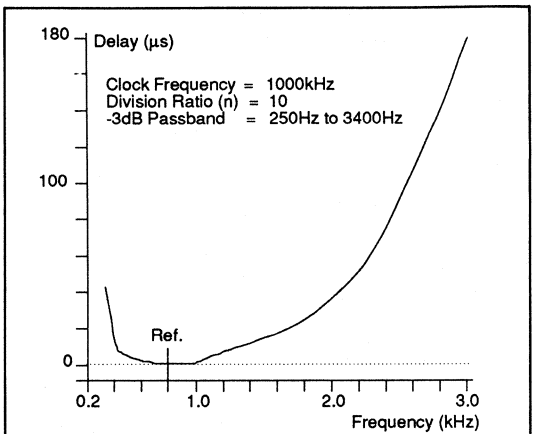
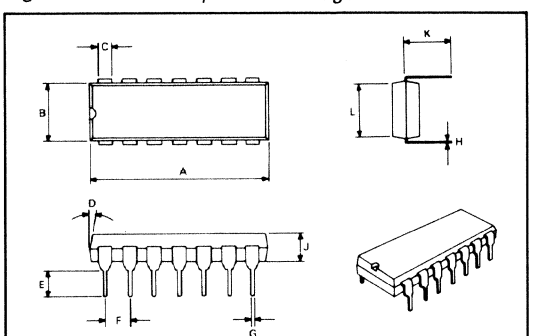



*Fig.7 Typical Group Delay Distortion*

## Package Outlines

The FX326P, the plastic package is shown in Figure 8 and the 'LG' version in Figure 9. To allow complete identification the 'LG' package has an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 8* **FX326P** *14-pin DIL Package*



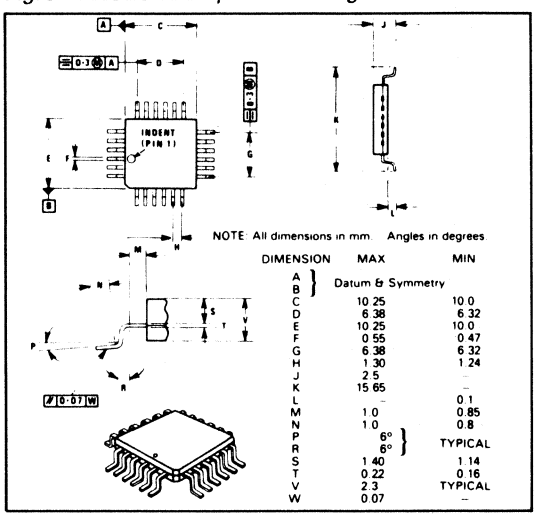

| DIMENSION | MAX. | MIN. |
|---|---|---|
| A | 19.24 | 18.86 |
| B | 6.41 | 6.29 |
| C | 1.54 | 1.51 |
| D | 7°30' | 6°30' |
| E | 3.20 | 3.15 |
| F | 2.54 | TYPICAL |
| G | 0.46 | |
| H | 0.25 | |
| J | 3.33 | 3.27 |
| K | 5.77 | 5.65 |
| L | 5.90 | 5.78 |

NOTE: All dimensions in mm. Angles in degrees.

## Handling Precautions

The FX326 is a CMOS LSI circuit whicl includes input protection.
However precautions should be taken to prevent static discharges which may cause damage.

*Fig. 9* **FX326LG** *24-pin DIL Package*




NOTE: All dimensions in mm. Angles in degrees

| DIMENSION | MAX | MIN |
|---|---|---|
| A | Datum & Symmetry | |
| B | | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | – |
| K | 15.65 | – |
| L | – | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | – |

## Ordering Information

| | |
|---|---|
| **FX326P** | **14-pin plastic DIL** |
| **FX326LG** | **24-pin quad plastic encapsulated bent and cropped** |

# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX406 Unifil™ Universal Analogue Signal Processor

**Publication D/406/6 November 1986**

**Provisional Issue**

## Features/Applications

- 2nd Order Multiple Filter
- PLL Clock Generator
- Programmable Q
- $F_c$ set by RC or External Clock
- Gain Adjustment on Inputs
- Single 5 Volt Supply CMOS
- Programmable Filters
- Voltage Controlled Filters
- Sinewave Oscillator
- Tracking Filters/Oscillators
- FSK and PSK Modems
- Square-Sine, Pulse-Sine Converter

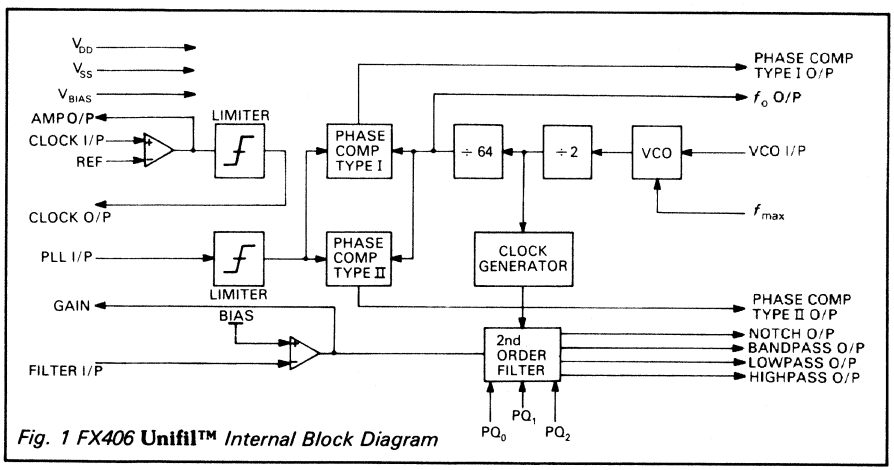



*Fig. 1 FX406* **Unifil™** *Internal Block Diagram*

**FX406**

## Brief Description

The FX406 **Unifil™** is a CMOS LSI circuit with a wide variety of signal processing applications. The device consists of a switched capacitor second order active filter with a single input and outputs for bandpass, notch, lowpass and highpass frequency responses, together with a clock generator to provide the switched capacitor sampling clock frequency. The centre frequency of the bandpass and notch filters is the same as the cut-off frequency $f_c$ of the lowpass and highpass filters. The filter sampling clock is derived from a multiplying phase locked loop whose reference or input frequency is the same as the desired cut-off frequency of the filters. The PLL comprises a voltage controlled oscillator, one of two types of phase comparator, a fixed divider and an external RC loop filter. Facilities are provided to programme the cut-off frequency of the filters by injecting an external signal into the PLL, or by using the on-chip clock oscillator circuit. The filters have gain adjustment on the input and the Q is programmable to eight values between 0.54 and 8.0.

| Pin Number | | | Function |
|---|---|---|---|
| FX406J | FX406LG | FX406LH | |
| 1 | 1 | 3 | **PCI O/P:** Output of 'EXCLUSIVE-OR' type phase comparator. See Note on PLL operation. |
| 2 | 2 | 4 | **PLL I/P:** Input to limiter preceding phase comparators. |
| 3 | 4 | 5 | $f_o$ **O/P:** Divided down VCO square wave output. |
| 4 | 5 | 6 | $PQ_0$ } **I/P:** These pins set the Q of the filters; they have internal resistors to |
| 5 | 6 | 7 | $PQ_1$ } set Q = 0.71 if left open circuit (logic state 101, ≈ 1MΩ). |
| 6 | 7 | 8 | $PQ_2$ } Possible Q values are: |
| | | | $PQ_2$ $PQ_1$ $PQ_0$ Q<br>1 1 1 0.54*<br>1 1 0 0.58 (Bessel)<br>1 0 1 0.71 (Butterworth)<br>1 0 0 1.00<br>0 1 1 1.31<br>0 1 0 2.00<br>0 0 1 4.00<br>0 0 0 8.00<br>*(Cascaded with a 1.31 section for a 4th order Butterworth filter). |
| 7 | 8 | 9 | **Clock O/P:** Digital output of limiter from uncommitted amplifier. |
| 8 | 10 | 10 | **Amp O/P:** Analogue output of uncommitted amplifier. |
| 9 | 11 | 13 | **Reference:** Inverting input to uncommitted amplifier. |
| 10 | 12 | 14 | **Clock I/P:** Non-inverting input to uncommitted amplifier. |
| 11 | 13 | 15 | **VSS:** Negative supply. |
| 12 | 14 | 16 | $V_{BIAS}$: $V_{DD}/2$ bias pin, externally decoupled. |
| 13 | 15 | 17 | **Filter I/P:** Input to filter input buffer amplifier. |
| 14 | 16 | 19 | **Gain:** Output of filter input buffer amplifier. |
| 15 | 17 | 21 | **Highpass O/P:** Output of the highpass filter. The cut-off frequency is identical to the input frequency to the PLL when locked. |
| 16 | 18 | 22 | **Lowpass O/P:** Output of the lowpass filter. The cutoff frequency is the same as the highpass filter. |
| 17 | 19 | 23 | **Bandpass O/P:** Output of the bandpass filter. $f_o$ is indentical to the input frequency to the PLL when locked. Gain in passband is dependent on Q. |
| 18 | 20 | 24 | **Notch O/P:** Output of the notch filter, $f_o$, is the same as the bandpass filter. |
| 19 | 21 | 26 | **VCO I/P:** Input of the VCO control voltage, usually connected to loop filter output. |
| 20 | 22 | 28 | $f_{max}$: This pin is connected to $V_{SS}$ via an external resistor $R_{max}$ ($R_{17}$, see Fig. 7). The value sets the maximum frequency of operation of the VCO, See Fig. 9(a) and (b). |
| 21 | 23 | 1 | **PCII O/P:** Output of the edge-triggered type of phase comparator. See Note on PLL operation. |
| 22 | 24 | 2 | $V_{DD}$: Positive supply. |
| — | 3, 9 | 11, 12, 18, 20, 25, 27 | **No Connection:** Leave open circuit. |

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | −0.3V to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = OV) | | −0.3V to ($V_{DD}$ + 0.3V) |
| Output sink/source current (total) | | 20mA |
| Operating temperature range: | FX406J | −30°C to + 85°C |
| | FX406LG/LH | −30°C to + 70°C |
| Storage temperature range: | FX406J | −55°C to +125°C |
| | FX406LG/LH | −40°C to + 85°C |
| Maximum device dissipation: | | All versions 100mW |

## Operating Limits

Typical characteristics measured using the following parameters unless otherwise specified:
$V_{DD}$ = 5V, $T_{amb}$ = 25°C, PLL input = 1kHz, filter Q = 0.707.
Limits specified over the full operating temperature and working voltage range.

| Characteristics | See Note | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Static Characteristics** | | | | | |
| Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| Supply current | | — | 4.5 | 8.5 | mA |
| Input impedance (Filter & Clock Osc) | | 1.0 | — | — | MΩ |
| Output impedance (Filter Outputs) | | — | — | 1.0 | kΩ |
| Output impedance (Clock Output) | | — | — | 1.0 | kΩ |
| Input impedance ($PQ_0$, $PQ_1$, $PQ_2$) | | 250 | — | — | kΩ |
| Output impedance ($f_o$ output) | | — | — | 5.0 | kΩ |
| Input logic '1' | | 70% $V_{DD}$ | — | — | V |
| Input logic '0' | | — | — | 30% $V_{DD}$ | V |
| **Filter Characteristics** | | | | | |
| Maximum cutoff frequency | | 4.0 | 5.0 | — | kHz |
| Minimum cutoff frequency | | — | 50 | 100 | Hz |
| Gain at $f_c$ ($f_o$) (HP BP LP) | | — | 20 log Q | — | dB |
| Notch filter depth | 1 | — | −30 | — | dB |
| Notch accuracy | 1 | — | ±0.5% $f_o$ | — | Hz |
| Maximum signal handling | 2 | 3.0 | — | — | Vp-p |
| No signal filter noise (BP) | | — | 6.0 | — | mVrms |
| (LP HP N) | | — | 3.0 | — | mVrms |
| **VCO Characteristics** | | | | | |
| VCO maximum frequency | 3 | 4.0 | 5.0 | — | kHz |
| VCO minimum frequency | 3 | — | 50 | 100 | Hz |
| VCO input impedance | | 1.0 | — | — | MΩ |
| **Phase Comparator Characteristics** | | | | | |
| Input impedance | | 100 | 500 | — | kΩ |
| Input sensitivity | 4 | 30 | 10 | — | mVrms |
| Output impedance PCII | 5 | — | — | 1.5 | kΩ |
| PCI | | — | — | 1.5 | kΩ |
| **Amplifier Characteristics** (Clock Oscillator and Filter inputs) | | | | | |
| Open loop gain | | 40 | — | — | dB |
| Input offset voltage | | — | — | 10 | mV |
| Maximum signal handling | 2 | 3.0 | — | — | Vp-p |

**Notes:** *1. Q = 8.*
*2. For SINAD = 30dB at output.*
*3. VCO frequency divided down at $f_o$ output.*
*4. At PLL input pin, ac coupled.*
*5. Output impedance when conducting, output is high impedance three-state when PLL is in lock.*

## Typical Filter Frequency Responses

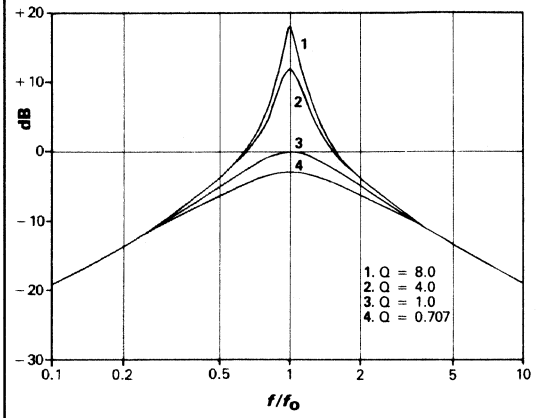



*Fig. 2 Bandpass Frequency Response for different Q Values*

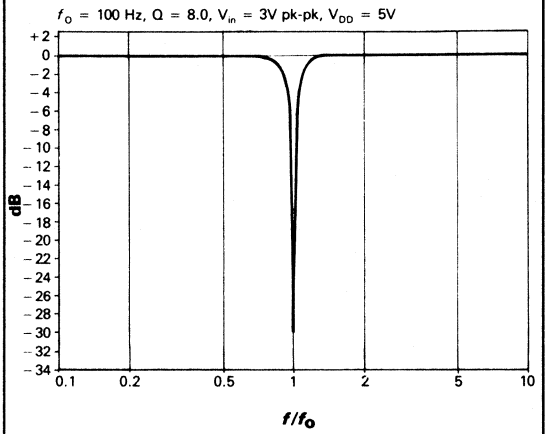



*Fig. 3 Notch Frequency Response*

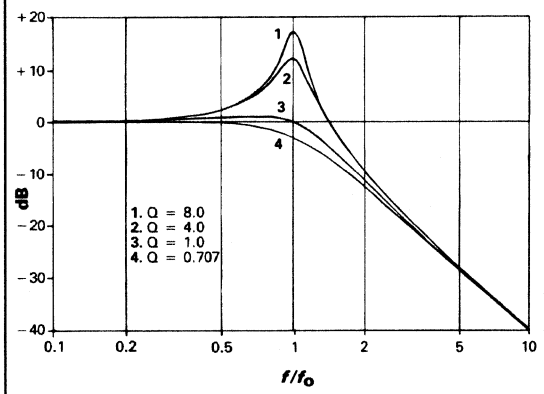



*Fig. 4 Lowpass Frequency Response for different Q Values*

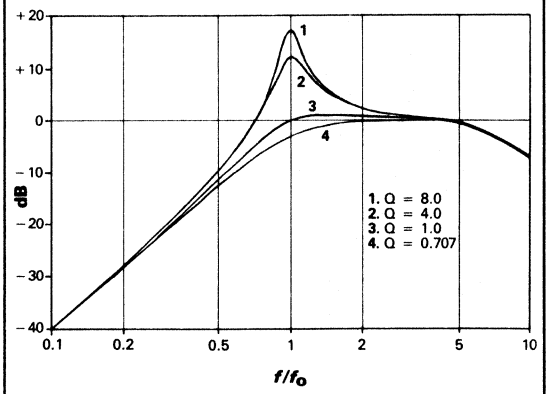



*Fig. 5 Highpass Frequency Response for different Q Values*

## PC4060 PCB For Design Evaluation

To assist in customer's design evaluation of the FX406, a PCB is available to enable external components to be connected for easy evaluation of application circuits.

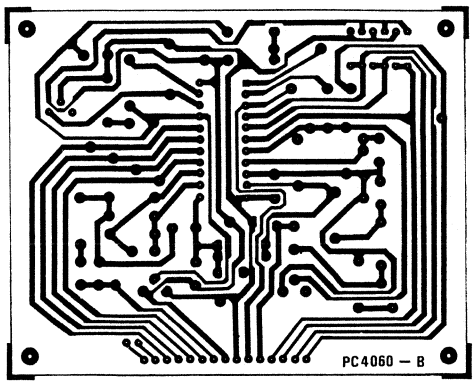



*Fig. 6 (a) Track Side*

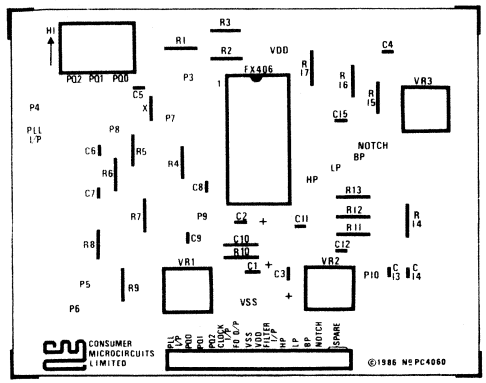



*Fig. 6 (b) Component Side*

*Fig. 6 PC4060 Printed Circuit Board*

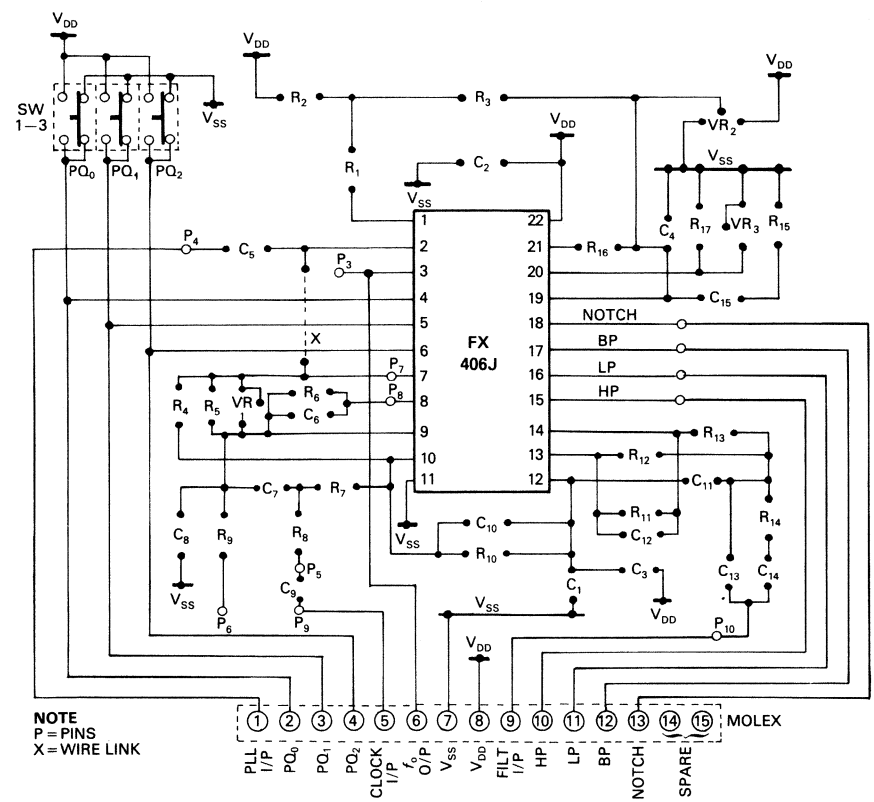



*Fig. 6 (c) PC4060 Printed Circuit Board Schematic Diagram*

## External Component Connections

The following examples of external component connections illustrate the basic modes of operation of the FX406. Where component references are used, these are the same as the circuit references on the PC4060 Evaluation PCB.

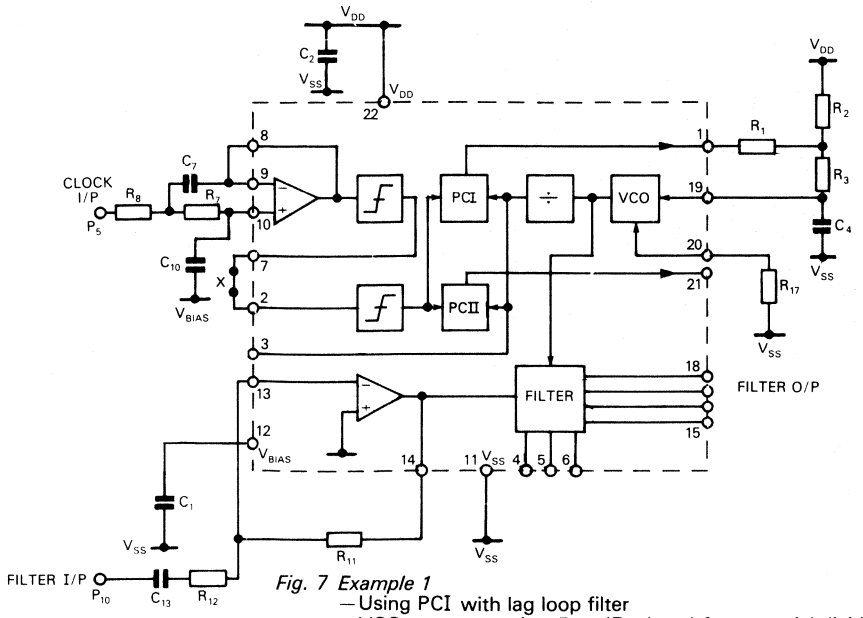



*Fig. 7 Example 1*

- Using PCI with lag loop filter
- VCO range set using $R_{max}$ ($R_{17}$) and $f_{min}$ potential divider ($R_1$, $R_2$)
- Filter input with simple gain adjustment
- Clock input pre-filtered with 2nd order LPF.

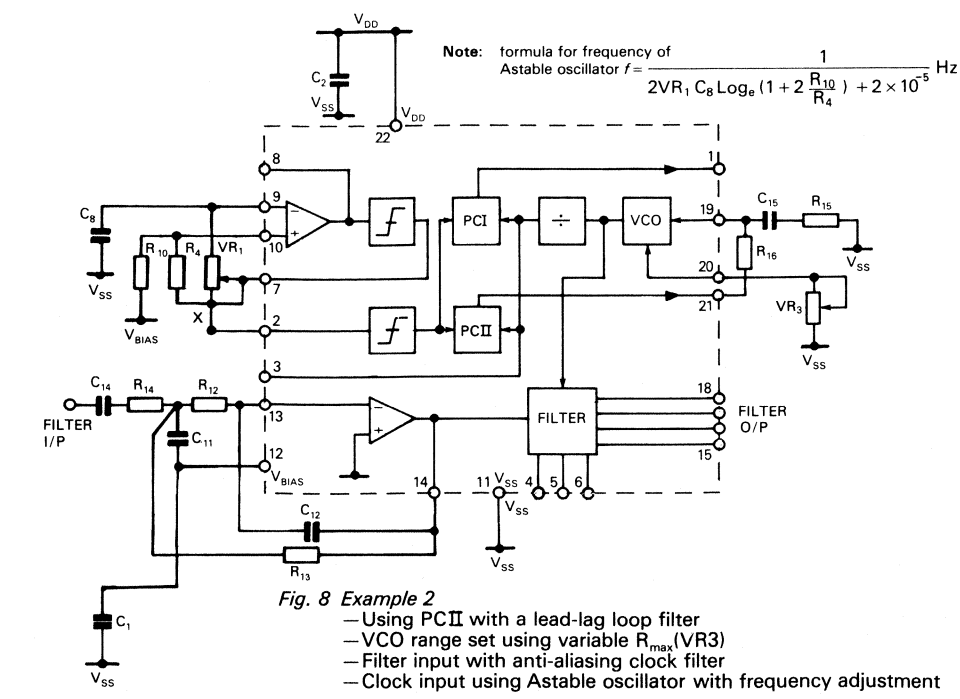



*Fig. 8 Example 2*

- Using PCII with a lead-lag loop filter
- VCO range set using variable $R_{max}$(VR3)
- Filter input with anti-aliasing clock filter
- Clock input using Astable oscillator with frequency adjustment

## Application Notes

### Note 1 — Setting VCO Frequency Range.

Set $f_{max}$* of VCO by selecting $R_{max}$ using graph in Fig. 9(a) & 9(b). If Phase comparator I is being used, it is also possible to set $f_{min}$ of the VCO by using the network shown in Fig. 9(c). $R_{min}$ may be determined using the graph in Fig. 9(c).

*Frequencies shown in graphs are actually $f_{VCO}/128$.

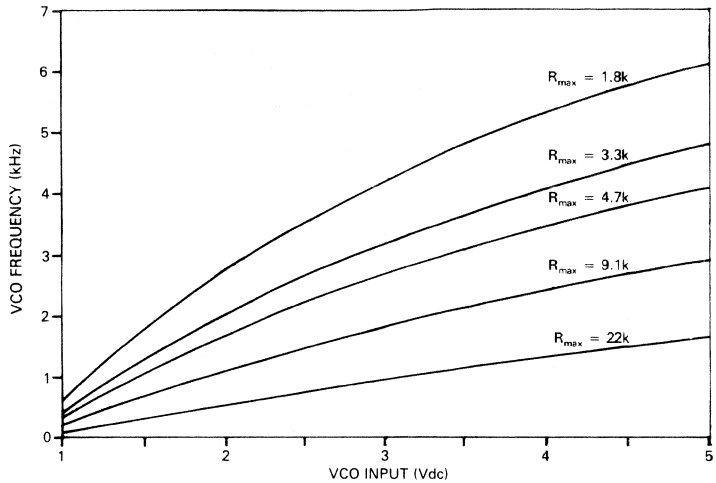



*Fig. 9(a) VCO Conversion Gain Curves For Different Values of $R_{max}$ ($R_{17}$)*

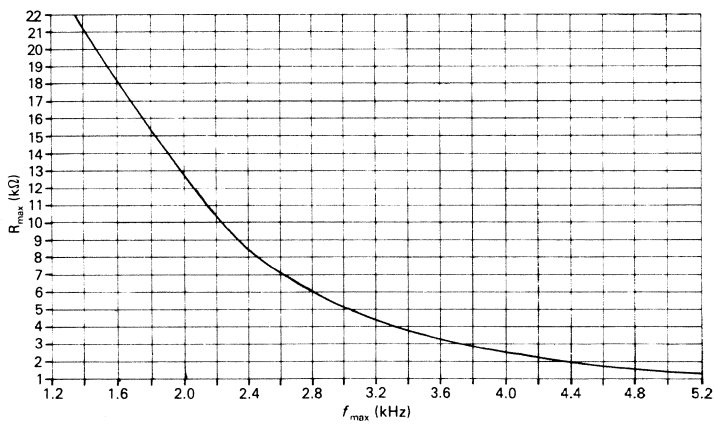



*Fig. 9(b) VCO $f_{max}$ Versus $R_{max}$ Curve*

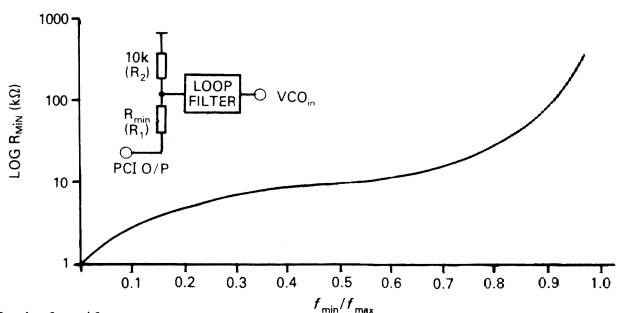



*Fig. 9(c) $R_{min}$ Versus Ratio $f_{min}/f_{max}$*

## Note 2 — Loop Filter Design

In order to maintain a fixed phase relationship between the VCO and reference input (or clock) signals, a 'second order loop' must be established. This is achieved by placing a lowpass filter between the phase comparator output and the VCO control input

This filter may be a 'lag' filter, (Fig.10a)or for improved stability a 'lead-lag' filter, (Fig10b).

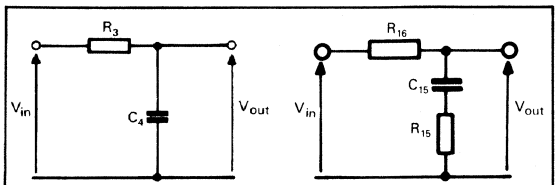



*Fig. 10(a) 'Lag' Filter* *Fig. 10(b) 'Lead-Lag' Filter*

The overall loop gain is given by $K_p . K_F \frac{K_{vco} . K_{div}}{j\omega}$

Where: $K_p$ = phase comparator gain in volts/radian.
$K_F$ = filter gain in volts/volt.
$K_{vco}$ = VCO conversion gain in radians/sec-volt.
$K_{div}$ = divider gain in radians/radian (1/128).

Selection of the frequency at which the loop gain is unity (0dB) depends on the application, the unity gain frequency should be high enough to allow the loop to track expected variations of the reference frequency but low enough to provide a 'flywheel' action to average noise and unwanted input transients.

Some typical loop filter component values for the FX406 using phase comparator II are tabled below.

| $f_{ug}$ Unity gain frequency (Hz) | $R_{17}=1.8k\Omega$ | | $C_{15}$ (F) |
|---|---|---|---|
| | $R_{16}$ (Ω) | $R_{15}$ (Ω) | |
| 50 | 92k | 13k | 1μ |
| 100 | 39k | 6k2 | 1μ |
| 250 | 200k | 62k | 0.1μ |
| 500 | 16k | 24k | 0.1μ |

When using phase comparator I, the locp filter frequency response may be used to limit the capture range of the loop, that is the range of input frequencies that the loop will lock onto. This property may be used to provide a degree of selectivity if required. The following table shows filter component values for various capture ranges. It should be noted that the loop filter used here is the simple 'lag' filter (i.e. $R_2 = 0$), this is to minimise ripple at 2 x $f_{in}$ on the loop filter output which would cause frequency modulation of the switched capacitor filter response.

| Capture Range $2f_c$ (Hz) | $R_3$ (Ω) | $C_4$ (F) |
|---|---|---|
| 100 | 470k | 340n |
| 200 | 100k | 390n |
| 500 | 100k | 68n |
| 1000 | 100k | 15n |
| 2000 | 100k | 3.9n |

## Note 3 — Phase Comparators

The following table shows the principal characteristics of second order loops using phase comparator I ('EX-OR') with a 'lag' filter and phase comparator II (edge-triggered) using a 'lead-lag' filter.

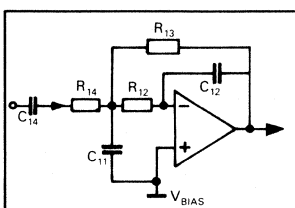
| | PC I | PC II |
|---|---|---|
| Input duty cycle | 50% optimum | don't care |
| Locks on harmonics of wanted signal | Yes | No |
| Noise rejection | Good | Poor |
| Ripple at 2 x $f_{in}$ on loop filter output | Yes | Low |
| Lock range, $2f_l$ | $f_{max}-f_{min}$ | $f_{max}-f_{ug}$ |
| Capture range, $2f_c$ | $\frac{1}{\pi}\sqrt{\frac{K_p K_{vco} K_{div}\pi}{2\tau_1}}$ | $f_{max}-f_{ug}$ |
| Frequency of VCO for no signal input | $\frac{f_{max}-f_{min}}{2}$ | $f_{min}$ |
| Phase angle between $f_{ref}$ and $f_{vco}/128$ in lock. | 0° at $f_{min}$<br>180° at $f_{max}$<br>90° at mid-point | 0° |

## Note 4 — Anti-aliasing

The relationship between $f_o$ and the switched capacitor sampling clock in the FX406 is $f_{clk}=64f_o$. This type of sampled filter produces alias or image responses centred on half the sampling rate, i.e., $32f_o$,

Filters with passbands extending beyond $32f_o$ will have spurious responses reflected into the passband at a corresponding distance below $32f_o$.

If the input frequency spectrum to the filter is likely to contain components at these alias frequencies then an additional RC filter is required to attenuate these inputs. This is easily accomplished by using the filter input amplifier, Fig. 11 shows a 2nd order 5kHz lowpass filter with passband gain suitable for values of $f_o$ above 250Hz.



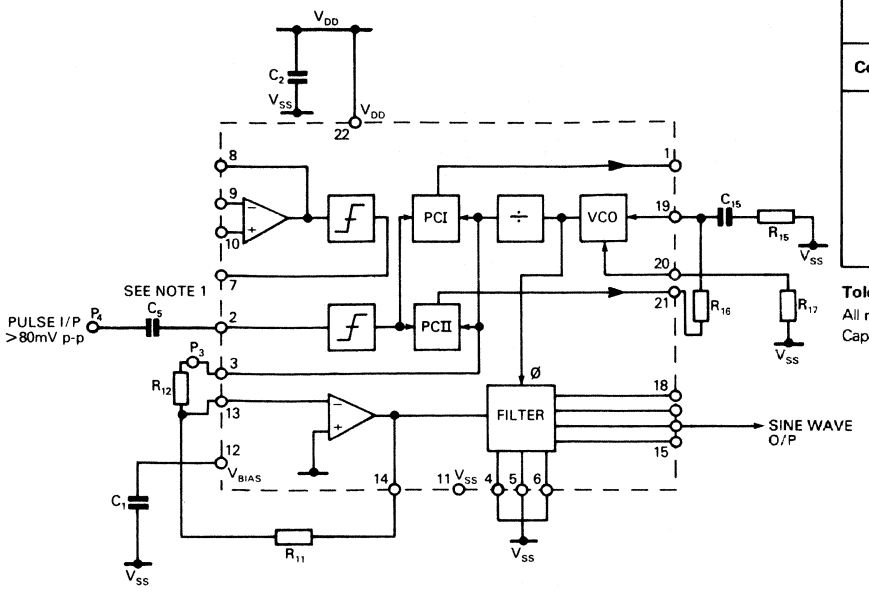

| | |
|---|---|
| $R_{12}$ | 47kΩ |
| $R_{13}$ | 100kΩ |
| $R_{14}$ | 100kΩ |
| $C_{11}$ | 560pF |
| $C_{12}$ | 150pF |
| $C_{14}$ | 0.1μF |

*Fig. 11 Anti-Aliasing Filter*

## Special Note

Care must be taken when using the FX406 with $f_o$ below 200Hz as the aliasing frequencies lie within the specified minimum passband of the filter.

On the highpass filter only, an additional lowpass response exists with its — 3dB point at $7f_c$ and a roll-off of 20dB/decade.

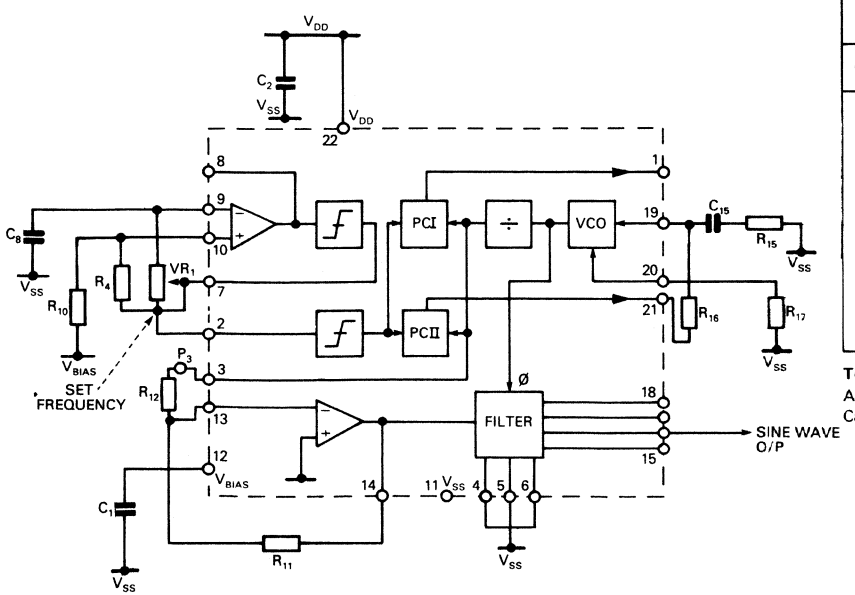



| Component References | |
|---|---|
| Component | Unit Value |
| $R_{11}$ | 24k |
| $R_{12}$ | 330k |
| $R_{16}$ | 39k |
| $R_{15}$ | 6.2k |
| $R_{17}$ | 1.8k |
| $C_1, C_2$ | 1.0µ |
| $C_5$ | 0.1µ |
| $C_{15}$ | 1.0µ |

**Tolerance**
All resistors ± 5%
Capacitors ± 20%

**NOTE 1**
*$C_5$ can be omitted for TTL or CMOS logic level input signals.*

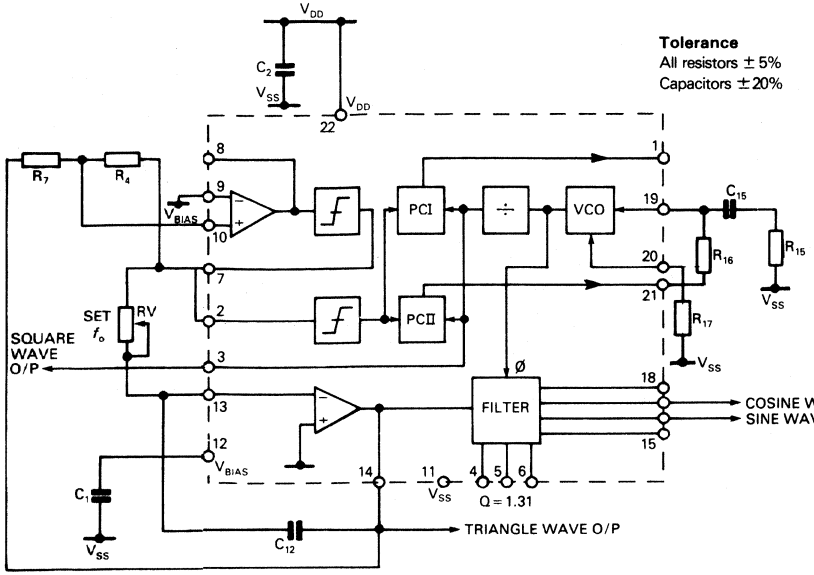
*Fig. 12 Pulse to Sine Converter*




| Component References | |
|---|---|
| Component | Unit Value |
| $R_4$ | 200k |
| $R_{10}$ | 100k |
| $R_{11}$ | 24k |
| $R_{12}$ | 330k |
| $R_{14}$ | 220k |
| $R_{15}$ | 13k |
| $R_{16}$ | 91k |
| $R_{17}$ | 1.8k |
| $C_1, C_2$ | 1.0µ |
| $C_8$ | 4.7n |
| $C_{15}$ | 1.0µ |
| $VR_1$ | 1MΩ |

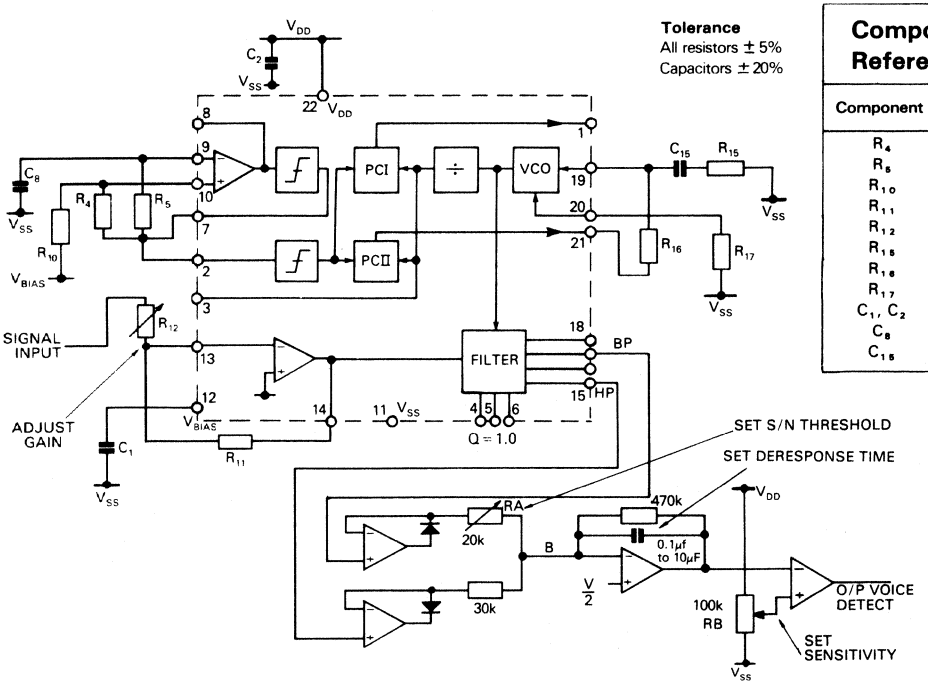
**Tolerance**
All resistors ± 5%
Capacitors ± 20%

*Fig. 13 1kHz Sine Wave Oscillator*




| Component References | |
|---|---|
| Component | Unit Value |
| $R_4$ | 180k |
| $R_7$ | 100k |
| $R_{15}$ | 13k |
| $R_{16}$ | 91k |
| $R_{17}$ | 1.8k |
| RV | 1M |
| $C_1$, $C_2$ | 1.0μ |
| $C_{12}$ | 4.7n |
| $C_{15}$ | 1.0μ |

*Fig. 14 Function Generator*




| Component References | |
|---|---|
| Component | Unit Value |
| $R_4$ | 100k |
| $R_5$ | 56k |
| $R_{10}$ | 100k |
| $R_{11}$ | 24k |
| $R_{12}$ | 30k |
| $R_{15}$ | 62k |
| $R_{16}$ | 200k |
| $R_{17}$ | 1.8k |
| $C_1$, $C_2$ | 1.0μ |
| $C_8$ | 10n |
| $C_{15}$ | 0.1μ |

**NOTES:**
1. *Adjust gain $R_{12}$ for largest filter output without clipping.*
2. *Vary $R_A$ to give $V_{\frac{1}{2}}$ at point B.*
3. *Set $R_B$ for threshold.*
4. *Set $C_A$ for de-response time.*

*Fig. 15 Voice Operated Switch*

| Component References | |
|---|---|
| **Component** | **Unit Value** |
| $R_4$ | 100k |
| $R_{10}$ | 100k |
| $R_{11}$ | 24k |
| $R_{12}$ | 330k |
| $R_{15}$ | 24k |
| $R_{16}$ | 16k |
| $R_{17}$ | 1.8k |
| $VR_1$ | 100k |
| $C_1, C_2$ | 1.0μ |
| $C_8$ | 4.7n |
| $C_{15}$ | 0.1μ |

**Tolerance**
All resistors ± 5%
Capacitors ± 20%

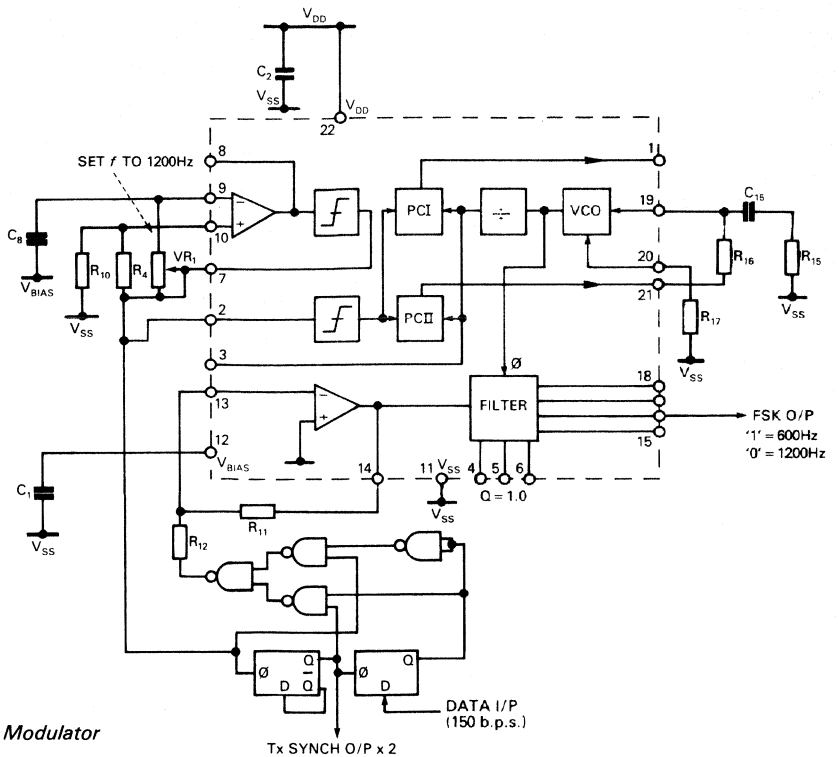



*Fig. 16 150 Baud FSK Modulator*

| Component References | |
|---|---|
| **Component** | **Unit Value** |
| $R_4$ | 200k |
| $R_{10}$ | 130k |
| $R_{11}$ | 270k |
| $R_{12}$ | 24k |
| $R_{17}$ | 1.8k |
| $VR_2$ | 50k |
| $C_1, C_2$ | 1.0μ |
| $C_{13}$ | 0.1μ |

**Tolerance**
All resistors ±5%
Capacitors ±20%

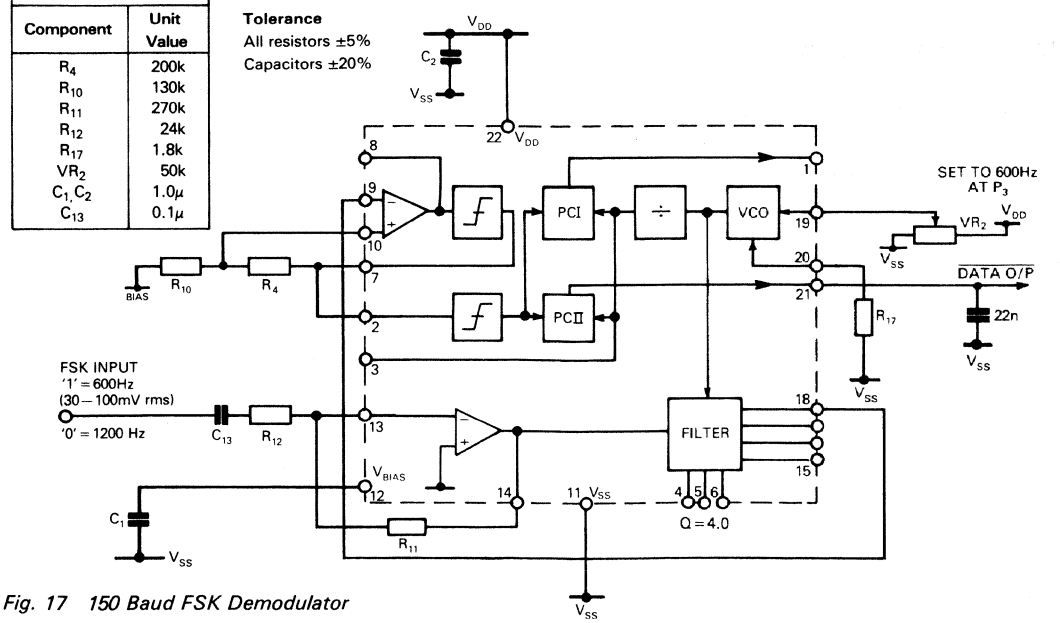
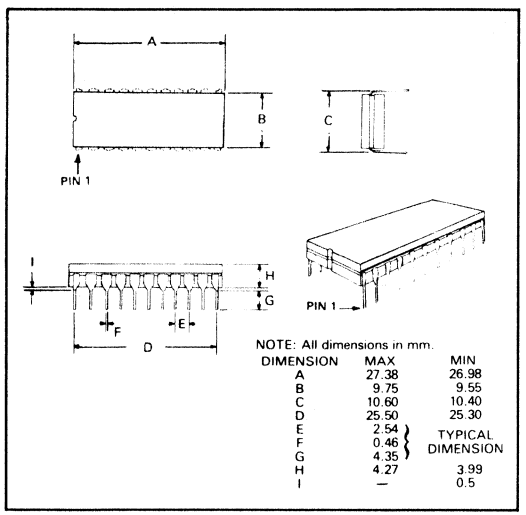



*Fig. 17 150 Baud FSK Demodulator*

## Package Outlines

The FX406J, the cerdip package, is illustrated in *Figure 18.* The 'LG' version is shown in *Figure 19,* and the 'LH' version in *Figure 20.* Both 'LG' and 'LH' packages are supplied in conductive trays for handling convenience. To allow complete identification, the FX406LG and LH packages have an indent spot adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 for LG package, between Pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).

*Fig. 18* **FX406J** Unifil™ *DIL Package*




NOTE: All dimensions in mm.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 27.38 | 26.98 |
| B | 9.75 | 9.55 |
| C | 10.60 | 10.40 |
| D | 25.50 | 25.30 |
| E | 2.54 | TYPICAL |
| F | 0.46 | DIMENSION |
| G | 4.35 | |
| H | 4.27 | 3.99 |
| I | — | 0.5 |

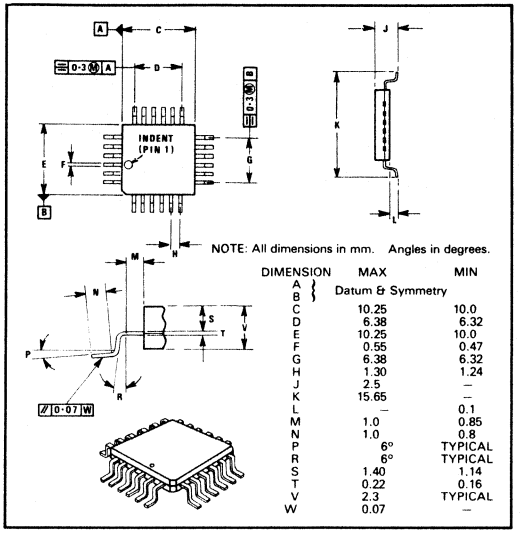
## Ordering Information

| | |
|---|---|
| **FX406J** | **22-pin cerdip DIL** |
| **FX406LG** | **24-pin quad plastic encapsulated, bent and cropped.** |
| **FX406LH** | **28-lead plastic leaded chip carrier.** |

## Handling Precautions

The FX406J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

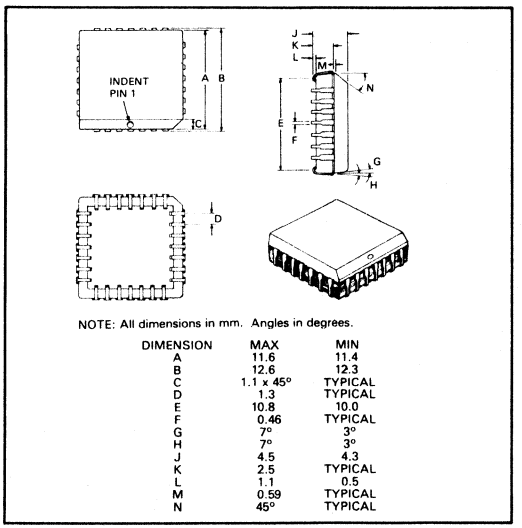
*Fig. 19* **FX406LG** Unifil™ *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A, B | Datum & Symmetry | |
| C | 10.25 | 10.0 |
| D | 6.38 | 6.32 |
| E | 10.25 | 10.0 |
| F | 0.55 | 0.47 |
| G | 6.38 | 6.32 |
| H | 1.30 | 1.24 |
| J | 2.5 | — |
| K | 15.65 | — |
| L | — | 0.1 |
| M | 1.0 | 0.85 |
| N | 1.0 | 0.8 |
| P | 6° | TYPICAL |
| R | 6° | TYPICAL |
| S | 1.40 | 1.14 |
| T | 0.22 | 0.16 |
| V | 2.3 | TYPICAL |
| W | 0.07 | — |

*Fig. 20* **FX406LH** Unifil™ *Package*




NOTE: All dimensions in mm. Angles in degrees.

| DIMENSION | MAX | MIN |
|---|---|---|
| A | 11.6 | 11.4 |
| B | 12.6 | 12.3 |
| C | 1.1 x 45° | TYPICAL |
| D | 1.3 | TYPICAL |
| E | 10.8 | 10.0 |
| F | 0.46 | TYPICAL |
| G | 7° | 3° |
| H | 7° | 3° |
| J | 4.5 | 4.3 |
| K | 2.5 | TYPICAL |
| L | 1.1 | 0.5 |
| M | 0.59 | TYPICAL |
| N | 45° | TYPICAL |



Note: **Unifil** ™ is the distinguishing 'TRADE MARK' *(Registration applied for)* of the product FX406.

# Integrated Circuits Data Book

Section 11

# Packaging and Applications

# CML Packaging

For ease and convenience CML products are packaged for despatch in industry standard bulk or individual packaging as described below.

- Trays (17cm x 10.5cm) and cardboard boxes with conductive foam.
- 50-pocket conductive trays for surface-mount microcircuits.
- Anti-static coated tubes, of various sizes, with thumbplugs.
- 13-inch reel Tape-and-Reel packaging which fully conforms to the latest EIC specification. The conductive embossed tape provides a secure cavity sealed with a peel-back cover tape. 500/1,000 units/reel (see Tape and Reel, Section 6.6) – no partial reel counts are available.

## CML Tape and Reel Specification

**1. Scope**

The specification relates to the tape packaging of integrated circuits suitable for use in "surface mount" assembly. It includes only those dimensions which are essential for the purchaser to use the product.

**2. Dimensions** (Refer to Figure 1)

**2.1 Tape Width (W)**

| | |
|---|---|
| LG, LH, LS, DW-20/24/28 | W = 24.0 ± 0.3mm |
| DW-16 | W = 16.0 ± 0.3mm |

**2.2 Carrier Tape Thickness (t)**

t = 0.3 ± 0.05mm

**2.3 Pitch of Sprocket Holes (Po)**

Po = 4.0 ± 0.1mm

**2.4 Diameter of Sprocket Holes (D)**

D = 1.5 + 0.1mm

**2.5 Distance (E)**

E = 1.75 ± 0.1mm

**2.6 Distance (F)**

F = 11.5 ± 0.1mm

**2.7 Dimension (P2)**

P2 = 2.0 ± 0.05mm

**2.8 Embossed Pocket Dimension (Ao and Bo)**

NOTE: These dimensions are measured at 0.3mm above the base of the pocket.

| | |
|---|---|
| LG | Ao = 15.8 ± 0.1mm |
| | Bo = 15.8 ± 0.1mm |
| LH | Ao = 13.1 ± 0.1mm |
| | Bo = 13.1 ± 0.1mm |
| LS | Ao = 11.7 + 0.1mm |
| | Bo = 11.7 + 0.1mm |
| DW-16 | Ao = 10.9 ± 0.1mm |
| | Bo = 10.7 ± 0.1mm |
| DW-20 | Ao = 10.9 ± 0.1mm |
| | Bo = 13.2 ± 0.1mm |
| DW-24 | Ao = 10.9 ± 0.1mm |
| | Bo = 15.8 ± 0.1mm |
| DW-28 | Ao = 10.9 ± 0.1mm |
| | Bo = 18.3 ± 0.1mm |

**2.9 Embossed Tape Dimension Ko**

| | |
|---|---|
| LG | Ko = 2.8 ± 0.1mm |
| LH | Ko = 4.9 ± 0.1mm |
| LS | Ko = 4.3 ± 0.1mm |
| DW-16/20/24/28 | Ko = 3.0 ± 0.1mm |

**2.10 Pitch of Component Compartments P1**

| | |
|---|---|
| LG | P1 = 20.0 ± 0.1mm |
| LH | P1 = 16.0 ± 0.1mm |
| LS | P1 = 16.0 ± 0.1mm |
| DW-16/20/24/28 | P1 = 12.0 ± 0.1mm |

**2.11 Outside Dimension of Pocket B1**

| | |
|---|---|
| LG | B1 = 16.5 ± 0.2mm |
| LH | B1 = 13.9 ± 0.2mm |
| LS | B1 = 12.4 ± 0.2mm |
| DW-16 | B1 = 11.4 ± 0.2mm |
| DW-20 | B1 = 13.9 ± 0.2mm |
| DW-24 | B1 = 16.5 ± 0.2mm |
| DW-28 | B1 = 18.9 ± 0.2mm |

**2.12 Pocket Centre Holes D1**

LG/LH/LS/DW D1 = 1.55 +1.0mm/-0.05mm

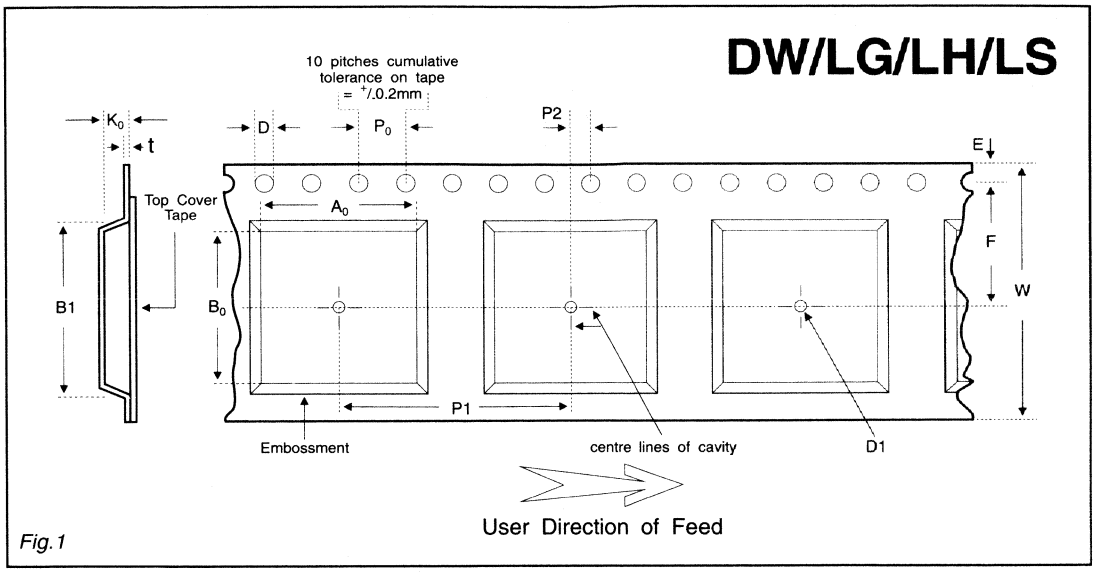



*Fig.1*

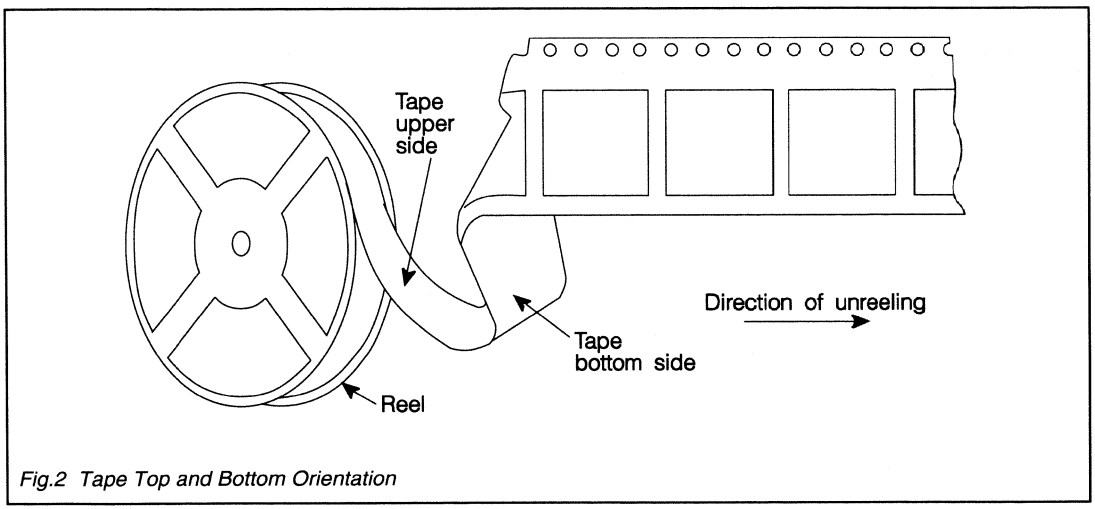



*Fig.2 Tape Top and Bottom Orientation*

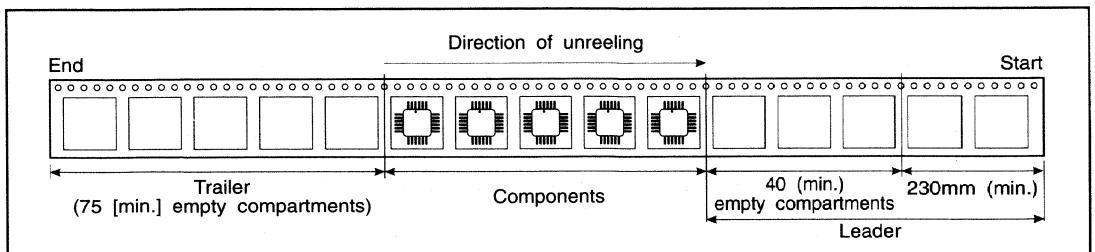



*Fig.3 Layout of Tape*

**3. Materials**

3.1 Carrier tape to be made of a conductive grade of polystyrene.

3.2 Conductive polycarbonate is also an approved carrier tape material and may be used under certain circumstances.

3.3 Cover tape is an anti-static grade of polypropylene/polyester or a PET/PE film.

**4. Polarity and Orientation of Components in Tape**

4.1 All components will be placed such that Pin 1 is adjacent to the sprocket holes (See Figures 6a, 6b and 6c).

4.2 The mounting side of the component shall be oriented to the bottom side of the tape (See Figure 2).

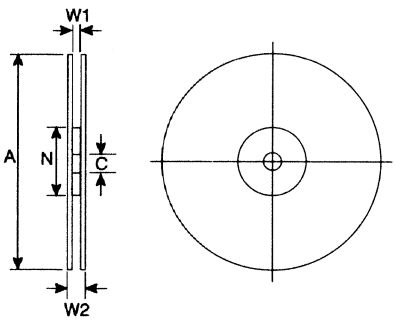


*Fig.4 Reel Dimensions*

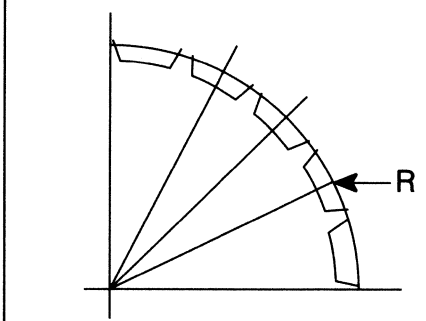


*Fig.5 Minimum Radius = 30mm*

**5. Fixing of Components in Tape**

5.1 Cover tapes shall not cover the sprocket holes.

5.2 Tapes in adjacent layers shall not stick together in the packing.

5.3 The adhesive of the cover tape shall not adversely effect the mechanical and electrical characteristics and marking of the components.

5.4 Components shall not stick to the carrier tape or the cover tape.

5.5 The tapes shall be suitable to withstand storage of the taped components without danger or migration of the terminations or the giving off of vapours which would impair soldering or deteriorate the component properties or termination by chemical action.

5.6 When the tape is bent with a minimum radius (See Figure 5) of 30mm, the tape shall not be damaged and the components shall remain in their position and orientation in the tape.

5.7 The peel strength of the cover tape shall be 50 ±25 grams measured at 175° - 180° with respect to the carrier tape along its longitudinal axis. The peel speed shall be 240mm/min.

5.8 After baking at 60°C for 48 hours or storage in ideal conditions for three months, the peel strength shall remain within the specified limits.

*Fig.6a*

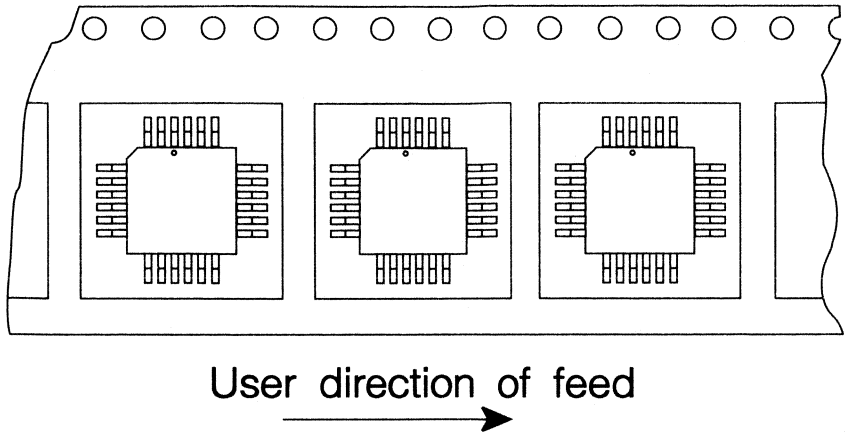



*Fig.6b*

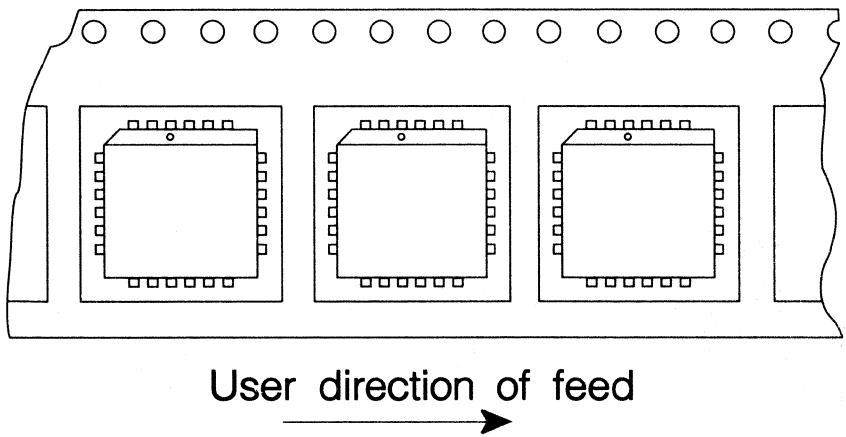



*Fig.6c*

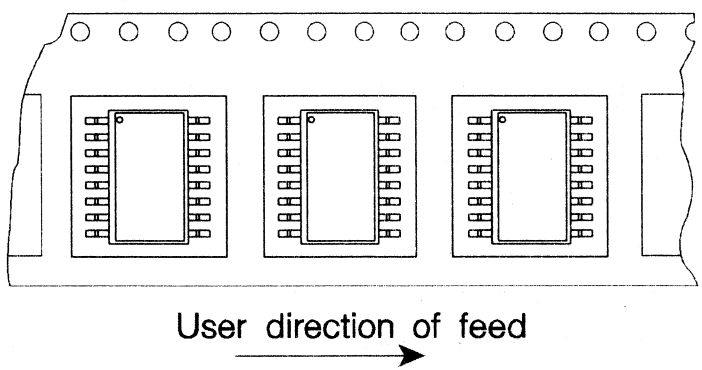



*Fig.6 Component Orientation*

# CML Packaging .....

## 6. Packaging

6.1 Tape will be wound on anti-static plastic reels (See Figure 4)

**Dimensions**

6.1.1

| A | C | N | W1 | W2 |
|---|---|---|---|---|
| Reel Dia. | Centre Hole | Hub Outer Dia. | Inside Cheek Width | Outside Cheek Width |
| 330mm | 12.7mm | 62.5mm | 24.5mm | 28.8mm |

6.2 There will be a leader of a minimum of 230mm followed by 40 empty compartments at the start of the carrier tape (See Figure 3).

6.3 There will be no missing components between the first and last part of working tape in any reel.

6.4 At the end of the tape there will be a trailer of a minimum of 75 empty compartments (See Figure 3).

6.5 The tape shall release from the reel hub as the last portion of the carrier tape unwinds from the reel.

6.6 Components on a reel.

LG = 500
LH = 500
LS = 500
DW = 1,000

6.7 The tape will be prevented from unreeling by winding a paper tape around the reel and fixing with adhesive tape.

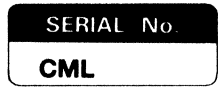
6.8 All reels will display:

1. Device Type
2. Quantity on reel
3. Date code
4. A static hazard warning label
5. CML Serial Number

6.9 Reel packed into anti-static bubble bag then in a cardboard box, with appropriate labelling as in paragraph 6.8.

6.10 Ideal storage conditions are 15°C to 20°C with a relative humidity of 60% - 70%.

6.11 Shelf-life when stored in ideal conditions will be in excess of six (6) months.



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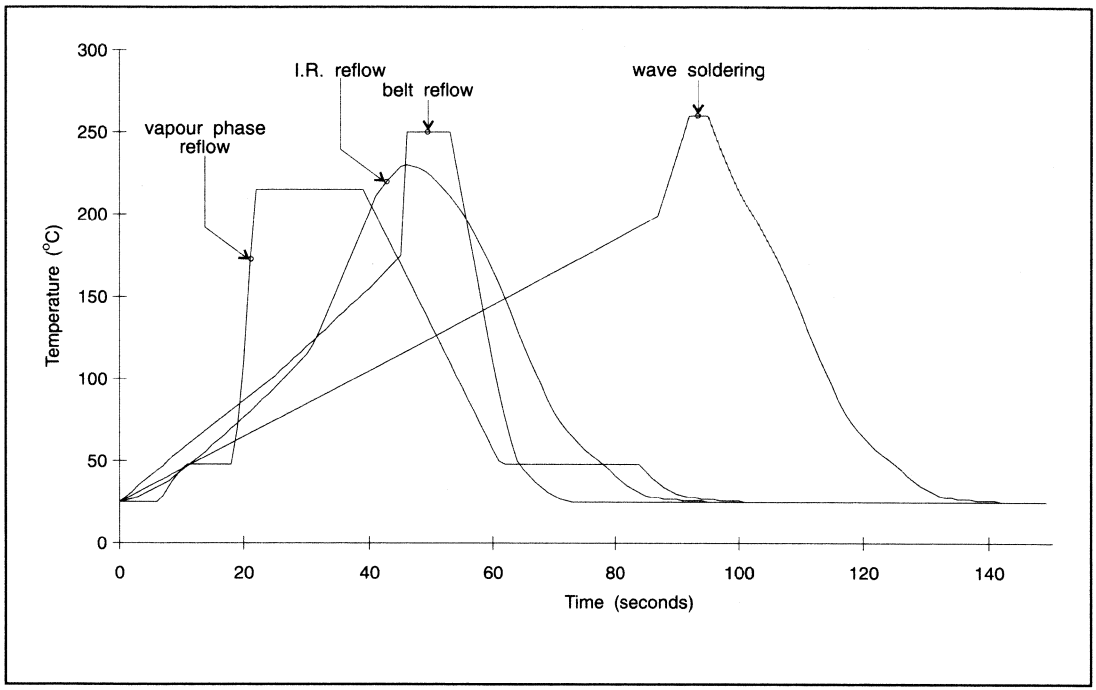
## Handling Precautions

CML microcircuits are CMOS LSI devices which include input protection. However precautions should be taken, at all times, to prevent static discharges which may cause device damage.

- It is recommended that the user initially stores and transports the microcircuit in the original supplied packaging.
- At all times observe anti-static precautions including the correct use of a conductive wrist-band and cord.
- Keep benches, personnel and test equipment at the same electrical potential.
- Ensure that the microcircuit is stored and operated well away from any potential source of static discharge.
- Do not insert or remove a microcircuit from an application whilst any power remains applied.
- Whenever possible ensure that the microcircuit is inserted after all other components have been mounted.
- Do not apply signals to a microcircuit until the power supply is suitably established.

# CML Microcircuit Soldering Profile



# Xtal Oscillator Circuits

Publication D/XT/2 December 1991

This Application Note discusses a general Xtal oscillator circuit applicable to most individual CML microcircuits.

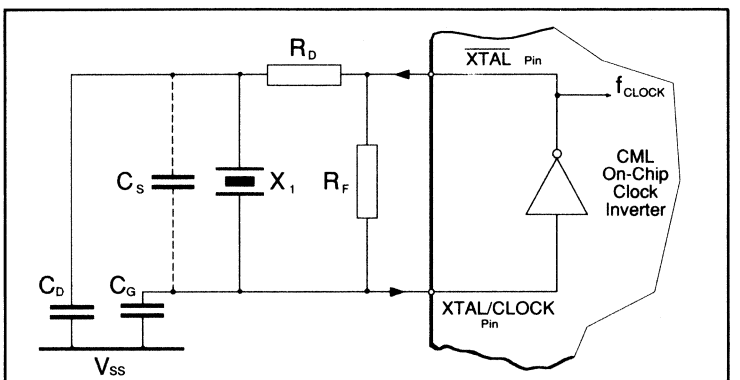
The figure below shows the standard Xtal oscillator circuit from which most recommended Data Sheet circuits are derived.

The standard on-chip CML CMOS oscillator circuit will function correctly with the majority of Xtals, however the use of this circuit with a few Xtal types may cause the following problems:

1. Excessive drive level to the Xtal.
2. Excessive over-voltage, outside the device maximum ratings, at the oscillator input pin. This over-voltage may show itself as degraded microcircuit performance.

**Note:** Operation of any CML microcircuit without a Xtal or clock input may cause device damage.

To minimise damage in the event of Xtal/drive failure, it is recommended that the power rail ($V_{DD}$) is fitted with a current limiting device (resistor or fast-reaction fuse).




*The Standard Xtal Oscillator Circuit*

## Standard Xtal Oscillator Components

**$R_F$ Feedback Resistor**

To set the bias point of the internal amplifier. Low values of $R_F$ will reduce loop-gain and disturb the phase of the feedback network. *Typical value = 1.0MΩ ± 20% in a range of 1.0MΩ to 20MΩ.*

**$R_D$ Drive Resistor**

Used to limit the Xtal drive level by forming a voltage-divider between $R_D$ and $C_D$. $R_D$ also stabilizes the oscillator against changes in the output impedance of the inverter. To verify that the maximum operating supply voltage does not overdrive the Xtal, observe the output frequency as a function at the buffered output. Under proper operating conditions the frequency should increase slightly (a few ppm) as the supply voltage increases. If the Xtal is being overdriven, an increase in supply will normally cause a decrease in frequency or instability. If the latter is the case (i.e. Xtal being overdriven), increase the value of $R_D$ *(refer to the Xtal manufacturers recommendations).*

**$X_1$ Xtal**

A parallel resonant Xtal to the value recommended in the relevant Data Sheet.

**$C_D$ Drain Capacitor**

To provide phase shift and reduce Xtal drive. Large values of $C_D$ tend to stabilize the oscillator against variations in power supply voltage but also reduce the tuning capability of the oscillator and overtone activity. *A typical value is 33.0pF ± 20% (Xtal manufacturer may recommend 5 – 40pF).*

**$C_G$ Gate Capacitor**

To provide phase shift and input voltage for the amplifier. In some oscillator circuits $C_G$ is used to adjust the oscillator to frequency although this generally may not be required. Large values of $C_G$ reduce loop-gain and increase stability. $C_G$ may be used to reduce over-voltage at the inverter input. However, the reduction in loop-gain may cause oscillator start-up problems. *$C_G$ value will be typically 5 – 65pF ± 20%, (refer to Xtal manufacturers recommendations).*

**$C_S$ Stray Capacitance**

Due to the low motional capacitance of small Xtals and the high inverter input impedance, the designer should be concerned with circuit board layout. For best oscillator performance $C_S$ should be less than 1.0pF.

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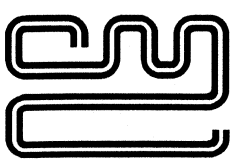

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